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A High Frequency, High Efficiency, High Power Factor Isolated On-board Battery Charger for Electric Vehicles

Yuqi Wei
University of Wisconsin-Milwaukee

A HIGH FREQUENCY, HIGH EFFICIENCY, HIGH POWER FACTOR ISOLATED ON-BOARD BATTERY CHARGER FOR ELECTRIC VEHICLES

by

Yuqi Wei

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ABSTRACT

A HIGH FREQUENCY, HIGH EFFICIENCY, HIGH POWER FACTOR ISOLATED ON-BOARD BATTERY CHARGER FOR ELECTRIC VEHICLES

by
Yuqi Wei

The University of Wisconsin-Milwaukee, 2018
Under the Supervision of Professor Adel Nasiri

In this paper, a high frequency, high efficiency and high power factor isolated on-board battery charger is proposed. The proposed topology includes two parts, AC/DC power factor correction (PFC) circuit unit and DC/DC converter unit. For the PFC circuit, SiC based totem-pole interleaved bridgeless PFC is selected, the diode bridge rectifier is eliminated. In addition, it can operate in continuous conduction mode (CCM) thanks to the low reverse recovery losses of the SiC MOSFETs. Besides, the interleaved technology minimizes the input current ripple. The DC/DC converter unit is composed of two LLC resonant converters sharing the same full-bridge inverter with constant switching frequency. The outputs of two LLC resonant converters are connected in series. One of the LLC resonant converter is operating at the resonant frequency, which is the highest efficiency operation point; while magnetic control is adopted for the second LLC resonant converter to fulfill the duty of providing closed-loop control for constant voltage (CV) and constant current (CC) charge modes. The proposed topology can achieve zero voltage switching (ZVS) for all primary switches and zero current switching (ZCS) for all secondary diodes during both CC and CV modes. Furthermore,

the constant switching frequency is simplified the electromagnetic interference (EMI) filter design. Simulation studies for 3.3kW power level and 100kHz switching frequency are performed, the simulation results are presented to verify the feasibility and validity of the proposed topology.

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How time flies! I can vividly remember the first day when I got here, it was like yesterday. I really enjoy my time in UWM. It would be one of the best memories in my life.

I would like to express my sincerely thanks to Professor David. C. Yu. He is so kind and helpful, both in life and study.

I really appreciate Professor Adel. Nasiri for being my supervisor. His rigorous academic attitude inspires me a lot. And his jokes make me nervous every time.

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Last but not least, I want to thank my family and my girlfriend. I don’t think I can finish my study without their support.

After my graduation from UWM, I become more confident. And I believe a bright future is awaiting for me.

Chapter 1 Introduction

With the development of society, the environmental problems are becoming more and more serious. Greenhouse emission is one of the most serious problems, which is mainly caused by excessively using of fossil fuels. Therefore, people are more concern about green energy, and there is a growing interest in the development of electric vehicles (EV) and plug-in hybrid electric vehicles (PHEV) [1]-[3]. Meanwhile, equipped with bidirectional battery charger, the vehicles can offer the power grid a flexible load, known as vehicle to grid (V2G) mode, which can contribute to utility operation by providing ancillary services. Typically, the ancillary services include grid regulation, spinning reserves, source of energy, peak shaving and voltage support.

However, up to now, EVs have not gain wide acceptance. There are basically three barriers: 1) high cost and cycle life of batteries; 2) complications of battery chargers; 3) lack of charging infrastructure. Furthermore, the harmonics effect is also an existing problem [4].

Basically, there are three power levels, that is, level 1, level 2 and level 3. Level 1 is usually adopted in home application and it is also known as slow charging; level 2 charging can be used both in private and public place, and it will be the focus of the future development; level 3 or DC fast charging are intended for commercial and public applications, and three-phase solutions are normally applied [5]. In this paper, single phase on-board battery charger for level 1 and level 2 applications will be discussed in detail.

For level 1 and level 2 charging, the on-board battery charger is always adopted, and the power is

range from 1.4kW to 19.2kW [5]. Figure 1-1 shows a conventional two-stage on-board battery charger. In this structure, a full-bridge diode rectifier is adopted to convert the input AC voltage to DC voltage, followed by a Boost PFC unit, which can provide unity power factor for the circuit, and an isolated DC/DC converter is used to regulate the output voltage and provide electrical isolation between the AC input and the battery.

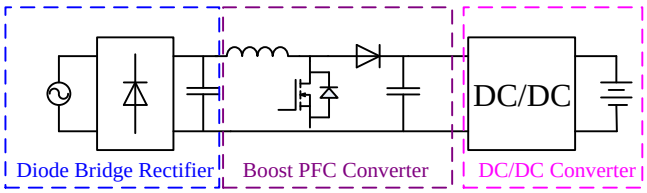


Figure 1-1 Conventional two-stage battery charger.

According to [6], it has specific requirements for the device. For the input power supply, the input voltage is the nominal voltage in each country with a variation of ± 15%, and the frequency is 50Hz or 60Hz with a variation of ± 5%; the output voltage is range from 50V to 500V DC, and output current is range from 0A to 125A; the limitation for the current ripple is 1.5A for 10Hz and 3.0A for 5kHz; the efficiency of the AC/DC conversion should be greater than 90% on the condition with maximum rated output power and current of the charger, which includes auxiliary loss; there are also requirements for acoustic noise, communication system and protection system. In addition, the standard also points out the isolation requirement between the input AC circuit and output DC circuit. Generally, the characteristics of an on-board battery charger are summarized as follows: 1) wide range of input voltage and output voltage; 2) low current ripple; 3) high efficiency; 4) electrical isolation between the input and output; 5) high power factor; 6) compact and light.

Based on the above discussion and existed topologies, there are basically two ways to improve the

performance of the system and satisfy the requirements. As we can see from Figure 1-1, the first direction for improvement is the PFC unit, which can be integrated with full-bridge diode rectifier or the isolated DC/DC converter. By doing so, the component counts will be reduced, and system efficiency will be improved; meanwhile, the interleaved technology can be adopted to reduce the current ripple and increase the power handling ability; the second improvement direction is isolated DC/DC converter, different topologies and control strategies are proposed to reduce power losses and improve efficiency, such as full-bridge converter, LLC resonant converter, dual active bridge (DAB) converter.

In this thesis, the AC/DC PFC unit is discussed in Chapter 2, different PFC topologies are analyzed and compared, a SiC based totem-pole interleaved bridgeless PFC is analyzed, including operation principles, design considerations and closed-loop design; in Chapter 3, the full-bridge LLC resonant converter is introduced, including operation analysis, modeling and basic characteristics; based on the analysis in Chapter 2 and 3, a high frequency, high efficiency and high power factor isolated on-board battery charger is proposed, its operation analysis and design considerations are presented in Chapter 4; in Chapter 5, the magnetic control is introduced and compared with other control schemes; in addition, the design considerations and modeling for the variable inductor are provided; finally, a conclusion is drawn in Chapter 6, and the future work is pointed out.

Chapter 2 SiC Based Totem-pole Interleaved Bridgeless Power Factor Correction Circuit

Conventionally, the power factor correction (PFC) circuit is shown in Figure 2-1 [7]. Obviously, it contains two parts, one is the diode bridge rectifier and another one is the Boost PFC converter. It can be seen that this topology is complicated and contains three semiconductors when the switch is on or off. It is noteworthy to mention that the losses of diode bridge rectifier take up a large percent of the total losses. Specifically, it takes up 30%-60% of the total losses. Therefore, many researchers focus on how to reduce components and improve the system efficiency. The bridgeless PFCs have been put forward [8]-[12]. Among all of them, the totem-pole bridgeless PFC has gained much attention due to the following characteristics: 1) no common-mode interface problem since the output is clamped to the input by diodes during each half cycle; 2) the circuit configuration is quite simple; 3) it is easy to achieve bi-directional power conversion. The totem-pole bridgeless PFC is shown in Figure 2-2.

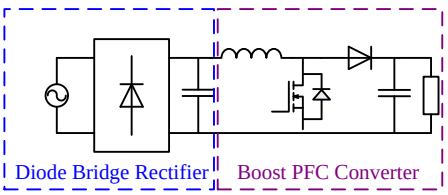


Figure 2-1 Traditional Boost PFC converter.

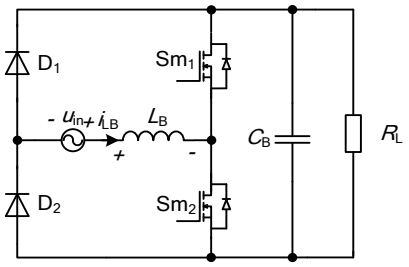


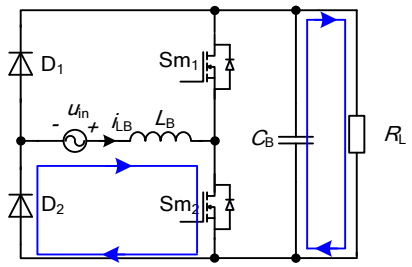
Figure 2-2 Totem-pole bridgeless PFC.

However, due to the bad performance of the body diodes of the MOSFETs, this topology is not suitable to operate in continuous conduction mode (CCM). To solve this problem, many methods have been proposed. In this research, a totem-pole bridgeless PFC based on Silicon-Carbide (SiC) device is adopted, which can operate in CCM with the help of the low reverse recovery charge of SiC body diode. Specifically, SiC power MOSFETs (C2M0160120D) from CREE are selected as an example. The reverse recovery charge of body diode is 192nC, which is quite small when compared with typical 2uC for a counterpart Si body diode [13]. In addition, the low turn-on resistance of SiC devices can further increase the system efficiency.

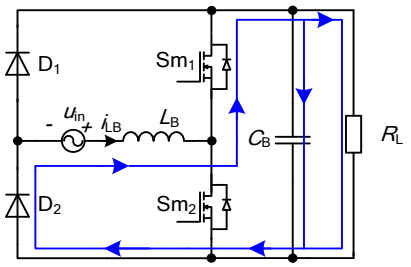
In this chapter, the operation analysis of the totem-pole bridgeless PFC is discussed firstly; then a simulation case is presented to verify the theoretical analysis; next, the interleaved technology is introduced and the analysis for the SiC based totem-pole interleaved bridgeless PFC is presented; the design considerations are discussed and a simulation case is introduced to verify the analysis; finally, the comparison between traditional PFC, totem-pole bridgeless PFC and SiC based totem-pole interleaved bridgeless PFC is presented and a brief summary is drawn.

2.1 Operation Analysis for Totem-pole Bridgeless PFC

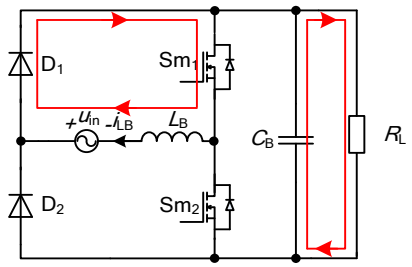
The configuration of the totem-pole bridgeless PFC is shown in Figure 2-2, generally, there are four different operation modes (the dead time is ignored here to simplify the analysis). When the input voltage is in its positive half cycle, diode D_1 keeps ON, switch S_{m1} acts like a Boost switch, while switch S_{m2} acts like a freewheeling diode. Therefore, when S_{m1} is ON, it is in charging state, when it is OFF, the circuit is in after-flow mode. Due to the symmetry of the circuit, the operation principles in negative half cycle are the opposite of the positive cycle, that is, diode D_2 keeps ON, switch S_{m2} acts like a Boost switch, switch S_{m1} acts like a freewheeling diode. And the operation details are shown in Figure 2-3.



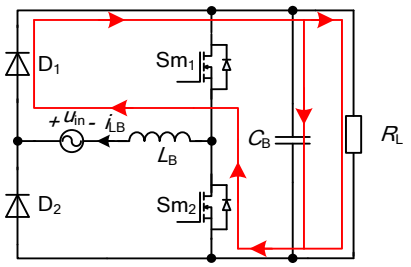
(a) Positive cycle charging mode.



(b) Positive cycle after-flow mode.



(c) Negative cycle charging mode.



(d) Negative cycle after-flow mode.

Figure 2-3 Four different operation modes.

One of the most significant advantages of totem-pole bridgeless PFC is that it can achieve power factor correction function automatically (without additional control). The principle behind it is shown in Figure 2-4. This only works when the circuit operating in discontinuous conduction mode (DCM). Obviously, the envelop curve of the boost inductor current i_{LB}, which is also the input current of the circuit, follows the input voltage and forms a sine wave. Therefore, the power factor can be corrected without additional control.

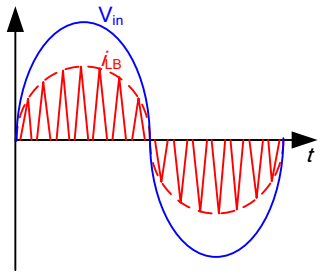


Figure 2-4 Waveforms of the inductor current and input voltage under DCM.

2.2 Simulation Verification for Totem-pole Bridgeless PFC

In this part, a simulation case for totem-pole bridgeless PFC is presented to verify the above analysis. The simulation parameters are shown in Table 2-1.

Table 2-1 Simulation parameters for totem-pole bridgeless PFC.

Input voltage U_{in}	220V
Inductor L_B	30uH
Output Capacitor C_B	500uF
Switching frequency f_s	100kHz

Output voltage V_o	400V

Figure 2-5 shows the waveforms of input voltage (blue) and input current (red). It can be seen that the input current is in phase with input voltage and it can achieve power factor correction function automatically. In addition, Figure 2-6 shows the waveform of inductor current, it can be seen that the inductor current is operating in DCM. Figure 2-7 shows the waveform of output voltage.

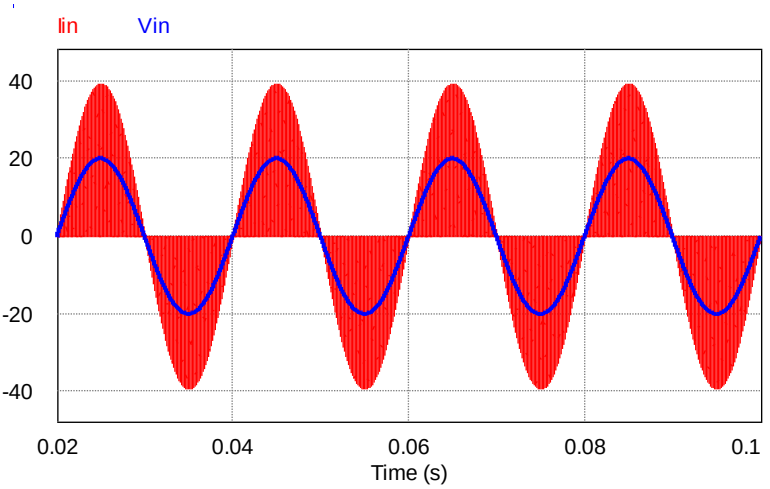


Figure 2-5 Simulation waveforms of input voltage and input current.

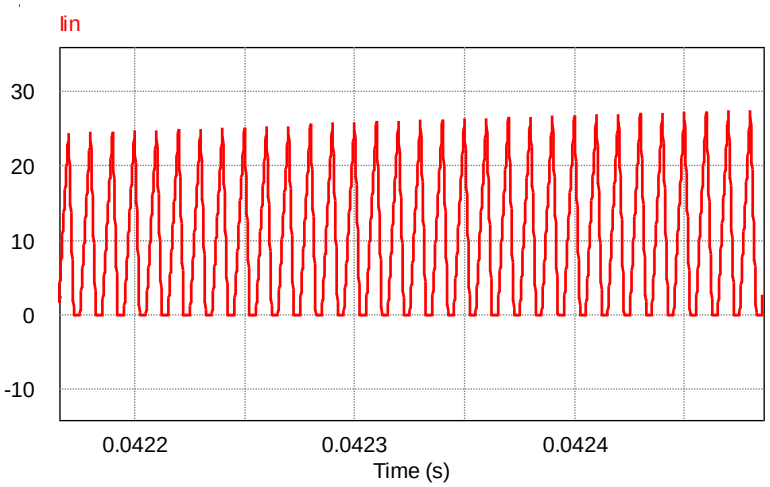


Figure 2-6 Simulation waveform of inductor current.

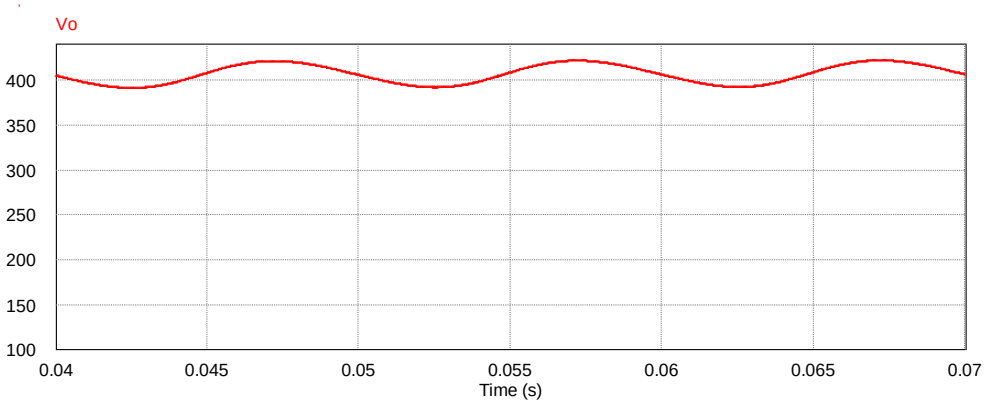


Figure 2-7 Simulation waveform of output voltage.

2.3 SiC Based Totem-pole Interleaved Bridgeless PFC Analysis

For totem-pole bridgeless PFC, there are some disadvantages: 1) it can only operate at DCM, the reverse recovery problem of the body diodes of MOSFETs limits its operation in CCM; 2) the ripple of the input current is relatively high, which requires an additional filter; 3) the power handing ability is relatively low (typical power rating is below 1kW). In order to solve these problems, lots of methods have been put forward.

For problem 1, the SiC device can be adopted to solve the problem, for SiC based totem-pole bridgeless PFC, due to manufacture, the reverse recovery problem is too small that can be ignored, so the circuit can operate in CCM.

For problem (2) and (3), the interleaved PFC circuits have been proposed recently [14]-[16]. The most often used topology is interleaved Boost PFC shown in Figure 2-8. This is a two-leg interleaved Boost PFC, the phase difference between S_1 and S_2 is 180 degrees, so the ripples cancel out completely or to some extent, depending on the duty ratio. The relation between duty ratio and

normalized current ripple is shown in equation (2-1) and Figure 2-9. It can be seen that when D=0.5, the ripples are canceled out completely.

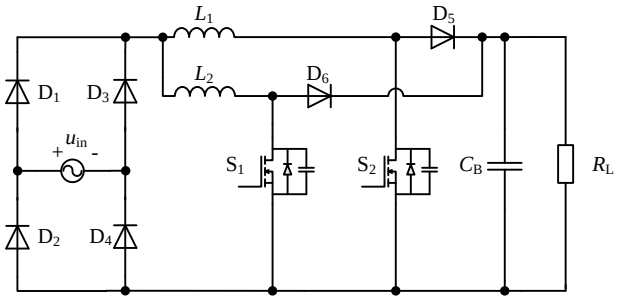


Figure 2-8 Interleaved Boost PFC.

$$K(d)=\frac{\Delta i_{in}}{\Delta i_L}=\begin{cases}\dfrac{1-2d}{1-d} & d<0.5\\ \dfrac{2d-1}{d} & d\geq 0.5\end{cases} \tag{2-1}$$

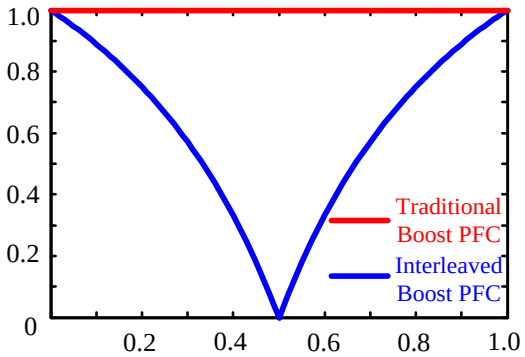


Figure 2-9 Normalized current ripple with different duty ratios.

Another advantage for the interleaved Boost PFC is that the input current is shared evenly between two inductors, and the energy stored in inductors is

$$E=\frac{1}{2}L\left(\frac{i_{in,rms}}{2}\right)^2+\frac{1}{2}L\left(\frac{i_{in,rms}}{2}\right)^2=\frac{1}{4}Li^2_{in,rms} \tag{2-2}$$

Compared with the traditional Boost PFC, the energy stored in inductor is shown in equation (2-3), the energy is reduced 50%. Therefore, a relatively small volume inductor can be selected to

achieve the same goal, the system is more compact.

$$E = \frac{1}{2} L i_{in,rms}^2 \tag{2-3}$$

However, for the interleaved Boost PFC, there still exist some problems: 1) there are four semiconductors during the path, so the conduction losses will be increased; 2) 8 semiconductors are required for this topology, which is complicated. Therefore, in this research, combined with totem-pole bridgeless PFC and interleaved technology, the SiC based totem-pole interleaved bridgeless PFC is studied.

2.3.1 Operation Analysis for Interleaved Totem-pole Bridgeless PFC

The topology of the interleaved totem-pole bridgeless PFC is shown in Figure 2-10, where two Boost interleaved phases (L_{B1}, S_{m1}, S_{m4} and L_{B2}, S_{m2}, S_{m3}) are driven with 180 degrees phase difference.

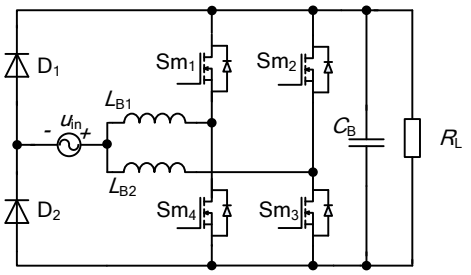
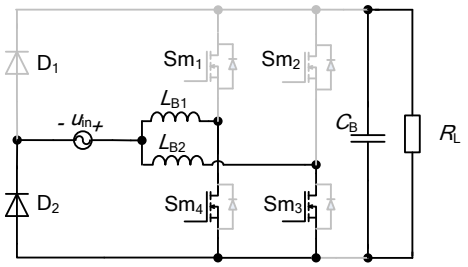
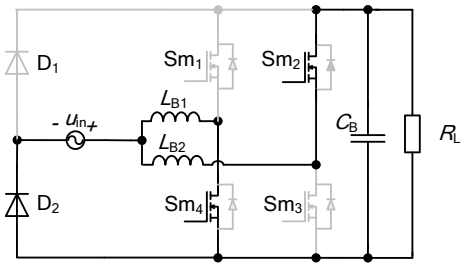


Figure 2-10 Interleaved totem-pole bridgeless PFC.

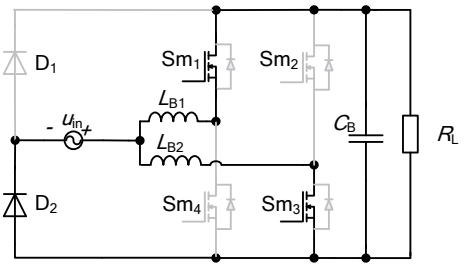
The analysis is simplified by ignoring the parasitic capacitance of the MOSFETs. Only half cycle is discussed here because of the symmetric characteristic of the topology. Obviously, there only exist four operation modes during half cycle, which are shown in Figure 2-11 (a), (b), (c) and (d).



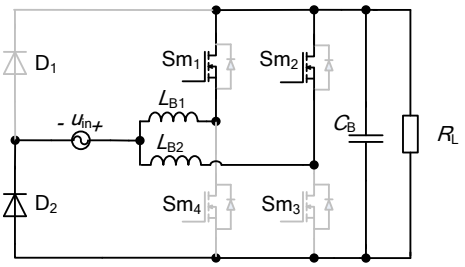
(a) Two lower switches are ON.



(b) One lower switch and one upper switch are ON.



(c) One lower switch and one upper switch are ON.



(d) Two upper switches are ON.

Figure 2-11 Equivalent circuits for different modes in positive half cycle.

Mode 1: As shown in Figure 2-11 (a), both lower switches are ON. In this mode, the currents flow through the inductor L_{B1} and L_{B2} can be easily obtained

$$\frac{di_{LB1}}{dt}=\frac{di_{LB2}}{dt}=\frac{u_{in}}{L_B} \tag{2-4}$$

In this research, L_{B1}=L_{B2}=L_B. Therefore, in mode 1, currents through L_{B1} and L_{B2} are increasing. The equivalent circuit in this mode is shown in Figure 2-12.

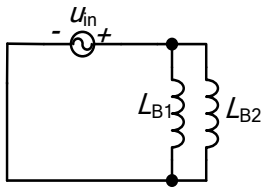


Figure 2-12 Equivalent circuit in Mode 1.

Mode 2: In this mode, both upper switches are ON, and the equivalent circuit is shown below.

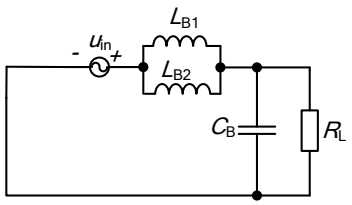


Figure 2-13 Equivalent circuit in Mode 2.

Similarly, the currents flow through L_{B1} and L_{B2} can be expressed as

$$\frac{di_{LB1}}{dt} = \frac{di_{LB2}}{dt} = \frac{u_{in} - u_o}{L_B} \tag{2-5}$$

Since the output voltage is greater than the input voltage, the currents flow through L_{B1} and L_{B2} start decreasing.

Mode 3: In this mode, where one upper MOSFET and one lower MOSFET are ON. The equivalent circuit is shown below.

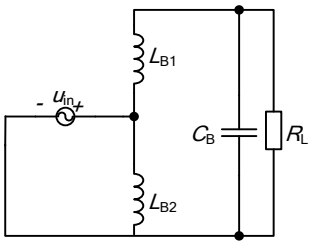


Figure 2-14 Equivalent circuit in Mode 3.

The currents flow through L_{B1} and L_{B2} can be expressed as

$$\frac{di_{LB1}}{dt} = \frac{u_{in} - u_o}{L_B} \tag{2-6}$$

$$\frac{di_{LB2}}{dt} = \frac{u_{in}}{L_B} \tag{2-7}$$

According to equation (2-6) and (2-7), in this mode, one of the inductor currents is increasing, while another one is decreasing.

Figure 2-15 shows the theoretical waveforms when duty cycle is greater than 0.5, where i_{in} is the input current. In this case, the input voltage is lower than the half of output voltage, and during a switching period, it has four stages.

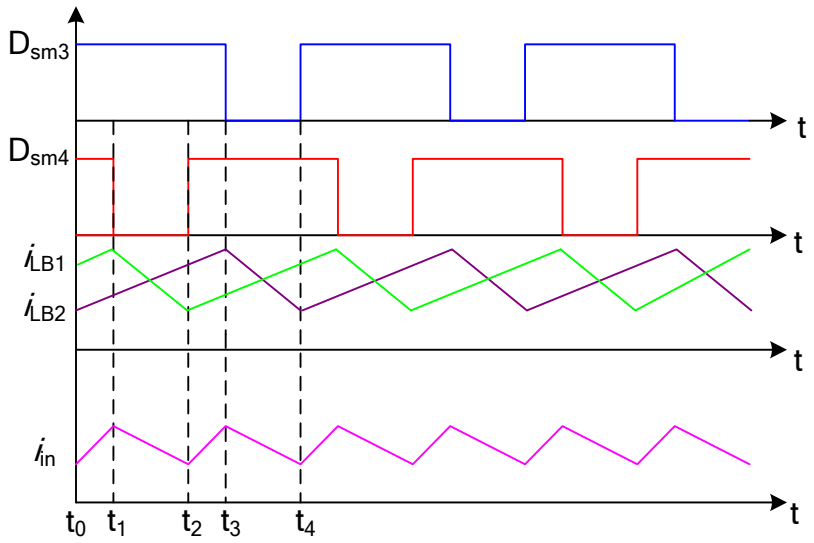


Figure 2-15 Theoretical waveforms of interleaved totem-pole bridgeless PFC when D is greater than 0.5.

Stage 1 [t_0-t_1]: During this stage, both switches are ON, which is Mode 1, the currents i_{LB1}, i_{LB2} and i_{in} will increase gradually;

Stage 2 [t_1-t_2]: In this stage, one lower and one upper switch are ON, which is Mode 3. At t_1, S_{m4} turns OFF; meanwhile, the upper switch S_{m2} acts as a freewheeling diode in this stage. Current flow through L_{B1} starts decreasing; i_{LB2} continues increasing, while i_{in} decreases slowly.

Stage 3 [t_2-t_3]: At t_2, S_{m4} turns ON, and both lower switches are ON, which is the same in stage 1.

Stage 4 [t_3-t_4]: At t_3, S_{m3} turns OFF, one upper switch is ON, and one lower switch is OFF, which

is the opposite of stage 2.

Similarly, the waveform of duty cycle lower than 0.5 is shown below.

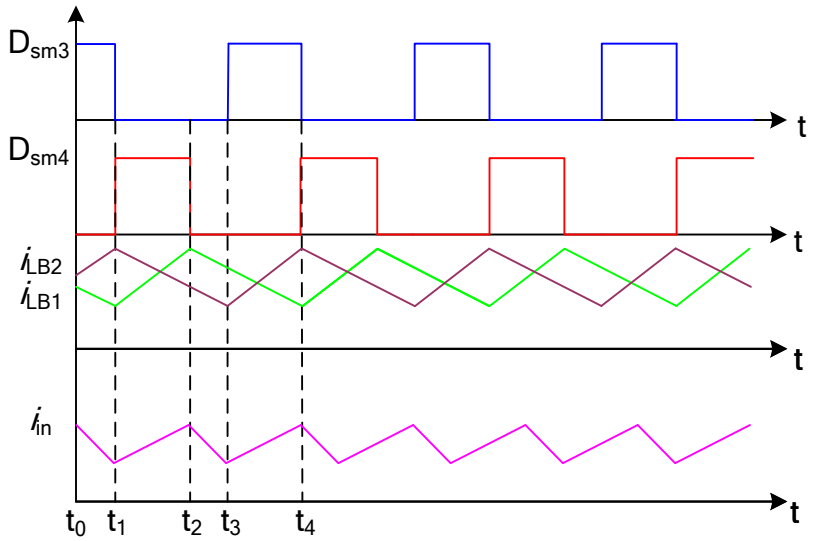


Figure 2-16 Theoretical waveforms of interleaved totem-pole bridgeless PFC when D is lower than 0.5.

2.3.2 Design Considerations for Interleaved Totem-pole Bridgeless PFC

In this part, the design considerations for the interleaved totem-pole bridgeless PFC are discussed. For the Boost inductors L_{B1} and L_{B2}, the current ripple requirement is adopted to define the value; for the output capacitor, the voltage ripple requirement is adopted to define the value. Firstly, the known parameters are shown in Table 2-2.

Table 2-2 Known parameters for the system.

Input voltage U_{in}	90V-264V
Output power P_o	330W-3.3kW
Switching frequency f_s	100kHz

Output voltage V_o	400V

The design guideline for the inductors L_{B1} and L_{B2} are the current ripple requirement. In this research, the maximum current ripple is selected to be 20% of its average value. The inductor current ripple can be expressed as

$$\Delta i_{LB} = \begin{cases} \frac{u_{in}}{u_o} T_s \frac{u_o - u_{in}}{L_B}, u_{in} \le u_o / 2 \\ (1 - \frac{u_{in}}{u_o}) T_s \frac{u_{in}}{L_B}, u_{in} \ge u_o / 2 \end{cases} \tag{2-8}$$

$$\Delta i_{LB} = \frac{P_{o,max}}{u_{in}} \times 20\% \tag{2-9}$$

According to equation (2-8) and (2-9), the inductor value can be expressed as

$$L_B = \frac{u_{in}{}^2 (u_o - u_{in})}{P_{o,max} \times f_s \times u_o \times 20\%} \tag{2-10}$$

Based on equation (2-10), L_{B1}=L_{B2}=L_B=360uH is selected.

For the output capacitor, it can be determined according to the following equation, where the voltage ripple is 5%.

$$C_B = \frac{P_o}{2\pi f_L V_o \Delta V_o} = 1300uF \tag{2-11}$$

where f_L is the input line frequency.

The next step is to find the voltage and current stress of the MOSFETs and diodes, which provide guidance for selecting MOSFETs and diodes.

The voltage stresses on the MOSFETs and diodes are equal to the output voltage, which is 400V in this research.

The diode current is half of the input current. Therefore, the peak current can be derived based on equation (2-12).

$$I_{D,\,peak} = I_{in,\,peak} = \frac{\sqrt{2}P_{in,\,\max}}{V_{in,\,\min}} = \frac{\sqrt{2}P_{o,\,\max}}{V_{in,\,\min}} = 52A \tag{2-12}$$

Assuming the power factor is 1, the diode current is a half sine wave, therefore, the RMS value can be calculated.

$$I_{D,\,RMS} = \frac{I_{in,\,peak}}{2} = 26A \tag{2-13}$$

For the currents flow through MOSFETs, due to the interleaved technology, the currents flow through the MOSFETs are half of the input current; therefore, the peak current is 26A.

Based on the calculations, the specific models for the components can be selected. Next, the control loop design for the system is presented.

2.4 Control Loop Design for Interleaved Totem-pole Bridgeless PFC

For the SiC based totem-pole interleaved bridgeless PFC, it can operate in CCM, CRM and DCM. Since the power of the system is relatively high, CCM operation is preferred. Power factor (PF) is defined as the ratio between AC input's real power and apparent power. Assuming input voltage is a perfect sine wave, PF can be defined as the product of current distortion and phase shift. The PFC control loop's tasks are:

(1) Control inductor current: The obligation is to make sure the shape of the input current is sinusoidal and in phase with the input voltage;

(2) Control output voltage: The obligation is to provide a constant DC output voltage for the next

stage.

The control scheme of the system is shown in Figure 2-17.

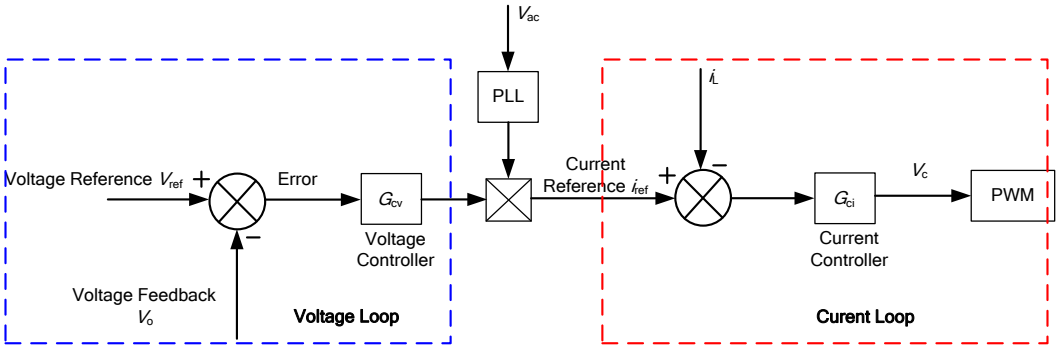


Figure 2-17 Control scheme of the system.

2.4.1 Current Loop Design

PI control is widely used and classical in industry control. In this application, both the voltage and current loops adopt PI regulator arithmetic. The small signal model of the current loop is shown in Figure 2-18.

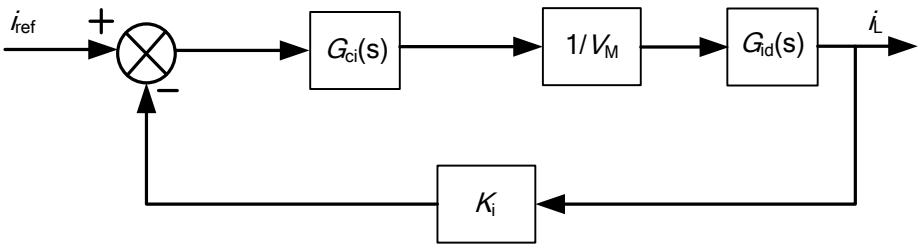


Figure 2-18 Small signal model of the current loop.

where $G_{ci}(s)$ is the current loop controller; $1/V_M$ represents the model of PWM; $G_{id}(s)$ is the duty-to-current transfer function; and K_i is sample ratio of the inductor current.

The system can be treated as a Boost converter, so the duty-to-output transfer function can be

expressed as

$$G_{id}(s)=\frac{V_o(2+R_LCs)}{LR_LCs^2+Ls+(1-D)^2R_L} \tag{2-14}$$

The bode diagrams of $G_{id}(s)$ for different duty cycles are shown in Figure 2-19. It can be seen that with different duty cycles, when frequency is above 500Hz, all curves are reduced to one. According to experience, the current loop is operating at frequencies above 1kHz, therefore, the transfer function can be further simplified.

$$G_{id}(s)=\frac{V_o}{Ls} \tag{2-15}$$

where $L=L_B/2$.

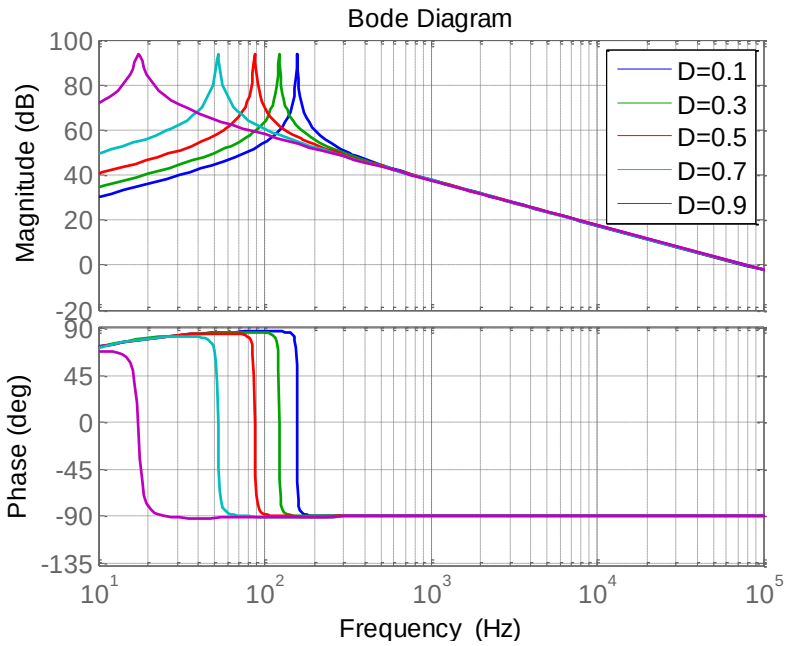


Figure 2-19 Bode diagrams of $G_{id}(s)$ for different duty cycles.

Therefore, the current loop gain without controller can be expressed as

$$T_i(s) = K_i \times \frac{1}{V_M} \times G_{id}(s) \tag{2-16}$$

Figure 2-20 shows the bode diagram of the open current loop gain. It can be seen that the bandwidth of the open current loop is about 35kHz. A PI controller $G_{ci}(s)$ is required to adjust the bandwidth. Generally, the bandwidth of the current loop is set to be 8-10kHz [17]. In this research, the bandwidth of the current loop is adjusted to 10kHz. And the PI controller is expressed as

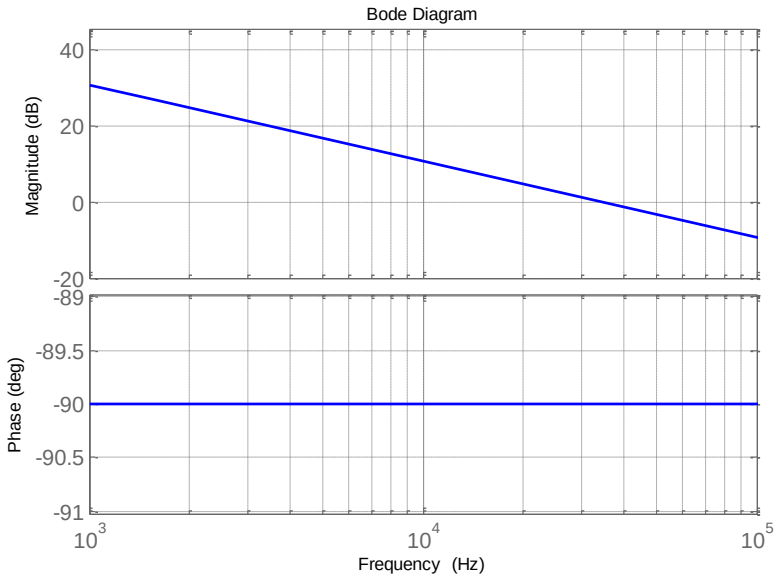


Figure 2-20 Bode diagram of the open current loop gain.

$$G_{ci}(s) = K_{Pi} + \frac{K_{Ii}}{s} \tag{2-17}$$

And the coefficients can be calculated according to the following equations.

$$K_{Pi} = \frac{L 2\pi f_{ci}}{K_i V_o} = 0.147 \tag{2-18}$$

$$K_{Ii} = K_{Pi} 2\pi f_{zi} = 921 \tag{2-19}$$

where f_{ci} is the frequency of the current loop bandwidth; f_{zi} is the frequency of the current

compensator zero; according to experience, f_{zi} is selected to be 3-10 times less than f_{ci}.

After adding PI controller, the bode diagram of the current loop is shown in Figure 2-21. It can be seen that the bandwidth is adjusted to around 10kHz.

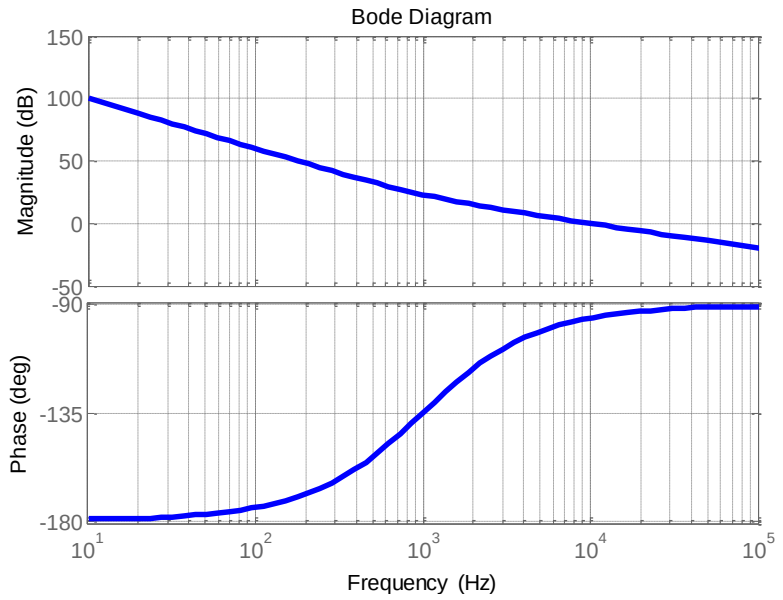


Figure 2-21 Bode diagram of the closed current loop gain.

2.4.2 Voltage Loop Design

To find the voltage loop transfer function, it is necessary to find the ratio v_{out}/v_c, where v_c is the output of voltage regulator. According to the control scheme

$$i_{ref} = i_{in} = i_L = k \cdot V_{in} \cdot V_c \tag{2-20}$$

By replacing the variables with their stationary components and small perturbations, one can obtain

$$I_{in} + \hat{i}_{in} = k \cdot (V_{in} + \hat{v}_{in}) \cdot (V_c + \hat{v}_c) \tag{2-21}$$

Ignore the second and higher orders of small signals,

$$\hat{i}_{in} = k \cdot V_{in} \cdot \hat{v}_c + k \cdot \hat{v}_{in} \cdot V_c \tag{2-22}$$

In order to get the voltage loop transfer function, the following assumption is accepted: the input power equals to the output power.

$$i_{in} \cdot V_{in} = i_o \cdot V_o \tag{2-23}$$

According to equation (2-20) and (2-23),

$$k \cdot V_c \cdot V_{in}^2 = i_o \cdot V_o \tag{2-24}$$

Similarly, by replacing the variables with their stationary components and small perturbations, we can obtain

$$k \cdot (\hat{v}_c + V_{c)} \cdot (\hat{v}_{in} + V_{in})^2 = (I_o + \hat{i}_o) \cdot (\hat{v}_o + V_o) \tag{2-25}$$

Ignore the high-orders of the small signals,

$$k \cdot \hat{v}_c \cdot V_{in}^2 + 2k \cdot V_{in} \cdot V_c \cdot \hat{v}_{in} = I_o \cdot \hat{v}_o + \hat{i}_o \cdot V_o \tag{2-26}$$

By rearranging equation (2-26), we can find the expression of i_o

$$\hat{i}_o = \frac{k \cdot \hat{v}_c \cdot V_{in}^2}{V_o} + \frac{2k \cdot V_{in} \cdot V_c \cdot \hat{v}_{in}}{V_o} - \frac{I_o \cdot \hat{v}_o}{V_o} \tag{2-27}$$

In order to simplify (2-27), we can make

$$g_c = \frac{k \cdot V_{in}^2}{V_o}, r_{out} = \frac{I_o}{V_o} \tag{2-28}$$

Since we only interest in the relation between v_o and v_c, the small signal v_{in} is set to be zero. Therefore, the small signal model for the voltage loop is shown in Figure 2-22. Thus, the control to output voltage transfer function can be expressed as.

$$\frac{\hat{v}_o}{\hat{v}_c} = g_c \cdot r_{out} // \frac{1}{Cs} // Z_L = g_c \frac{Z_L r_{out}}{Z_L + r_{out} + r_{out} \cdot Z_L Cs} \tag{2-29}$$

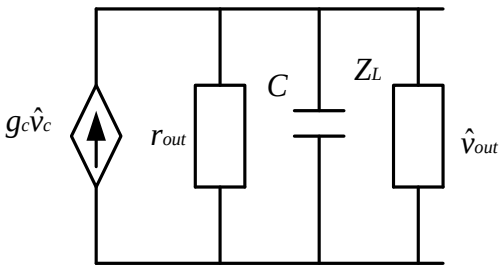


Figure 2-22 The small signal model of the voltage loop.

The load impedance can be presented in different variants. According to [18], if the PFC is connected to another converter, this variant is considered as a constant load power consumption, and the input impedance of the following converter is assumed to be the PFC output impedance. The transfer function of the voltage loop in this case is represented by

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_c} = g_c \frac{1}{Cs} \tag{2-30}$$

The voltage loop block diagram is shown in Fig. 2-23. The open loop gain can be expressed as

$$T_v(s) = K_v \times G_{vc}(s) \tag{2-31}$$

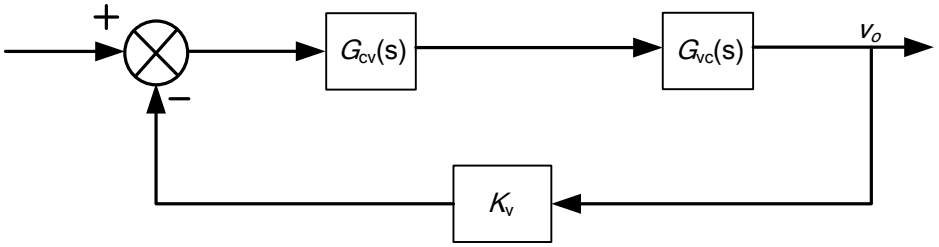


Figure 2-23 Block diagram of the voltage loop.

The bode diagram of the open loop gain is shown in Figure 2-24. It can be seen that the bandwidth of the voltage loop is 130Hz; in order to reduce the influence of line frequency, the bandwidth of the voltage loop is selected to be 10-20Hz. And the PI parameters for voltage controller can be

calculated according to the following equations.

$$K_{Pv} = \frac{VoC2\pi f_{cv}}{kK_v V_{in}^{\ 2}} = 8.1 \tag{2-32}$$

$$K_{Iv} = K_{Pv} 2\pi f_{zv} = 501 \tag{2-33}$$

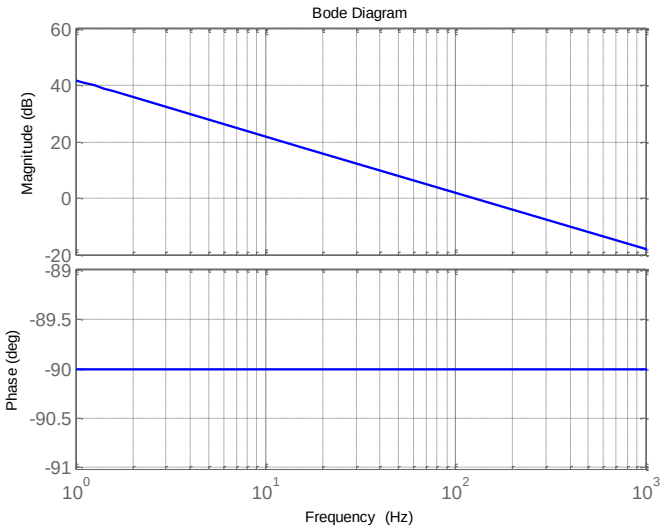


Figure 2-24 Bode diagram of the open voltage loop gain.

The bode diagram of the voltage loop with voltage controller is shown in Fig. 2-25. It can be seen that the bandwidth is adjusted to about 12Hz.

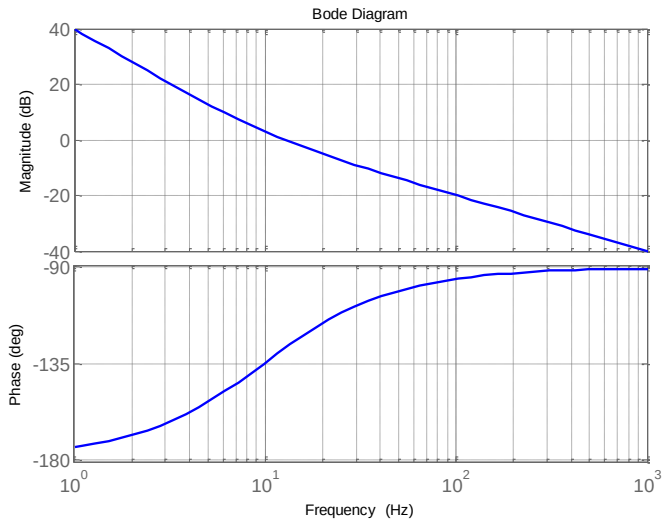


Figure 2-25 Bode diagram of the closed voltage loop gain.

2.5 Simulation Verification

In this part, the theoretical analysis is verified by implementing simulation on PSIM. The system parameters are shown in Table 2-3.

Table 2-3 Simulation parameters for interleaved totem-pole bridgeless PFC

Input voltage U_{in}	90V-264V
Boost inductor L_{B1}, L_{B2}	360uH
Output Capacitor C_B	1300uF
Switching frequency f_s	100kHz
Output voltage V_o	400V
Output power P_o	330W-3.3kW

Firstly, the operation principle of the interleaved totem-pole bridgeless PFC is verified. Figure 2-26 shows the simulation waveforms when input voltage is 110VRMS, while Figure 2-27 show the waveforms when input voltage is 220VRMS.

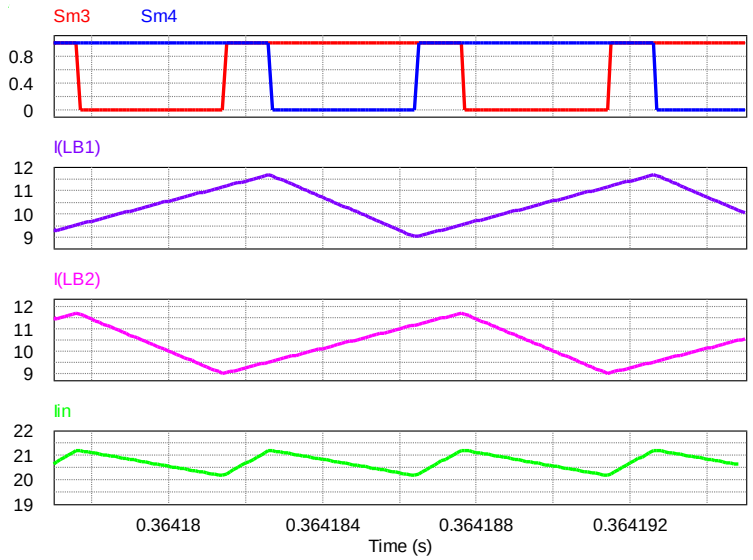


Figure 2-26 Simulation waveforms when input voltage is 110VRMS.

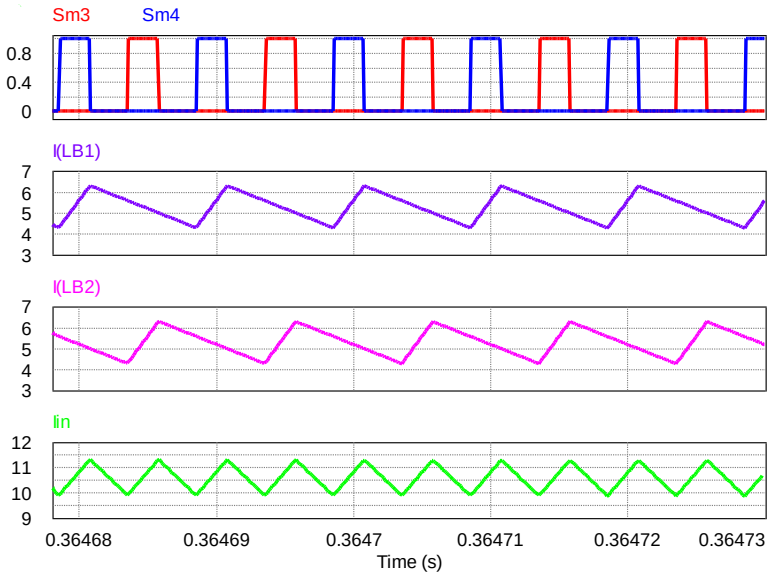
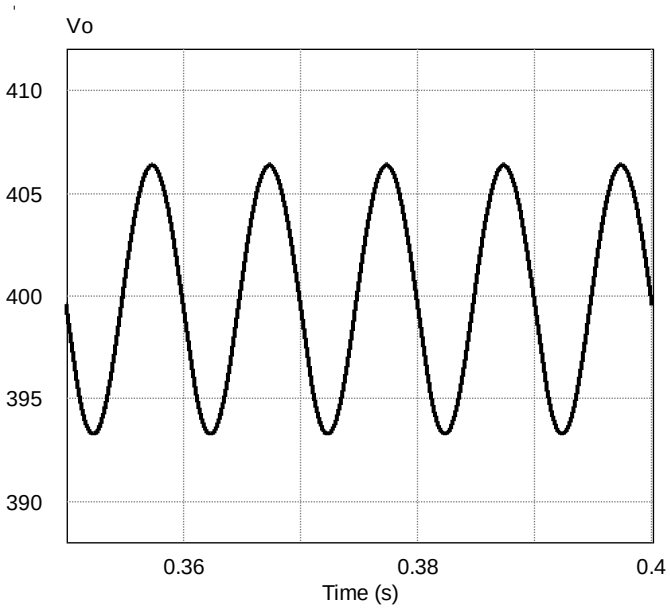
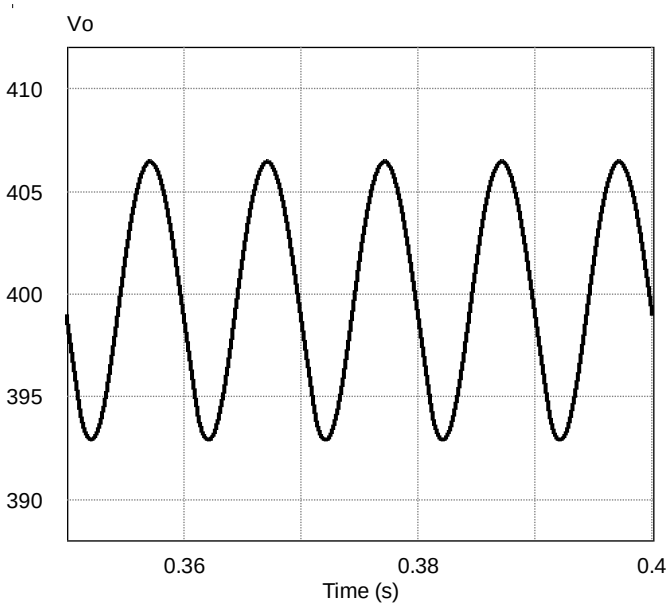


Figure 2-27 Simulation waveforms when input voltage is 220VRMS.

Figure 2-28 shows the waveform of output voltage.



(a)

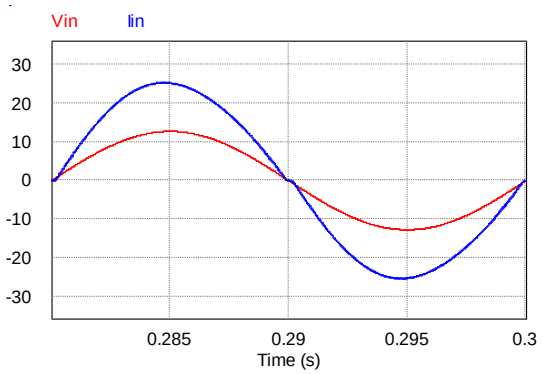


(b)

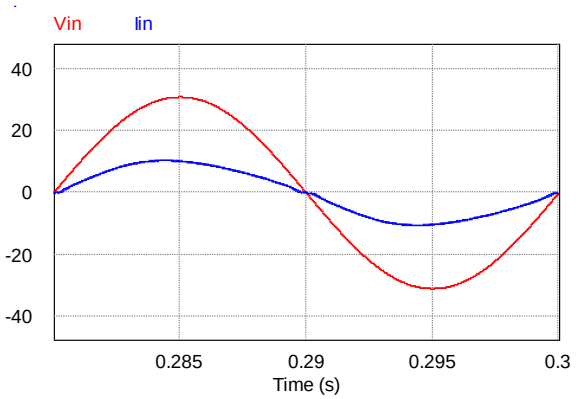
Figure 2-28 Simulation waveforms of the output voltage. (a) when input voltage is 110VRMS. (b) when input voltage is 220VRMS.

From Figure 2-26-2-28, it can be seen that both the inductor current and output voltage can meet the ripple requirements, which verifies the previous calculation.

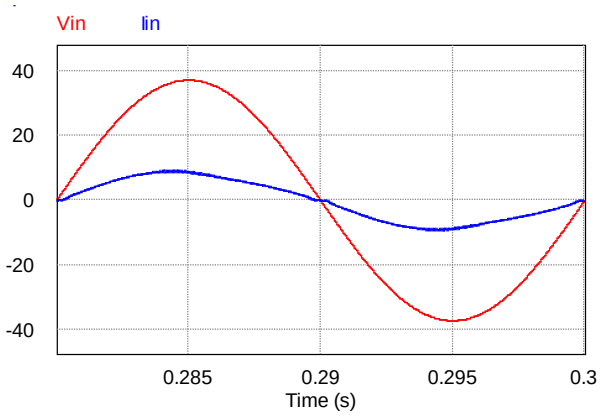
Next, the power factor function for different conditions are studied. Figure 2-29 shows the simulation results. The red line represents for input voltage (one tenth of the real value), the blue line represents for the input current. The power factor and THD information with different input voltage and output power are also given in Figure 2-30 and 2-31. It can be seen that power factor is greater than 0.98 under all conditions; in addition, THD of the input current is less than 5% at rated power.



(a)



(b)



(c)

Figure 2-29 Simulation waveforms of the input voltage and input current. (a) when input voltage is 90VRMS.

(b) when input voltage is 220VRMS. (c) when input voltage is 264VRMS.

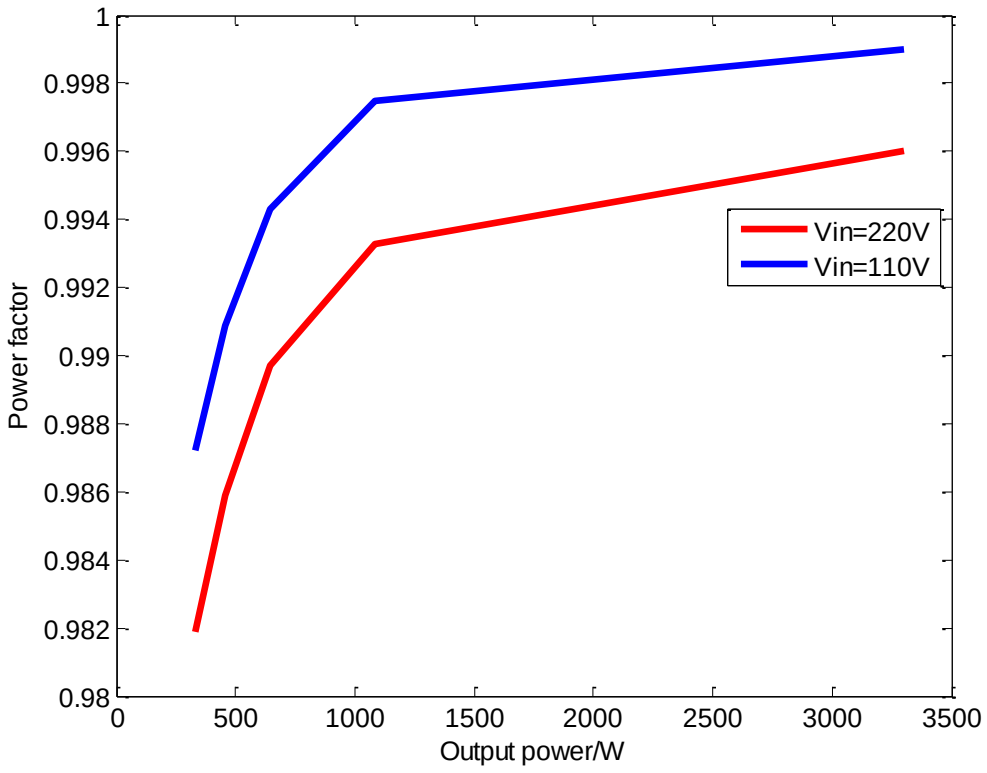


Figure 2-30 Power factor with different input voltage and output power.

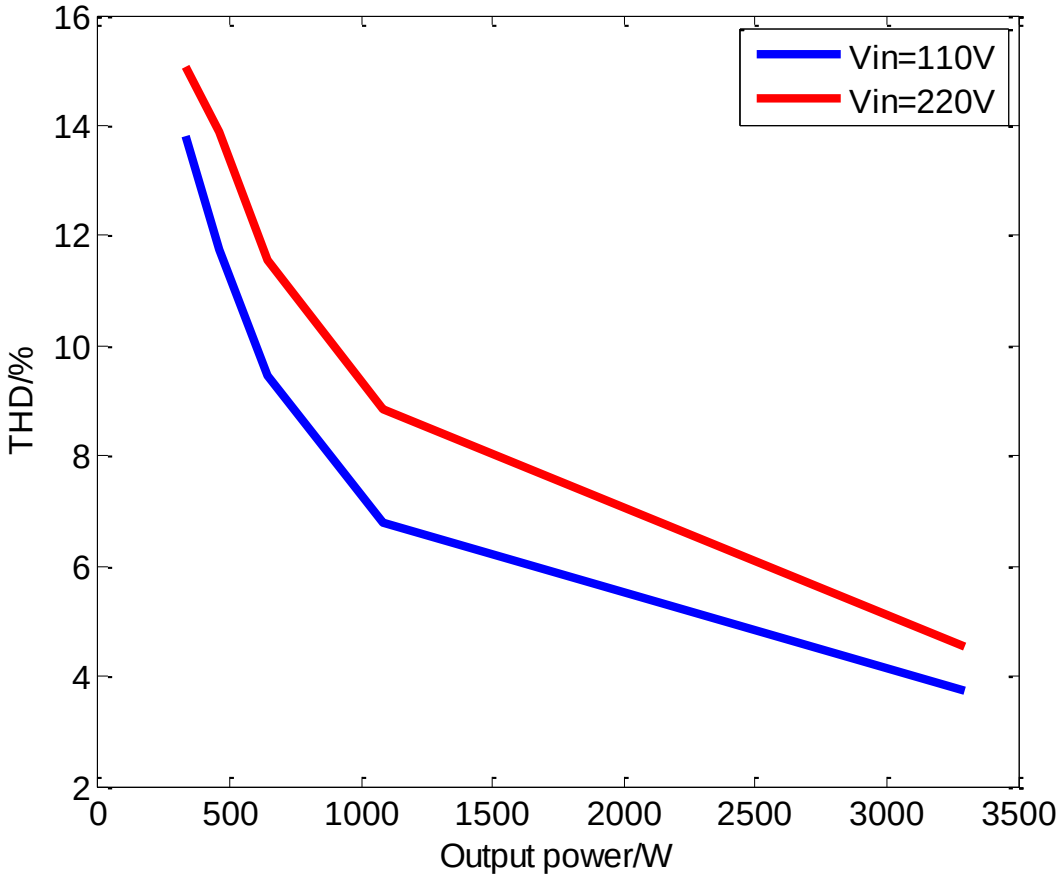


Figure 2-31 THD of input current with different input voltage and output power.

2.6 Summary

In this chapter, the power factor correction circuits are studied, including traditional Boost PFC, totem-pole bridgeless PFC and SiC based totem-pole interleaved bridgeless PFC. The comparison results between them are shown in Table 2-4.

Table 2-4 Comparison between three different PFC topologies.

Topology	Traditional Boost PFC	Totem-pole bridgeless PFC	SiC based Totem-pole interleaved bridgeless PFC
Slow Diode	4	2	2
MOSFET	1(Si)	2(Si)	4(SiC)
Fast Diode	1	0	0
Input Inductor	1	1	2
Output Capacitor	1	1	1
Semiconductors in Path	3	2	3
Efficiency	Low	High	Best
Operation Mode	CCM DCM CRM	DCM CRM	CCM CRM DCM

Chapter 3 Full-bridge LLC Resonant DC/DC Converter

For the safety requirement of the battery charger, an isolated DC/DC converter topology, which can provide electrical isolation between the primary and secondary side is required. Among different kinds of DC/DC converters, the LLC resonant converters have drawn much attention because of their ability to achieve zero voltage switching (ZVS) for primary switches and zero current switching (ZCS) for secondary rectifier diodes. In this chapter, the operation principles, modeling and characteristics of a full-bridge LLC resonant converter are discussed.

3.1 Operation Principles of Full-bridge LLC Resonant Converter

Compared with the half-bridge topology, the power rating of the full-bridge configuration is higher. In this research, the full-bridge LLC resonant converter is selected. The topology is shown in Figure 3-1. In Figure 3-1, S_1-S_4 are the primary switches, D_1-D_4 are their corresponding body diodes, while C_1-C_4 are their corresponding junction capacitors. The resonant components include L_r, C_r and L_m (which is also the magnetic inductance of the transformer). D_{s1}-D_{s4} form a diode bridge rectifier; in addition, C_o is the output capacitor and R_L is the load. There exist two resonant frequencies, one is the resonant frequency f_r between L_r and C_r; another one is the resonant frequency f_m between L_r, C_r and L_m. And their expressions are shown below.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3-1}$$

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{3-2}$$

According to the relationship between switching frequency f_s and resonant frequency f_r, there are mainly three operation modes.

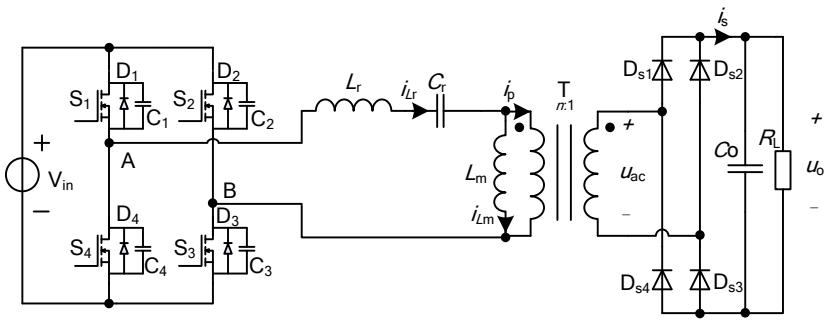


Figure 3-1 Full-bridge LLC resonant converter.

Mode 1: $f_s<f_r$. The main waveforms are shown in Figure 3-2. In this mode, when the resonant current i_{Lr} equals to magnetic current i_{Lm}, the magnetic inductor L_m begins to resonant with L_r and C_r. During this stage, since the resonant current and magnetic current are same, the secondary side current equals to zero. Therefore, the rectifier diodes on the secondary side can achieve ZCS, and the output current is discontinuous.

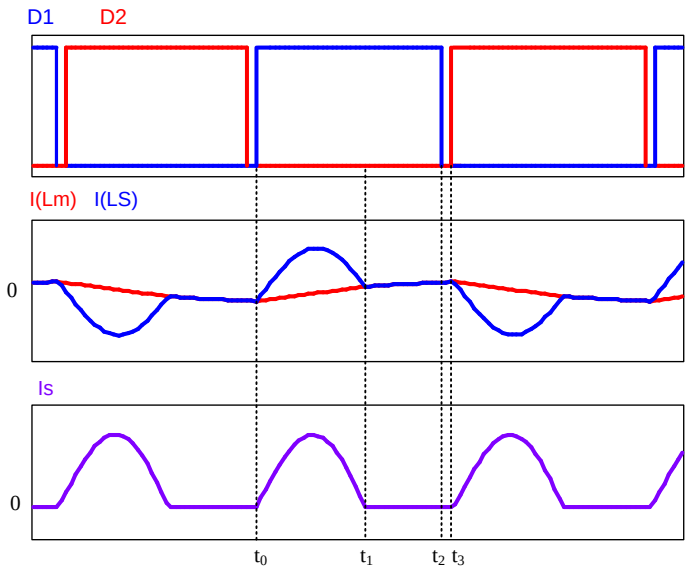


Figure 3-2 Theoretical waveforms in mode 1.

Mode 2: f_s=f_r. The main waveforms are shown in Fig. 3-3. In this mode, the magnetic inductor L_m does not resonant with L_r and C_r, and the voltage across the magnetic inductor is clamped by output voltage. In addition, the output current is in critical conduction mode, and it can achieve ZCS.

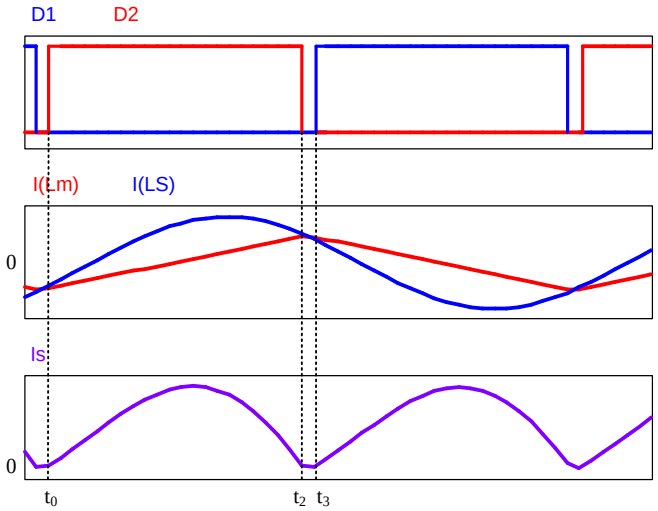


Figure 3-3 Theoretical waveforms in mode 2.

Mode 3: f_s>f_r. The main waveforms are shown in Figure 3-4. In this mode, L_m does not resonant with L_r and C_r, and the output current is continuous, it cannot achieve ZCS.

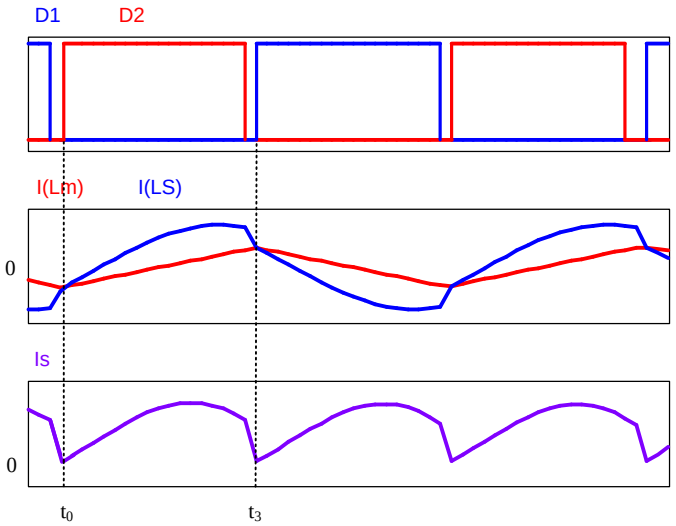


Figure 3-4 Theoretical waveforms in mode 3.

Since mode 1 contains all the stages of other modes, it is selected to be analyzed. In addition, only half cycle will be discussed because of its symmetric characteristic.

Stage 1 [t_0-t_1]: At this stage, the drive signals for S_1 and S_3 are enabled, the equivalent circuit is shown in Figure 3-5. The voltage across point A and B equals to input voltage, i_{Lr} and i_{Lm} begin to increase, since L_r is smaller than L_m, i_{Lr} is greater than i_{Lm}, and the difference between i_{Lr} and i_{Lm} goes to the secondary side of the transformer. In addition, the voltage across the magnetic inductor L_m is clamped by the output voltage, so i_{Lm} can be expressed as

$$nV_o = L_m \frac{di_{Lm}}{dt} \tag{3-3}$$

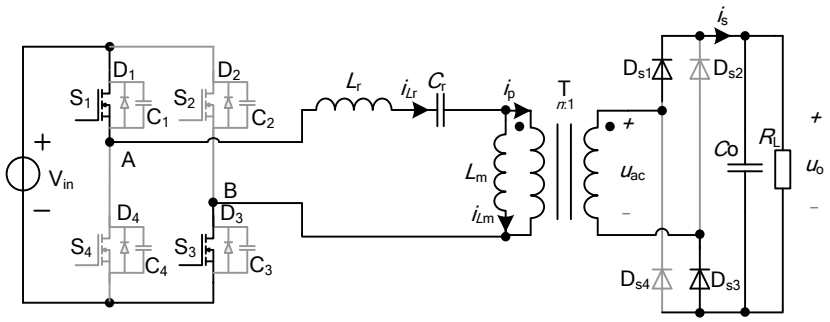


Figure 3-5 The equivalent circuit in stage 1.

Stage 2[t_1-t_2]: The equivalent circuit is shown in Figure 3-6. At t_1, i_{Lm} equals to i_{Lr}, so there is no current flow into the primary and secondary side of the transformer, and the currents flow through diode D_{s1} and D_{s4} decrease to zero at t_1, which achieve ZCS turn off and no reverse recovery problems. From t_1 to t_2, L_m resonant with L_r and C_r.

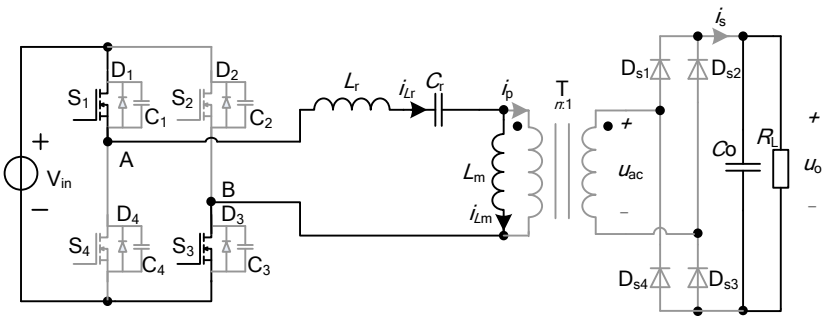


Figure 3-6 The equivalent circuit in stage 2.

Stage 3[t_2-t_3]: During this stage, the equivalent circuit is shown in Figure 3-7. This stage is also known as the dead time. All switches are OFF, capacitors C_2 and C_3 are discharging, while C_1 and C_4 are charging. When C_2 and C_3 are fully discharged before their drive signals coming, they can achieve ZVS turn on.

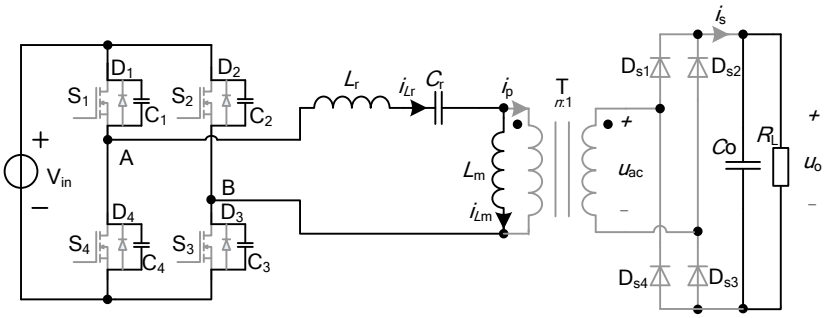


Figure 3-7 The equivalent circuit in stage 3.

3.2 Analysis and Modeling of LLC Resonant Converter

In this part, fundamental harmonic analysis (FHA) method is adopted to obtain the model of the full-bridge LLC resonant converter; meanwhile, the DC voltage gain, constant output voltage characteristic, and constant output current characteristic are discussed.

3.2.1 Fundamental Harmonic Analysis

In order to improve the efficiency of the LLC converter, the operating point should be near the resonant frequency. Therefore, the fundamental harmonic analysis (FHA) method can be adopted to analyze the converter approximately. It assumes that only fundamental frequency can transfer energy, so the LLC resonant converter can be simplified as a linear circuit. In this part, the FHA method is adopted to analyze the full-bridge LLC resonant converter [19]-[21].

The topology of the full-bridge LLC resonant converter is shown in Figure 3-8. Obviously, it can be divided into three parts, namely, switch network, resonant network and rectifier and filter network. And the switch network and rectifier and filter network can be simplified by adopting FHA.

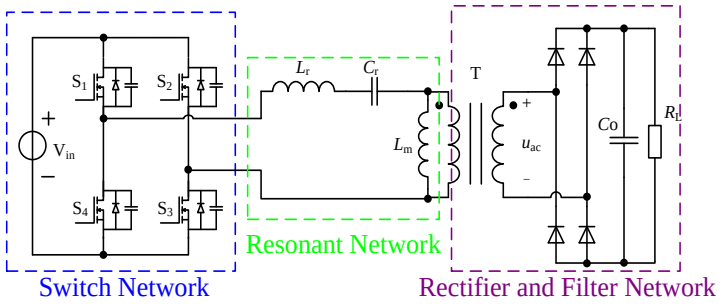


Figure 3-8 The topology of the full-bridge LLC resonant converter.

Firstly, the simplification of the switch network is discussed.

The drive signals for S_1 and S_3, S_2 and S_4 are 180 degrees out of phase. Ignore the turn-on and turn-off processes of switches, when the switch pair S_1 and S_3 are ON, the voltage across point A and B is V_{in}; when the switch pair S_2 and S_4 are ON, the voltage becomes $-V_{in}$. Therefore, the input voltage for the resonant network is a square wave as shown in Figure 3-9.

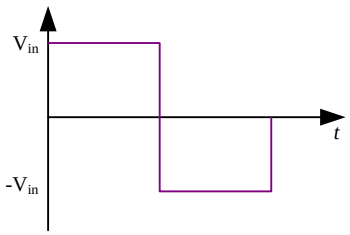


Figure 3-9 Input voltage of the resonant network.

By doing the Fourier analysis for the voltage across point A and B, we can obtain

$$v_{AB}(t) = V_{in} + \frac{4V_{in}}{\pi} \sum_{n=1,2,3...} \frac{1}{n} \sin(nw_s t) \tag{3-4}$$

where $w_s = 2\pi f_s$.

It can be seen that v_{AB} includes DC term and AC terms. According to (3-4), the fundamental harmonic of v_{AB} is shown in Figure 3-10, and it can be expressed as

$$v_{AB1}(t) = \frac{4V_{in}}{\pi} \sin(w_s t) = \sqrt{2} V_{AB1} \sin(w_s t) \tag{3-5}$$

where V_{AB1} is the effective value, which equals to

$$V_{AB1} = \frac{2\sqrt{2}V_{in}}{\pi} \tag{3-6}$$

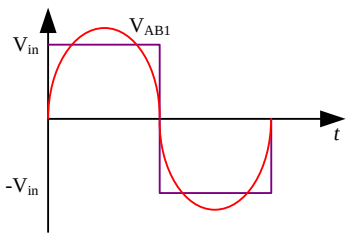


Figure 3-10 Fundamental harmonic of the input voltage of the resonant network

Therefore, the switch network can be simplified as an AC voltage source. Next, the simplification of the rectifier and filter network is discussed.

When the switching frequency is adjacent to the resonant frequency f_r, the primary side current i_p of the transformer can be treated as a sine wave, which can be expressed as

$$i_p = \sqrt{2} I_{p1} \sin(w_s t - \varphi) \tag{3-7}$$

where φ is the phase shift between i_p and V_{AB}, I_{p1} is the effective value of i_p.

According to Figure 3-8, when i_p is positive, the primary side voltage is clamped by nV_o, $i_s = ni_p$; when i_p is negative, the primary side voltage is clamped by $-nV_o$, $i_s = -ni_p$. After the capacitor, a relatively constant DC current is obtained, that is

$$I_o = \frac{1}{T_s}\int_0^{T_s} n\left|i_p(t)\right|dt = \frac{2n}{T_s}\int_0^{\frac{T_s}{2}} \left|\sqrt{2} I_{p1} \sin(w_s t - \varphi)\right| dt = \frac{2\sqrt{2}n}{\pi} I_{p1} \tag{3-8}$$

So, I_{p1} equals to

$$I_{p1} = \frac{\pi}{2\sqrt{2}n} I_o \tag{3-9}$$

By substituting (3-9) to (3-7),

$$i_p(t) = \frac{\pi}{2n} I_o \sin(w_s t - \varphi) \tag{3-10}$$

By doing Fourier analysis for the primary voltage,

$$v_p(t) = \frac{4nV_o}{\pi} \sum_{n=1,3,5\ldots} \frac{1}{n} \sin(n w_s t) \tag{3-11}$$

The fundamental component can be expressed as

$$v_{p1}(t) = \frac{4nV_o}{\pi} \sin(w_s t - \varphi) = \sqrt{2} V_{p1} \sin(w_s t - \varphi) \tag{3-12}$$

Where V_{p1} is the effective value of the fundamental component, which equals to

$$V_{p1} = \frac{2\sqrt{2}nV_o}{\pi} \tag{3-13}$$

From (3-9) and (3-13), we can see that the fundamental harmonic of the primary side current and voltage are in phase with each other, which means the rectifier and filter network can be regarded as an AC equivalent resistor.

$$R_{ac} = \frac{V_{p1}}{I_{p1}} = (\frac{2\sqrt{2}n}{\pi})^2 \frac{V_o}{I_o} = \frac{8n^2}{\pi^2} R_L \tag{3-14}$$

Based on the above analysis, the full-bridge LLC resonant converter can be treated as a linear circuit shown below.

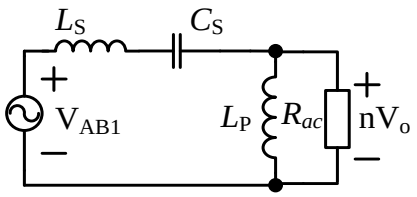


Figure 3-11 Simplified linear circuit model for the full-bridge LLC resonant converter.

3.2.2 Voltage Gain

According to the simplified circuit model, the transfer function of the full-bridge LLC resonant converter can be expressed as

$$H(s) = \frac{nV_o}{V_{AB1}} = \frac{jw_sL_m // R_{ac}}{jw_sL_r + 1/ jw_sC_r + jw_sL_m // R_{ac}} \tag{3-15}$$

Assume the voltage gain of the full-bridge LLC resonant converter is

$$M = \frac{nV_o}{V_{in}} = \frac{\pi V_{p1} / 2\sqrt{2}}{\pi V_{AB1} / 2\sqrt{2}} \tag{3-16}$$

Therefore, by getting the magnitude of $H(s)$, we can obtain the voltage gain.

$$M = \left\| H(jw_s) \right\| = \frac{nV_o}{V_{AB1}} = \left\| \frac{jw_s L_m // R_{ac}}{jw_s L_r + 1/ jw_s C_r + jw_s L_m // R_{ac}} \right\| \tag{3-17}$$

Here, we make some definitions, that is,

$$\lambda = L_m / L_r \tag{3-18}$$

$$Q = \sqrt{L_r / C_r} / R_{ac} \tag{3-19}$$

Finally, we can get the expression of the voltage gain.

$$M = \frac{1}{\sqrt{\left[(1 - \frac{1}{(f_s^*)^2}) Q f_s^* \right]^2 + \left[(1 - \frac{1}{(f_s^*)^2}) \frac{1}{\lambda} + 1 \right]^2}} \tag{3-20}$$

where f_s^* is the normalized frequency, it equals to f_s / f_r.

The equivalent input impedance of the resonant work can be expressed as

$$Z = jw_s L_r + 1/ jw_s C_r + jw_s L_m // R_{ac} \tag{3-21}$$

By substituting (3-18) and (3-19) into (3-21), we can obtain

$$Z = \frac{R_{ac}}{\lambda^2 (f_s^*)^3 + \frac{f_s^*}{Q^2}} \left\{ \lambda^2 (f_s^*)^3 + j \left[\frac{1}{Q} (f_s^*)^3 (1 + \lambda) - \frac{1}{Q} - \lambda^2 Q (1 - (f_s^*)^2)(f_s^*)^2 \right] \right\} \tag{3-22}$$

From (3-22), we can easily get the relation between Q and f_s when the input impedance is resistive, where the imaginary part of the input impedance equals to zero.

$$Q_{res} = \frac{1}{\lambda f_s^*} \sqrt{\frac{(1 + \lambda)(f_s^*)^2 - 1}{1 - (f_s^*)^2}} \tag{3-23}$$

By substituting (3-23) into (3-20), we can derive the voltage gain when the input impedance is resistive.

$$M(f_s^*)_{res} = \frac{1}{\sqrt{\frac{1}{\lambda}(1-\frac{1}{(f_s^*)^2})+1}} \tag{3-24}$$

When L_r is settled, the larger lambda means larger L_m, which will decrease the magnetic current, then the losses will be decreased, or the efficiency will be increased; however, L_m cannot be very large, since its value should make sure that the switches can operate in ZVS region; so, a reasonable value for lambda is required. Here, lambda is set to be 10.

In addition, according to the resistive voltage gain curve, LLC resonant converter is divided into two regions, namely ZVS and ZCS. When converter operating in the left hand of this curve, the input impedance of this network is capacitive, and the switches can achieve ZCS; when converter operating in the right hand of this curve, the input impedance network is inductive, and the switches can achieve ZVS. It can be seen from Figure 3-12, the resistive voltage gain curve and line f_s^*=1 divide the whole area into three regions, namely, region 1, 2, and 3.

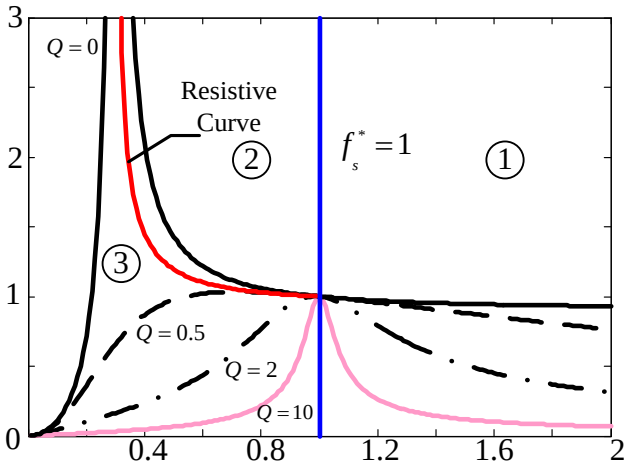


Figure 3-12 The DC voltage gain curve of the LLC resonant converter.

Region 1: At the right hand of both curves. In this region, the voltage gain is lower than 1, the input

impedance is inductive and the switches can achieve ZVS, the diodes at the secondary side are hard switching;

Region 2: At the right hand of the resistive curve and the left hand of line $f_s^*=1$. In this region, the voltage gain is higher than 1, the input impedance is inductive and the switches can achieve ZVS, the rectifier diodes can achieve ZCS;

Region 3: At the left hand of both curves. In this region, the voltage gain can be higher or lower than 1, the input impedance is capacitive and the switches can achieve ZCS, the rectifier diodes can achieve ZCS.

It is well known that, for higher frequency operation, MOSFET is more advantageous. For MOSFETs, it is suitable to work under ZVS condition. The general purpose of the parameter design is to make sure the converter is operating in Region 2.

3.3 Constant Output Voltage Characteristic

When the switching frequency is equal to f_r, the output voltage is independent of the load. According to Figure 3-11, by using the voltage divider law, the output voltage equals to

$$V_o(s) = n\frac{\frac{R_{ac}L_m s}{R_{ac}+L_m s}V_{in}}{\frac{R_{ac}L_m s}{R_{ac}+L_m s}+L_r s+\frac{1}{C_r s}} \tag{3-25}$$

By simplifying (3-25), we can obtain

$$V_o(s) = n\frac{V_{in}}{1+\frac{L_r s+\frac{1}{C_r s}}{L_m s}+\frac{1}{R_{ac}}(L_r s+\frac{1}{C_r s})} \tag{3-26}$$

Since in this situation, the resonant components are L_r and C_r, the sum of $L_r s+1/C_r s=0$, finally, (3-

26) can be rewritten as

$$V_o(s) = nV_{in} \tag{3-27}$$

The output voltage only depends on the turns ration and input voltage, and it is independent of the load.

3.4 Constant Output Current Characteristic

Simply, equation (3-26) divided by R_{ac} (the turns ration should be taken into account), which equals to the output current.

$$I_o(s) = \frac{V_o(s)}{Rac} = \frac{1}{n} \frac{V_{in}}{R_{ac}(1 + \frac{L_r s + \frac{1}{C_r s}}{L_m s}) + L_r s + \frac{1}{C_r s}} \tag{3-28}$$

When the converter is operating at the lower resonant frequency f_m, the resonant components are L_r, C_r and L_m, the term associated with R_{ac} in equation (3-28) equals to zero, which means the output current is independent of the load.

3.5 Simulation Verification

In this part, a simulation case is presented to verify the theoretical analysis. The simulation parameters are shown in Table 3-1.

Table 3-1 Simulation parameters for full-bridge LLC resonant converter.

Input voltage U_{in}/V	400
Resonant inductor $L_{r/}$uH	35
Resonant capacitor C_r/nF	10
Magnetizing inductance L_m/uH	350
Lower resonant frequency f_r/kHz	269
Higher resonant frequency f_m/kHz	81
Output capacitor C_o/uF	200
Junction capacitor C_1-C_4/pF	20
Dead time t_{dead}/ns	70
Turns ration	2:1

Firstly, the ZVS operation for the primary switches and ZCS operation for the rectifier diodes in region 2 are verified. The switching frequency is 268kHz, which is marginally less than the resonant frequency f_r. Figure 3-13 shows the simulation waveforms in this case, which are consist with the theoretical analysis. The secondary current is in CRM. Therefore, the ZCS operation is achieved for the diodes.

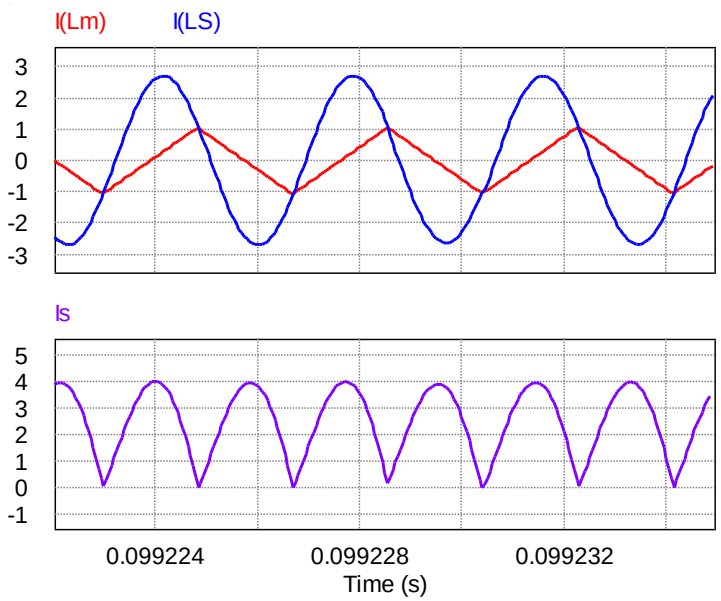


Figure 3-13 Simulation waveforms.

Figure 3-14 shows the detail of the voltage across the switch and its corresponding drive signal. It can be seen that before its drive signal coming, the voltage across the switch has already decreased to zero, the ZVS operation is achieved.

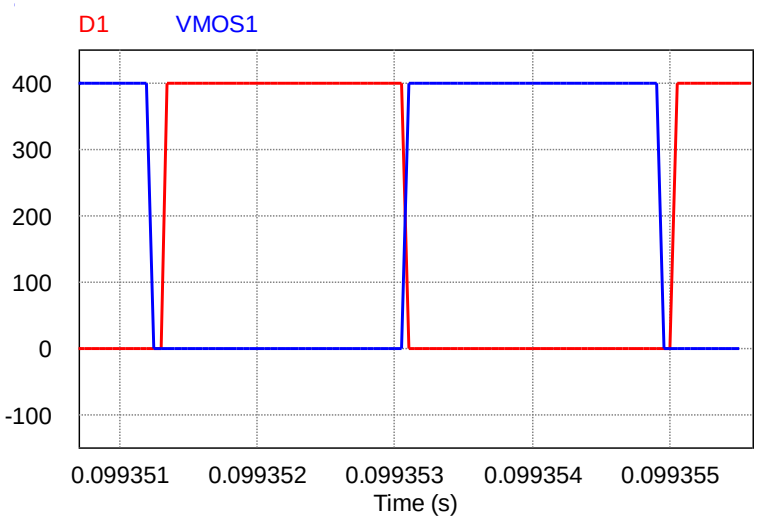


Figure 3-14 Simulation waveforms of the voltage across the switch and its corresponding drive signal.

Next, the constant output voltage and constant output current characteristics are verified. When

the switching frequency equals to 269kHz, according to the previous analysis, the output voltage should independent of the load. In simulation, the load is increased from 50ohm to 500ohm, and the increase step is 100ohm. The simulation results are shown in Figure 3-15.

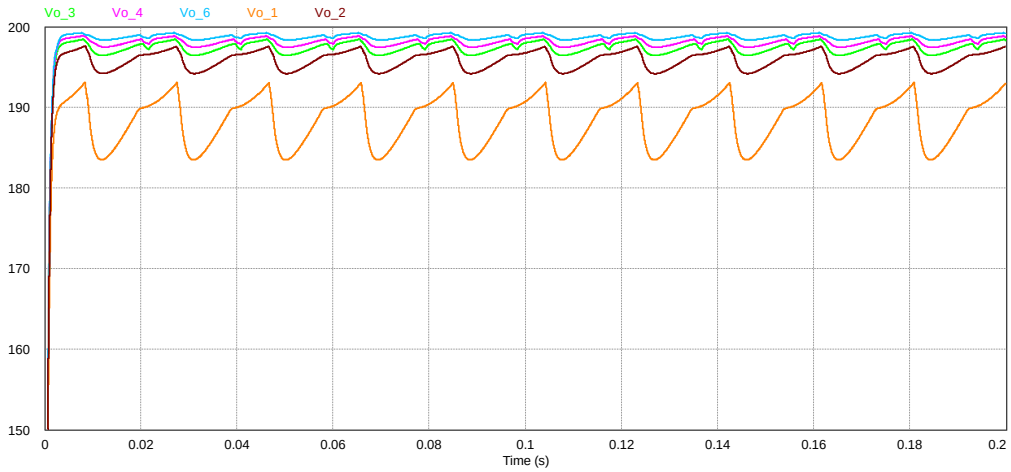


Figure 3-15 Simulation waveforms of the output voltage with different loads.

It can be seen that with the increase of load resistance, the output voltage almost remains constant. When the switching frequency equals to 81kHz, the output current should independent of the load. In simulation, the load resistance is changed from 30ohm to 50ohm. According to (3-28), the bode diagram of $I_o(s)$ shown in Figure 3-16 can be obtained by using Matlab. As we can see from the bode diagram, when the switching frequency is 81kHz, the magnitude is 13dB, so in this situation, the output current should be equal to 4.47A. The simulation results are shown in Figure 3-17.

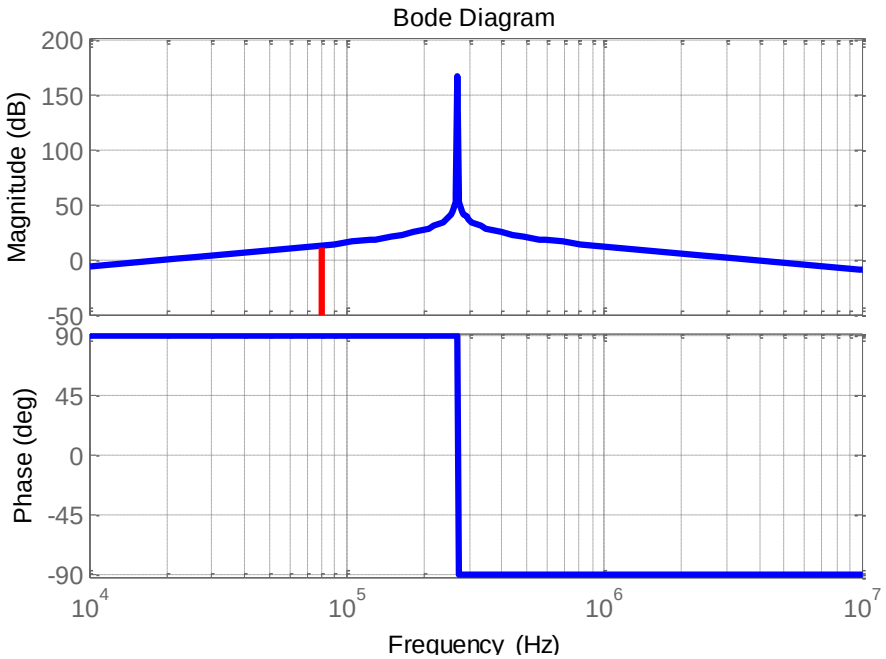


Figure 3-16 Bode diagram of the output current transfer function

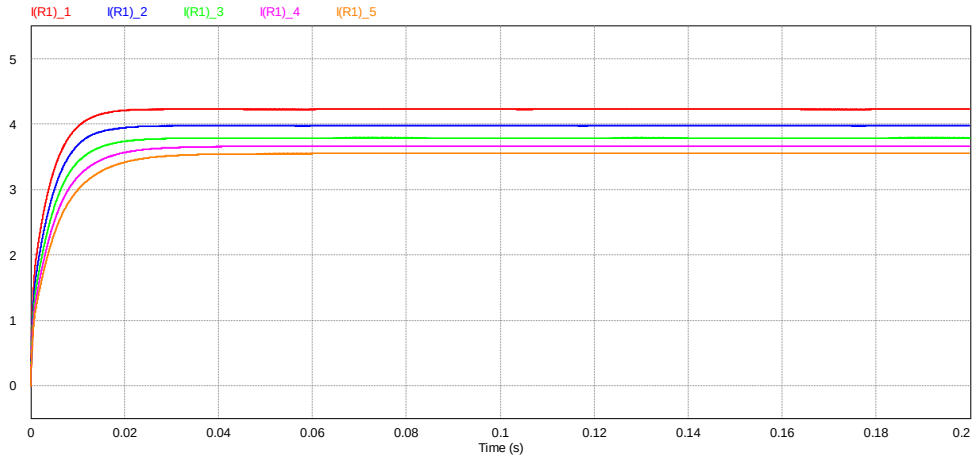


Figure 3-17 Simulation waveforms of the output current with different loads.

It can be seen that the output current is in an acceptable range with different loads.

3.6 Summary

In this chapter, the operation principles, modeling, DC voltage gain, constant output voltage characteristic, and constant output current characteristic are discussed. By designing the LLC converter to make sure it operates in region 2, the system can achieve ZVS operation for the switches, and ZCS operation for the diodes. Therefore, the efficiency of the system can be improved. Finally, a simulation case is discussed to verify the theoretical analysis, and the simulation results agree with the theoretical analysis.

Chapter 4 A High Frequency, High Efficiency, High Power Factor Isolated On-Board Battery Charger for Electric Vehicles

In this chapter, a high frequency, high efficiency, high power factor isolated on-board battery charger is proposed based on the previous analysis. Firstly, the battery charging profile is discussed, which clarifies the requirements for the battery charger; next, the topology of the battery charger is proposed and analyzed; then, the design considerations for the proposed topology are presented. In addition, the theoretical analysis is verified by simulations and finally, a summary is drawn.

4.1 Battery Charging Profile

In this research, the Li-ion battery cells are selected. The information for an individual Li-ion battery cell is shown in Table 4-1.

Table 4-1 Specifications for a Li-ion battery cell.

Nominal voltage/V	3.7
Discharging current/mA	10C5A
Nominal capacity/Ah	10
Internal impedance/mOhm	<7
Discharge cut-off voltage/V	2.75
Charging current(standard)	2A
Charging current(fast)	10A

Charging voltage(max)/V	4.20
Charging mode	CC/CV

According to the specifications, its charging profile can be drawn. In this research, a battery pack contains 100 series connected battery cells is considered. The specifications for the battery pack are shown in Table 4-2.

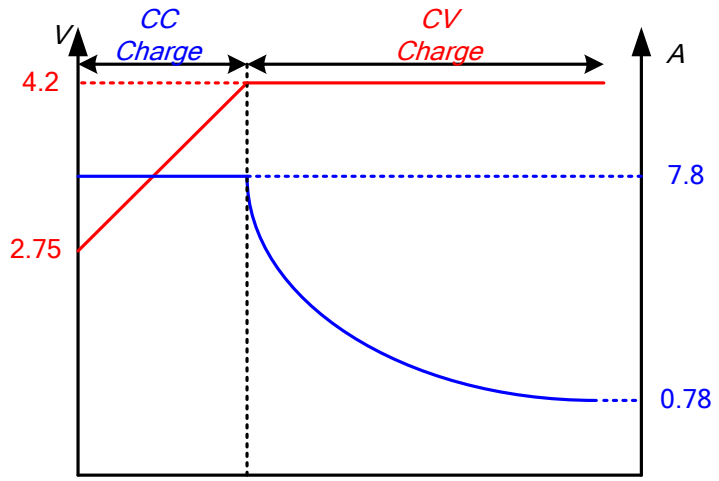


Figure 4-1 Charging profile of a Li-on battery cell.

Table 4-2 Specifications for the Li-ion battery pack.

Nominal voltage/V	370
Maximum charging voltage/V	420
Minimum charging voltage/V	275
Maximum charging current/A	7.8
Minimum charging current/A	0.78

Based on the specifications, the required output power of the battery charger ranges from 330W-3300W.

4.2 Proposed On-board Battery Charger

Recently, many topologies have been proposed for battery charger [22]-[27]. In [23] and [24], wireless battery charger topologies based on LLC resonant converters are proposed. In [25], by selecting the transformer turns ratio as a variable, a high efficiency battery charger topology is proposed. In [26], a bidirectional battery charger topology is proposed for V2G and G2V operation. In this research, a unidirectional, high frequency, high efficiency, high power factor battery charger is proposed.

According to the above analysis, the maximum power is calculated as 3.3kW. And the output voltage ranges from 275V to 420 V. The power rating is the reason why full-bridge LLC resonant converter is selected instead of half-bridge LLC resonant converter. In order to further improve the power handling ability, two LLC resonant converters are adopted; specifically, their inputs are in parallel by sharing the same full-bridge inverter and the outputs are connected in series, which can reduce the voltage stress of the rectifier diodes on the secondary side. And the topology is proposed based on [22]. Combining with the interleaved totem-pole bridgeless PFC circuit, we can obtain the final topology of the proposed high frequency, high efficiency, high power factor isolated on-board battery charger. It is a typical two-stage battery charger configuration. The first stage is AC/DC converter whose function mainly includes two parts, namely, providing unity power factor and constant output voltage for the next stage. The second stage is an isolated DC/DC converter, which is aimed to provide required charge voltage and current for the battery pack.

Compared with one full-bridge LLC resonant converter, the proposed topology has the following

advantages: 1) The current stress for the resonant network is reduced under the same power level due to its parallel connection; 2) the voltage stress on the secondary rectifier diodes is reduced due to its series connection; 3) the system efficiency is improved. A brief efficiency calculation example is shown below. In order to make it obvious, the following assumptions are made: 1) the output power is the same for both topologies; 2) in the proposed topology, assuming the power is evenly shared between two converters; 3) when the operating frequency is at the resonant frequency the system efficiency is 98%; otherwise, the system efficiency is 95%. 4) for the proposed topology, one of the LLC resonant converters is operating at the resonant frequency, another one is working at a wide range frequency in order to achieve closed loop control, which is the same for the topology only contains one LLC resonant converter.

Based on the assumptions, the efficiency for the topology only contains one LLC resonant converter is

$$\eta_1 = 95\% \tag{4-1}$$

And the efficiency for the proposed topology is

$$\eta_1 = \frac{95\% + 98\%}{2} = 96.5\% \tag{4-2}$$

Therefore, for the proposed topology, the efficiency is improved.

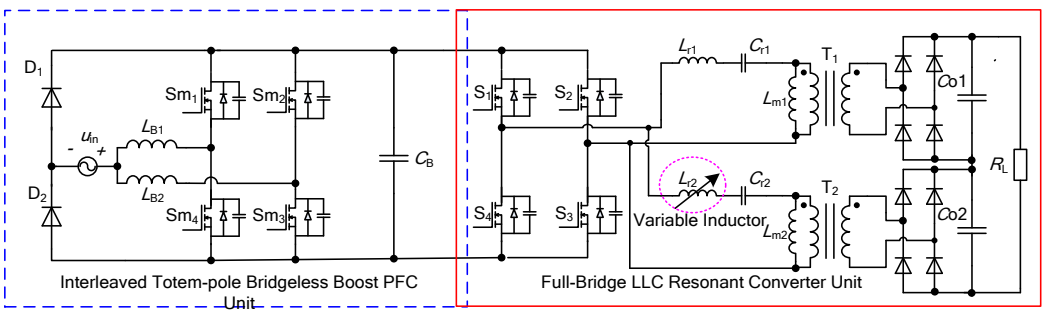


Figure 4-2 Proposed topology for the electric vehicle battery charger application.

Compared with the topology presented in [22], constant frequency operation can be provided by using magnetic control; in addition, the control scheme is simplified by eliminating a switch and capacitor; besides, in this research, two-stage system is analyzed instead of only analyzing the DC/DC converter unit.

4.3 Design Considerations for The Proposed Topology

The design guidelines for the interleaved totem-pole bridgeless PFC have been discussed in Chapter 2. Therefore, in this part, only the design considerations for the LLC resonant converters are presented. Recently, many publications focus on the design of LLC resonant converters [27]-[32]. However, unlike the proposed design methodologies, in this research, two LLC resonant converters instead of one are adopted. Therefore, some modifications should be made when comparing with the design methodologies already existed.

Firstly, the charging profile for the two LLC resonant converters are shown in Figure 4-3; in addition, the power distributions of two LLC resonant converters are shown in Figure 4-4.

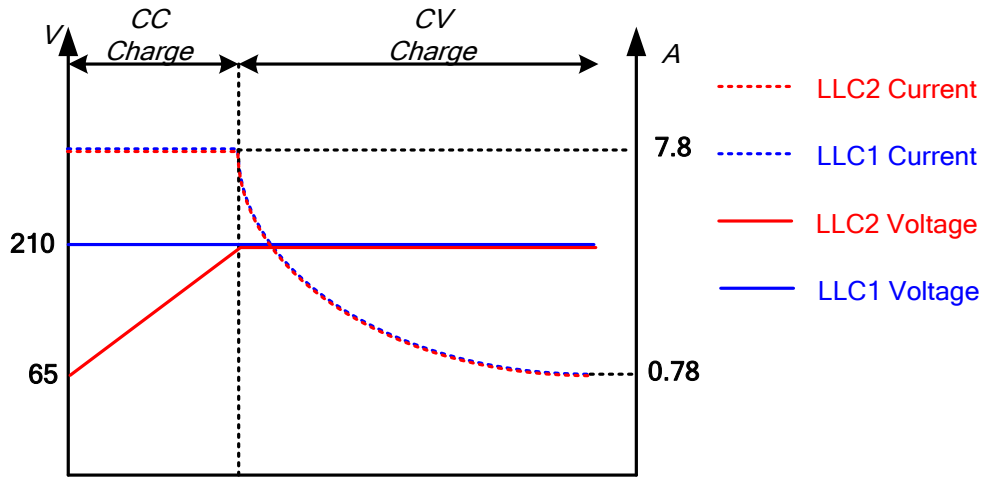


Figure 4-3 Charging profile of LLC1 and LLC2.

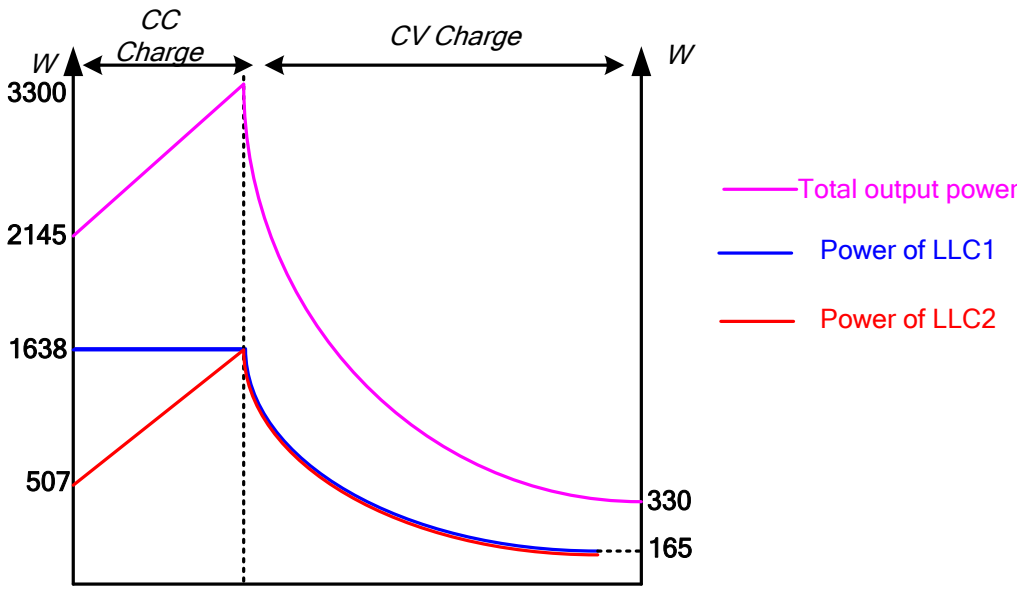


Figure 4-4 Output power for LLC1 and LLC2.

Based on the charging profile, for LLC1, it is operating at the resonant frequency, where its output voltage is independent of load, in order to simplify the design process, the output voltage during CV mode for LLC1 and LLC2 are assumed to equal to the half of the total output voltage. For LLC2, its resonant frequency is variable to achieve closed loop control.

Since the output voltage of LLC2 ranges from 65V to 210V during the CC mode, it is reasonable to design its parameters firstly.

4.3.1 Design Considerations for LLC2

Unlike LLC1, LLC2 is designed to fulfill the duty of closed-loop control. The constant output voltage and current characteristics are adopted here to simplify the control. The basic idea is, during the CC mode, LLC2 operates at lower resonant frequency f_{m2} and the output current will remain constant and independent of the load; during CV mode, LLC2 will operate at higher resonant frequency f_{r2} and the output voltage will remain constant. In this research, the switching frequency remains constant, the magnetic control is adopted, the basic idea is that a variable inductor is used instead of a constant inductor value, and the details are discussed in Chapter 5.

There exist four resonant frequencies in this topology as shown in Table 4-3.

Table 4-3 Resonant frequency in LLC2.

Resonant components	Resonant frequency
L_{r2_CC}, C_{r2}	$f_{r2,1}=\frac{1}{2\pi\sqrt{L_{r2,CC}C_{r2}}}$
L_{r2_CV}, C_{r2}	$f_{r2,2}=\frac{1}{2\pi\sqrt{L_{r2,CV}C_{r2}}}$
L_{r2_CC}, C_{r2}, L_{m2}	$f_{m2,1}=\frac{1}{2\pi\sqrt{(L_{r2,CC}+L_{m2})\cdot C_{r2}}}$
L_{r2_CV}, C_{r2}, L_{m2}	$f_{m2,2}=\frac{1}{2\pi\sqrt{(L_{r2,CV}+L_{m2})\cdot C_{r2}}}$

Note: L_{r2_CC} is the inductance value during CC stage, while L_{r2_CV} is the inductance value during CV stage.

In this research, the resonant frequency $f_{r2,2}$ and $f_{m2,1}$ are adopted in CV and CC mode respectively.

Since the switching frequency remains constant, $f_{r2,\,2}$ and $f_{m2,\,1}$ should equal to the switching frequency.

$$f_{r2,\,2}=\frac{1}{2\pi\sqrt{L_{r2,\,CV}C_{r2}}}=f_{m2,\,1}=\frac{1}{2\pi\sqrt{(L_{r2,\,CC}+L_{m2})\cdot C_{r2}}}=f_s \tag{4-3}$$

1) The selection of transformer turns ratio

During the CV mode, LLC2 operates at higher resonant frequency $f_{r2,2}$, the output voltage is independent of load, and the turns ratio can be determined by the relation between input voltage and output voltage.

$$n_2=\frac{V_{in}}{V_{o2}}=\frac{400}{210}=1.9 \tag{4-4}$$

2) The selection of resonant tank components

For LLC2, the magnetic inductance value L_{m2} will be determined first according to the characteristic discussed in Chapter 3.

$$I_o(s)=\frac{V_{o2}(s)}{R_{ac}}=\frac{1}{n_2}\frac{V_{in}}{R_{ac}(1+\dfrac{L_{r2}s+\dfrac{1}{C_{r2}s}}{L_{m2}s})+L_{r2}s+\dfrac{1}{C_{r2}s}} \tag{4-5}$$

Since during CC mode, LLC2 is operating at lower resonant frequency $f_{m2,1}$, and the resonant components are L_{r2_CC}, C_{r2} and L_{m2}. The constant output current is 7.8A, so L_{m2} equals to

$$L_{m2}=\frac{n_2V_{in}}{2\pi f_sI_{o2}}=\frac{1.9\times400}{2\times3.14\times100\times10^3\times7.8}=155uH \tag{4-6}$$

The next step is to find a reasonable range for the resonant inductance. And the guideline is the RMS current of the resonant tank. The expression of the RMS current is

$$I_{Lr2,\,RMS}=\sqrt{\sum_{N=1,3,5\cdots}^{\infty}\left(\frac{4V_{in}}{\sqrt{2}N\pi\left|Z_{in2}(jNw_s)\right|}\right)^2} \tag{4-7}$$

where Z_{in2} is the input impedance of LLC2, which can be expressed as

$$Z_{in2}(jNw_s) = L_{r2}jNw_s + \frac{1}{C_{r2}jNw_s} + \frac{L_{m2}jNw_sR_{ac2}}{L_{m2}jNw_s + R_{ac2}} \tag{4-8}$$

For LLC2, during the CC mode, the load resistance ranges from 8.3ohm to 26.9ohm. Therefore, the equivalent AC resistance can be expressed as

$$R_{ac2,\,\min,\,CC} = \frac{8n_2^2}{\pi^2} \cdot R_{Ld2,\,\min,\,CC} = 24.4\Omega \tag{4-9}$$

$$R_{ac2,\,\max,\,CC} = \frac{8n_2^2}{\pi^2} \cdot R_{Ld2,\,\max,\,CC} = 78.8\Omega \tag{4-10}$$

According to equation (4-3), C_{r2} is dependent on L_{r2}. Figure 4-5 shows the relation of the RMS current of the resonant tank and different resonant inductance values. The blue one represents for R_{ac2} equals to 24.4ohm, while the red one represents for R_{ac2} equals to 78.8ohm. It can be seen that when the resonant inductance is greater than 40uH, the slope of the RMS current becomes slow. Therefore, in this research, L_{r2}=50uH is selected.

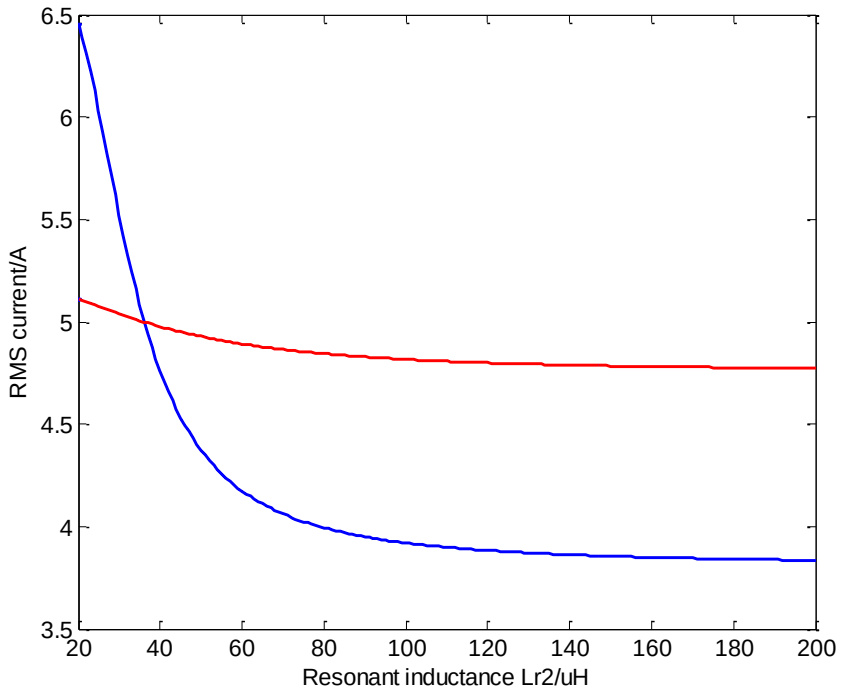


Figure 4-5 RMS current of the resonant tank with different resonant inductance value.

Then, the resonant capacitor and the resonant inductor range can be calculated according to

$$C_{r2} = \frac{1}{4\pi^2 (L_{r2,\,CC} + L_{m2})} = 12nF \tag{4-11}$$

$$L_{r2\_CV} = L_{r2\_CC} + L_{m2} = 205uH \tag{4-12}$$

4.3.2 Design Considerations for LLC1

According to the above analysis, LLC1 is designed to operate at the resonant frequency, where its efficiency is the highest and output voltage is independent of the load.

1) The selection of transformer turns ratio;

When the switching frequency equals to the resonant frequency f_{r1}, the DC gain of the LLC is 1, so the turns ration can be determined according to

$$n_1 = \frac{V_{in}}{V_{o1}} = \frac{400}{210} = 1.9 \tag{4-13}$$

2) The selection of the resonant components;

For LLC1, its DC voltage gain is constant and independent of the load. Therefore, the design guidelines for LLC1 are: 1) the total resonant converter operates in inductive region; 2) minimize the RMS current flows through the resonant network, which is related to the losses

For LLC1, during the CC mode, the range of the equivalent load resistance can be calculated according to Figure 4-2.

$$R_{ac1,\,CC} = \frac{8n^2}{\pi^2} \cdot R_{Ld1,\,CC} = 78.8\Omega \tag{4-14}$$

Due to the connection of LLC1 and LLC2, the total input impedance can be expressed as

$$Z_{in} = Z_{in1} // Z_{in2} \tag{4-15}$$

At the resonant frequency operating point, the input impedance can be simplified as

$$Z_{in1} = \frac{L_{m1} s R_{ac1}}{L_{m1} s + R_{ac1}} \tag{4-16}$$

Figure 4-6 shows the total input impedance angle with different value of L_{r2} and L_{m1}. It can be seen that magnetic inductance no greater than 70uH is required in order to achieve ZVS operation for all operation conditions.

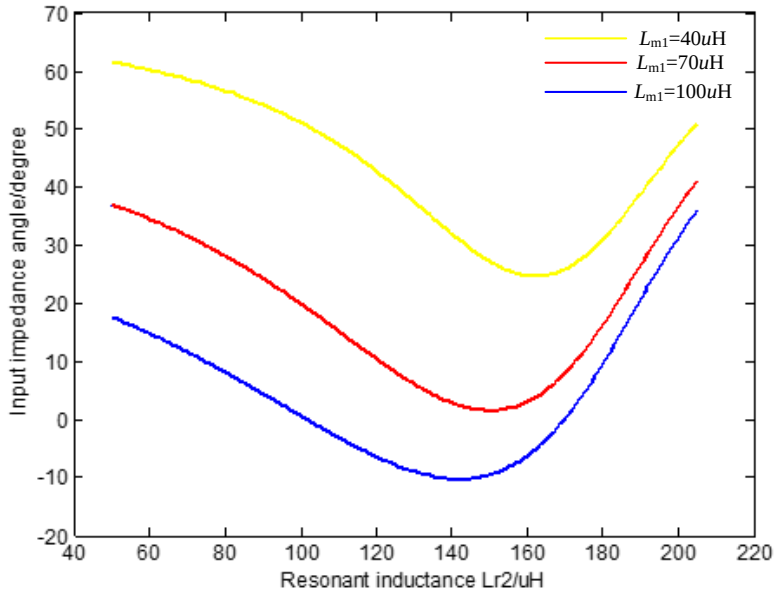


Figure 4-6 Input impedance angle with different value of L_{r2} and L_{m1}.

For LLC1, it is operating at the resonant frequency, the waveform in steady state is shown in Figure 3-3. According to previous analysis, the resonant current is a sine wave, which can be expressed as

$$i_{Lr1}(t) = I_{m1} \sin(2\pi f_{r1} t - \phi_1) \tag{4-17}$$

where ϕ_1 is the initial position of resonant current and I_{m1} is the magnitude of resonant current. The expression for magnetic current i_{Lm1} can be expressed as

$$i_{Lm1}(t)=\begin{cases}\dfrac{n_1V_{o1}}{L_{m1}}t-\dfrac{n_1V_{o1}}{4L_{m1}f_{r1}}(0<t<\dfrac{T_s}{2})\\ -\dfrac{n_1V_{o1}}{L_{m1}}t+\dfrac{n_1V_{o1}}{4L_{m1}f_{r1}}(\dfrac{T_s}{2}<t<T_s)\end{cases} \tag{4-18}$$

The secondary side current i_{S1} can be expressed as

$$i_{s1}(t)=n\left|i_{Lr1}(t)-i_{Lm1}(t)\right| \tag{4-19}$$

The output current is the secondary side current goes through output capacitor,

$$I_{o1}=\frac{1}{T_s}\int_0^{Ts}i_{s1}(t)dt=\frac{n_1}{T_s}\int_0^{Ts}\left|i_{Lr1}(t)-i_{Lm1}(t)\right|dt \tag{4-20}$$

By substituting (4-17) and (4-18) into (4-20), we can obtain

$$I_{m1}\cos(\phi_1)=\frac{\pi I_{o1}}{2n_1} \tag{4-21}$$

At t=0, i_{Lm1} and i_{Lr1} are equal,

$$I_{m1}\sin(-\phi_1)=-\frac{n_1V_{o1}}{4L_{m1}f_{r1}} \tag{4-22}$$

According to (4-21) and (4-22), the maximum value of magnetic current is

$$I_{m1}=\sqrt{\frac{\pi^2{I_{o1}}^2}{4{n_1}^2}+\frac{{n_1}^2{V_{o1}}^2}{16{L_{m1}}^2{f_{r1}}^2}} \tag{4-23}$$

And the RMS value can be easily obtained

$$I_{Lr1-RMS}=\frac{I_{m1}}{\sqrt{2}}=\sqrt{\frac{\pi^2{I_{o1}}^2}{8{n_1}^2}+\frac{{n_1}^2{V_{o1}}^2}{32{L_{m1}}^2{f_{r1}}^2}} \tag{4-24}$$

Obviously, the resonant RMS current is inversely proportional with the magnetic inductance. And Figure 4-7 shows the relationship between them. It can be seen that when the magnetic inductance value is greater than 60*u*H, the decrease slop of the RMS current is slow. Therefore, based on Figure 4-6 and 4-7, magnetic inductance equals to 70*u*H is selected. Since when LLC resonant converter is operating at the higher resonant frequency, the RMS current of the resonant tank has

no relation with the resonant inductance; however, the voltage stress on the resonant capacitor is inversely proportional with the resonant capacitor value. Therefore, a relatively small value of the resonant inductance is preferred. In this research, Lambda equals to 5 is selected. The resonant inductance value and resonant capacitor value can be determined according to the following equation

$$L_{r1} = \frac{L_{m1}}{\lambda_1} = 14uH \tag{4-25}$$

$$C_{r1} = \frac{1}{(2\pi f_{r1})^2 L_{r1}} = 180nF \tag{4-26}$$

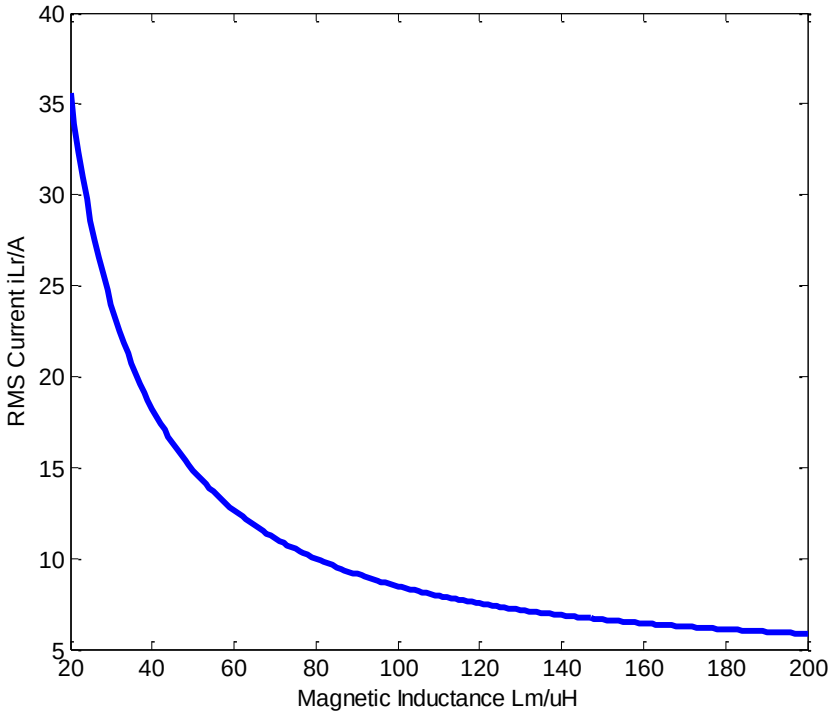


Figure 4-7 The relationship between RMS current and magnetic inductance.

3) Selection of primary switches

The RMS current for primary switch can be expressed as

$$I_{Q1-RMS}=\sqrt{\frac{1}{T_s}\int_0^{Ts/2} i_{Lr1}{}^2(t)dt}=\sqrt{\frac{1}{2T_s}\int_0^{Ts} i_{Lr1}{}^2(t)dt}=\frac{I_{Lr1-RMS}}{\sqrt{2}}=\sqrt{\frac{\pi^2 I_{o1}{}^2}{16n_1{}^2}+\frac{n_1{}^2 V_{o1}{}^2}{64L_{m1}{}^2 f_{r1}{}^2}}} \tag{4-27}$$

At steady state, the maximum current flows through primary switch is the maximum value of resonant current i_{Lr1}. During the whole charging process, the maximum output current is 7.8A in CC mode. By replacing I_{o1} with 7.8A, we can obtain

$$I_{m1}=\sqrt{\frac{\pi^2 I_{o1}{}^2}{4n_1{}^2}+\frac{n_1{}^2 V_{o1}{}^2}{16L_{m1}{}^2 f_{r1}{}^2}}=15.64A \tag{4-28}$$

$$I_{Q1-RMS}=\sqrt{\frac{\pi^2 I_{o1}{}^2}{16n_1{}^2}+\frac{n_1{}^2 V_{o1}{}^2}{64L_{m1}{}^2 f_{r1}{}^2}}=7.82A \tag{4-29}$$

4) Selection of Secondary Side Diodes

For the secondary side diodes, the current flows through the diode can be expressed as

$$i_{D1}(t)=n_1(i_{Lr1}(t)-i_{Lm1}(t)) \tag{4-30}$$

The RMS value of diode current is

$$I_{D1-RMS}=\sqrt{\frac{1}{T_s}\int_0^{Ts/2} i_D{}^2(t)dt}=\frac{1}{4}\sqrt{\frac{\pi^2 I_{o1}{}^2}{4}+\frac{5n_1{}^4 V_{o1}{}^2}{48L_{m1}{}^2 f_{r1}{}^2}-\frac{n_1{}^4 V_{o1}{}^2}{\pi^2 L_{m1}{}^2 f_{r1}{}^2}}=3.39A \tag{4-31}$$

And the average value is

$$I_{D1-AVG}=\sqrt{\frac{1}{T_s}\int_0^{Ts/2} i_D(t)dt}=\frac{1}{4}I_{o1}=1.95A \tag{4-32}$$

According to (4-22), we can obtain the initial position

$$\phi_1=-\arcsin(-\frac{n_1 V_{o1}}{4I_{m1}L_{m1}f_{r1}})=1.146 \tag{4-33}$$

The time when i_{D1} reaches the maximum value can be obtained by setting the deviation of equation (4-30) to zero.

$$t_p = \frac{\phi_1 + \arccos(\frac{n_1 V_{o1}}{2\pi I_{m1} L_{m1} f_{r1}})}{2\pi f_{r1}} = 3.3391\times10^{-6}\mathrm{S} \tag{4-34}$$

By substituting (4-33) and (4-34) into (4-30), we can obtain the maximum current flows through the diode.

$$I_{D-MAX} = 15.12A \tag{4-35}$$

The voltage stress across diode is the output voltage, which is 210V.

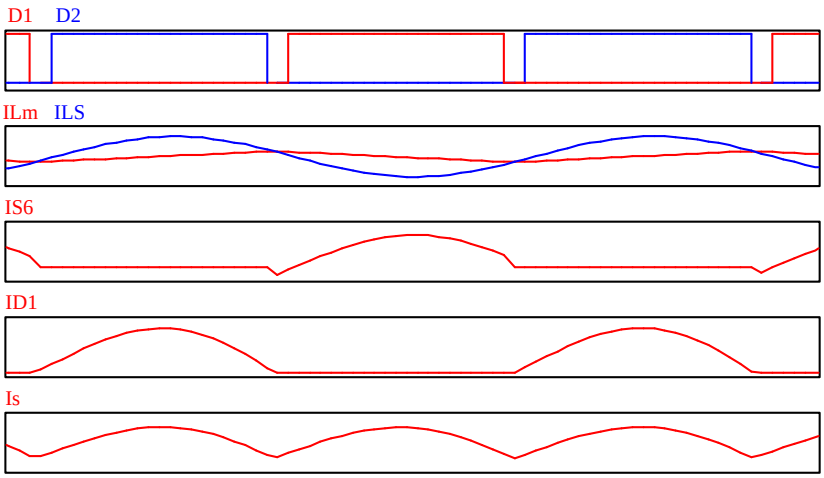


Figure 4-8 Theoretical waveforms when f_s=f_r.

5) Selection of Output Capacitor

The design guideline for the output capacitor is the output voltage ripple requirement. The waveforms of the secondary side current, capacitor current and output voltage are shown in Figure 4-9. In order to calculate the output voltage ripple, t_1 and t_2 should be found first. Obviously, t_1 and t_2 are the time when the secondary side current equals to output current. Based on that, the secondary side current and output current are draw in one figure, and t_1, t_2 can be found.

$$t_1 = 3.12us \tag{4-36}$$

$$t_2 = 5.38us \tag{4-37}$$

Obviously, the output voltage ripple can be calculated according to the following equation.

$$\Delta V_{o1} = \frac{1}{C_{o1}} \int_{t1}^{t2} [i_{s1}(t) - I_{o1}] dt = \frac{1}{C_{o1}} 1.66 \times 10^{-5} \tag{4-38}$$

In this research, the requirement for the output voltage ripple is 2%, so the output capacitor can be calculated.

$$C_{o1} = \frac{1.66 \times 10^{-5}}{\Delta V_{o1}} = \frac{1.66 \times 10^{-5}}{210 \times 0.02} = 4uF \tag{4-39}$$

Finally, C_{o1} equals to 10uF is selected.

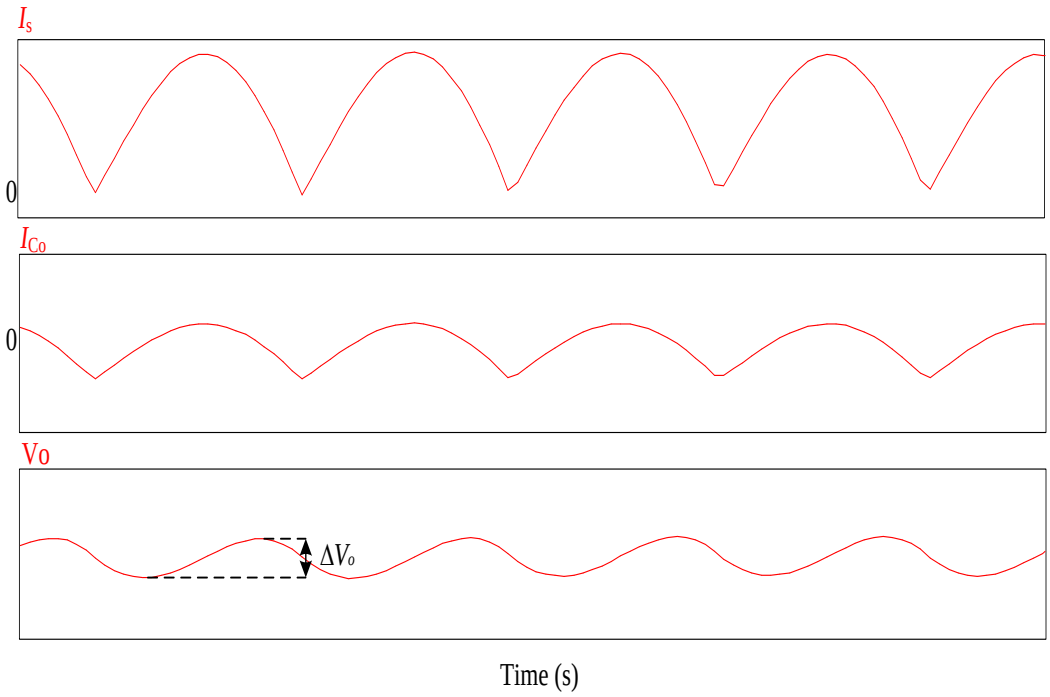


Figure 4-9 Theoretical waveforms of secondary side current, capacitor current and output voltage.

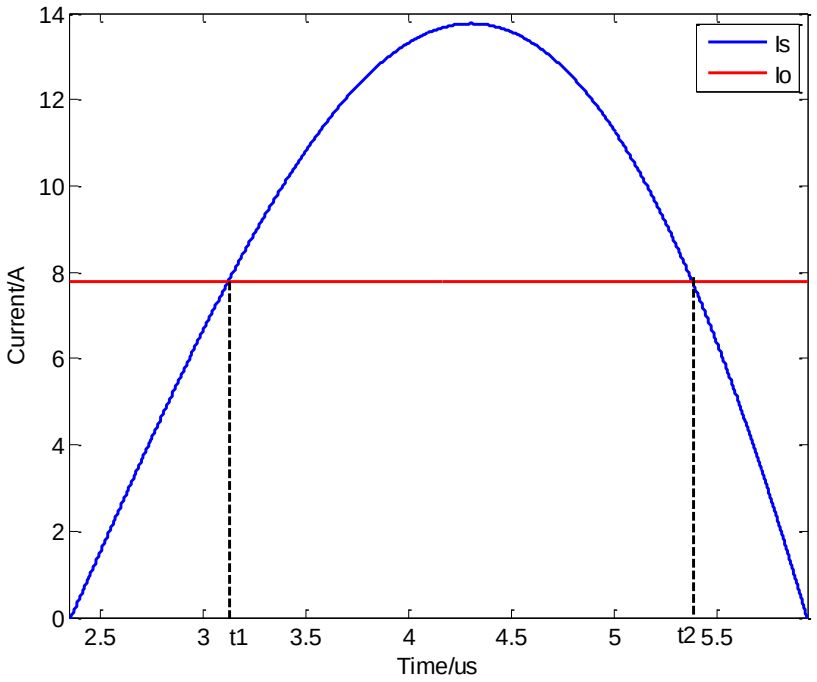


Figure 4-10 Mathematical expressions of secondary side current and output current.

In order to simplify the calculation, the current stress and voltage stress for the components of LLC2 are less than that of LLC1. Therefore, the components can be selected based on the calculations for LLC1. It is noteworthy to mention that the RMS current calculated before should be two times due to the parallel connection.

4.4 Simulation Verification

In this part, the parameters calculated before are adopt here to verify the correctness and effectiveness. The simulation parameters are shown in Table 4-4.

Table 4-4 Simulation parameters for LLC1 and LLC2.

Input voltage U_{in}/V	400

Resonant inductor L_{r1}/uH	14
Resonant capacitor C_{r1}/nF	180
Magnetizing inductance L_{m1}/uH	70
Resonant frequency f_{r1}/kHz	100
Output Capacitor C_{o1}/uF	10
Turns ration n_1	1.9:1
Resonant inductor L_{r2}/uH	50-205
Resonant capacitor C_{r2}/nF	12
Magnetizing inductance L_{m2}/uH	155
Resonant frequency f_{r2}/kHz	100
Output Capacitor C_{o2}/uF	10
Turns ration n_2	1.9:1

Firstly, the calculations for the current stress will be examined. Figure 4-11 shows the simulation waveforms of magnetic inductance current, MOSFET current, diode current and output voltage of LLC1 during CC mode; while Figure 4-12 shows the simulation waveforms of LLC2 during CC mode. It can be seen that the simulation results agree with the calculations.

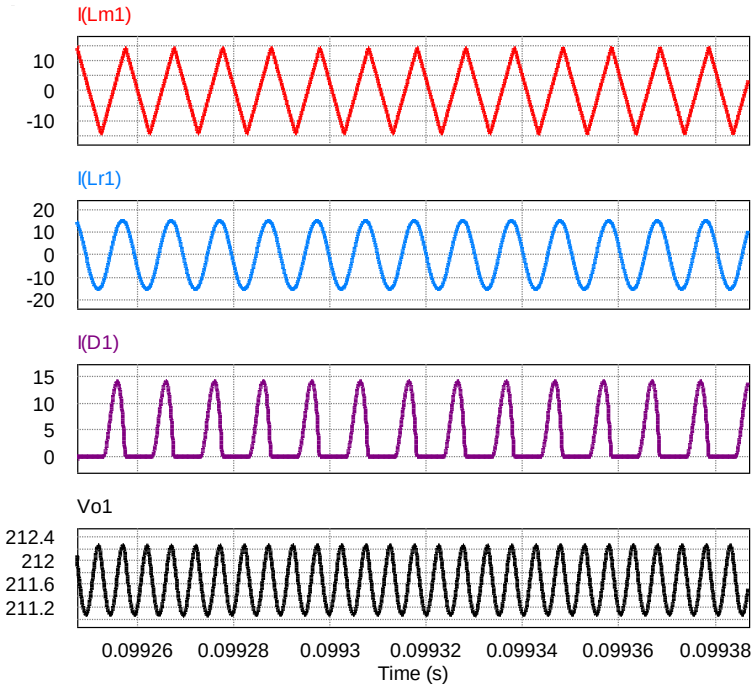


Figure 4-11 Simulation waveforms of LLC1 during CC mode.

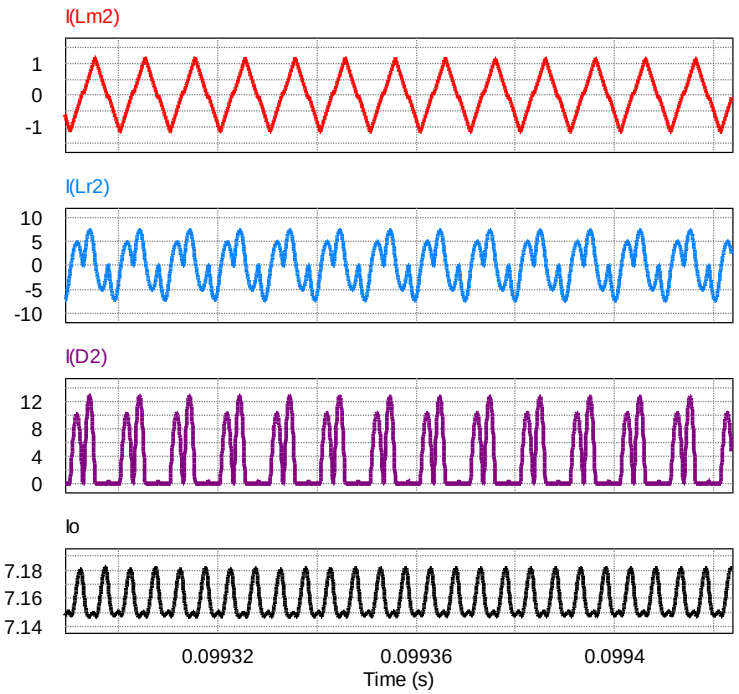


Figure 4-12 Simulation waveforms of LLC2 during CC mode.

Figure 4-13 shows the simulation waveforms of LLC2 during CV mode.

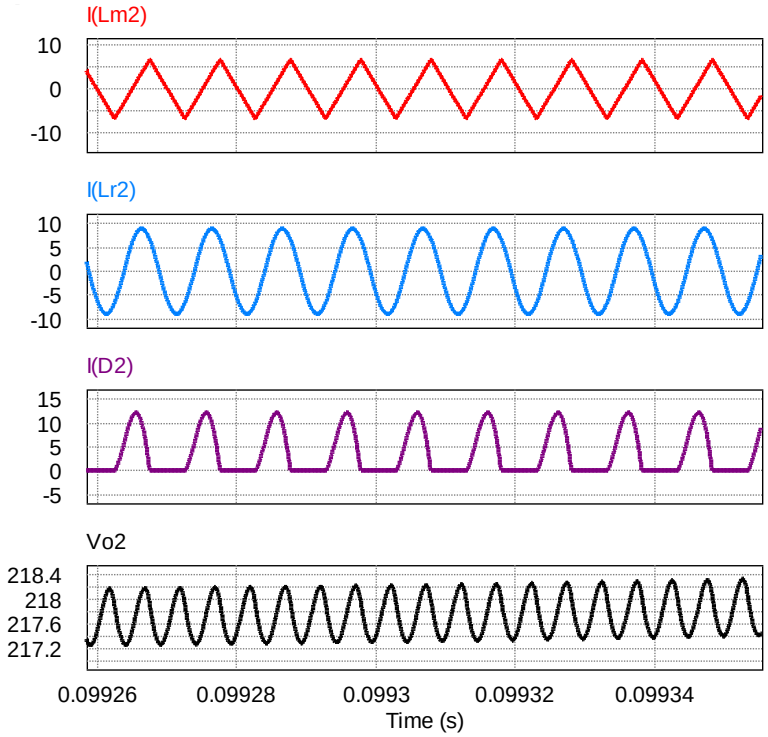


Figure 4-13 Simulation waveforms of LLC2 during CV mode.

Next, the whole system, which inculdes interleaved totem-pole bridgeless PFC and two LLC resonant converters, operation will be discussed. The simulation circuit is shown in Figure 4-14.

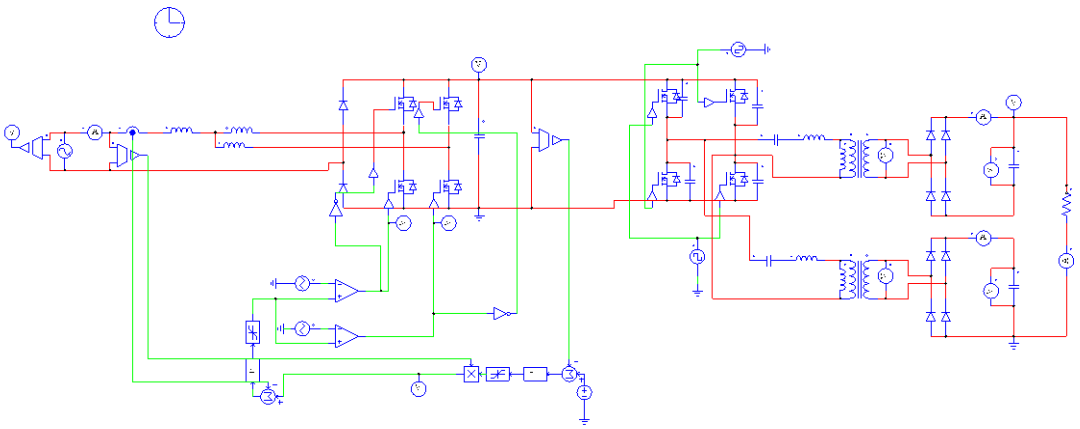


Figure 4-14 Simulation circuit of the proposed battery charger.

In this simulation case, the AC input voltage is 220VRMS. And six operation points are selected to verify the feasibility of the proposed topology. The details are shown in Table 4-5. Figure 4-15 shows the simulation waveforms of input current, input voltage, and DC-link voltage. Figure 4-16 shows the simulation waveforms of output voltage V_{o1}, V_{o2} and the output current I_o. Figure 4-17 shows the simulation waveforms of the drive signal, voltage across the corresponding switch and secondary diode. Figure 4-18 shows the input voltage and current of the total resonant tank. It can be seen that the ZVS operation for the primary switches and ZCS operation for the secondary diodes are achieved during the whole charging process.

Table 4-5 Theoretical values for six operation points.

Operation point	a	b	c	d	e	f
Charge mode	CC	CC	CC/CV	CV	CV	CV
Output power/W	2145	2737	3300	2000	1000	330
Output voltage of LLC1/V	210	210	210	210	210	210
Output voltage of LLC2/V	65	141	210	210	210	210
Output current/A	7.8	7.8	7.8	4.76	2.38	0.78
Equivalent load resistance/ohm	35	45	54	88	160	538

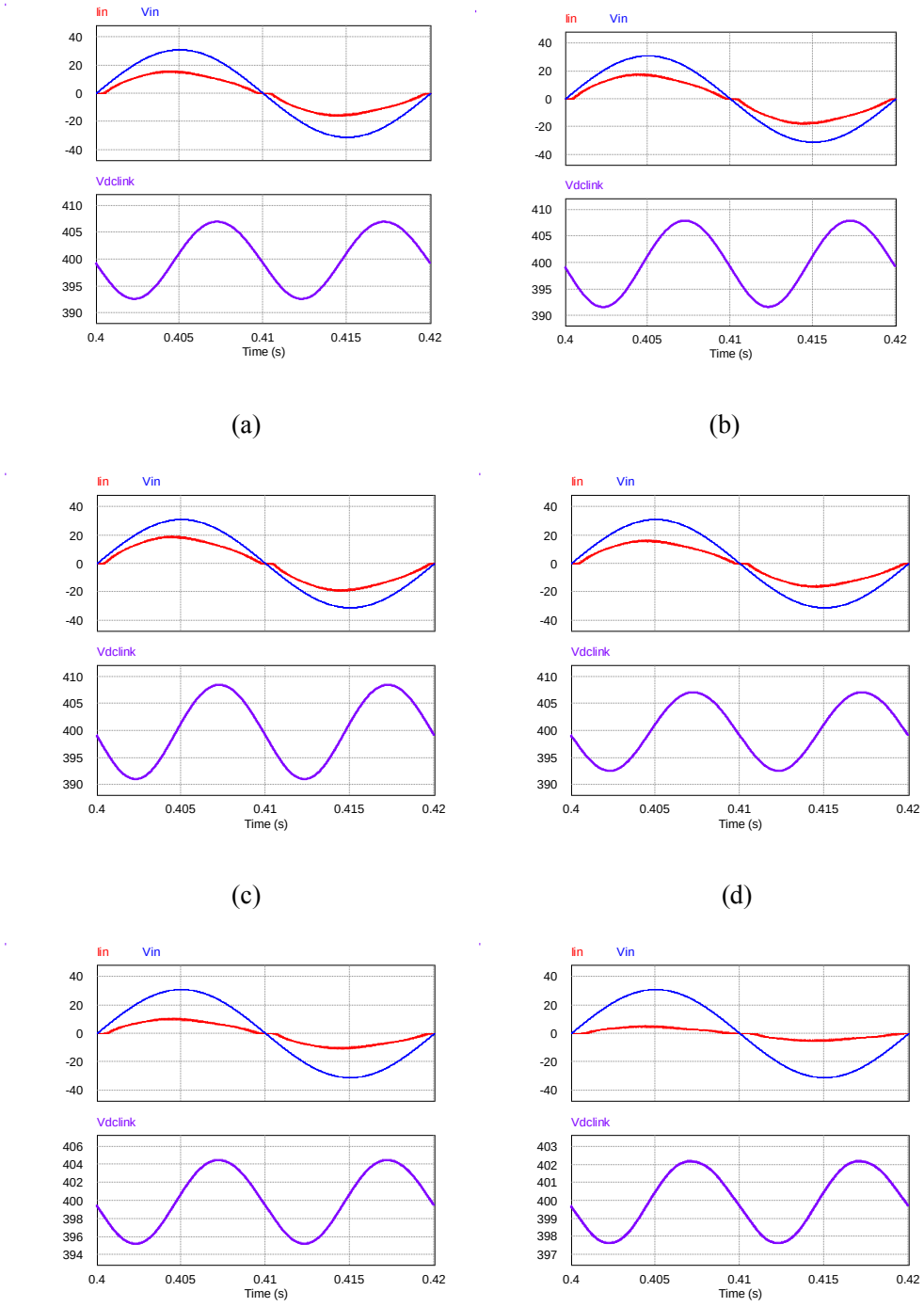
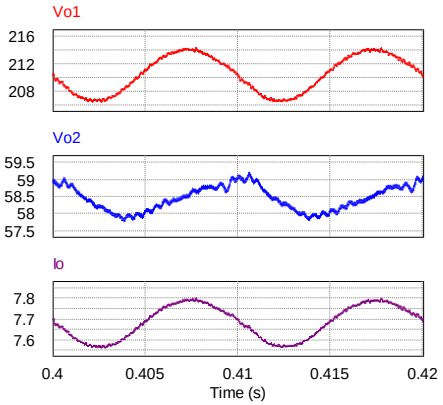


Figure 4-15 Simulation waveforms of input current, input voltage, and DC-link voltage.



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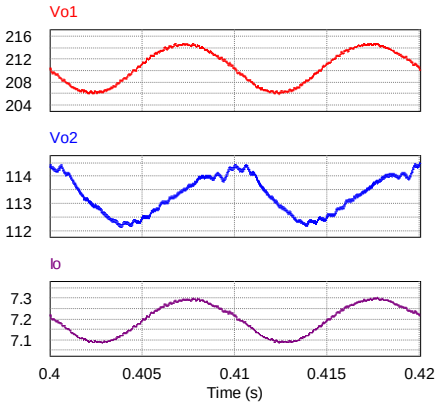

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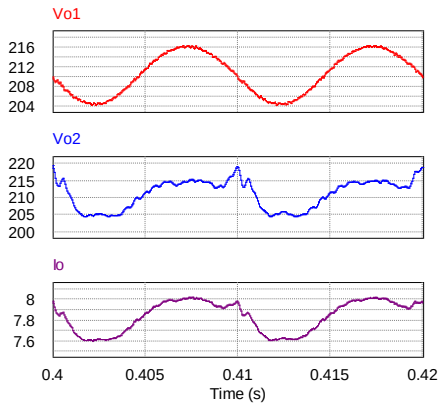

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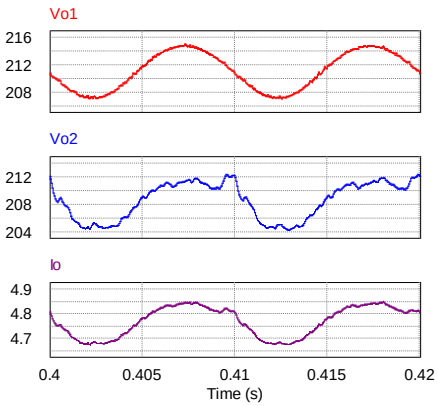

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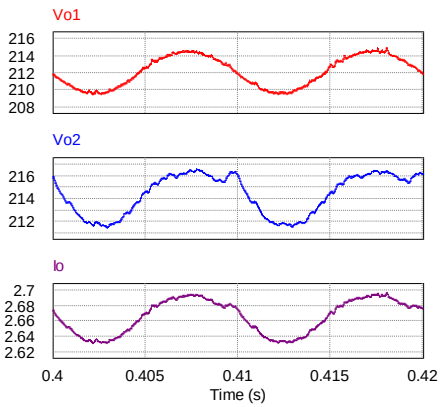

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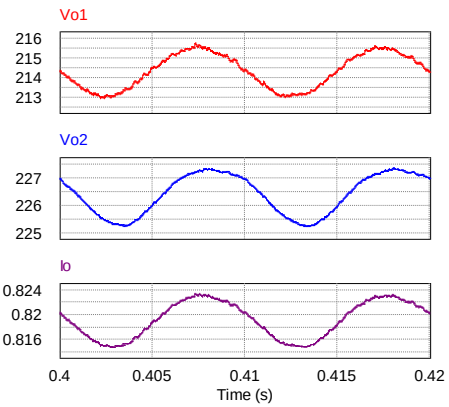

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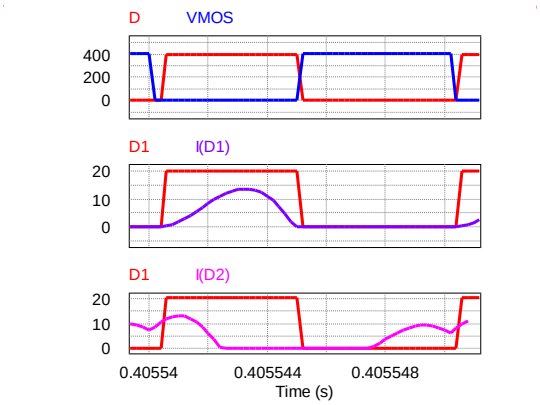
Figure 4-16 Simulation waveforms of output voltage V_{o1}, V_{o2} and output current I_o.



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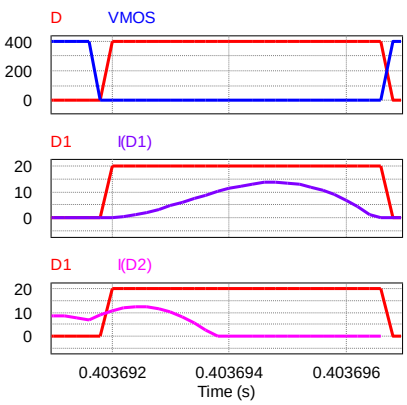

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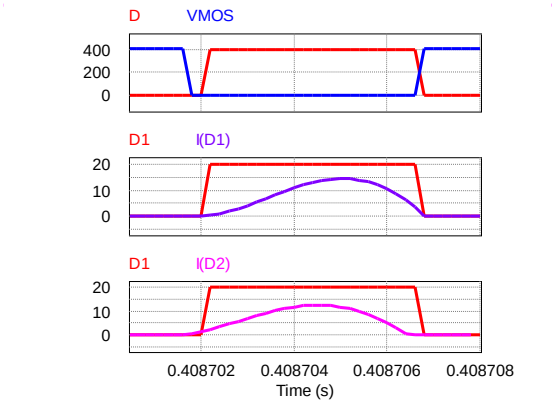

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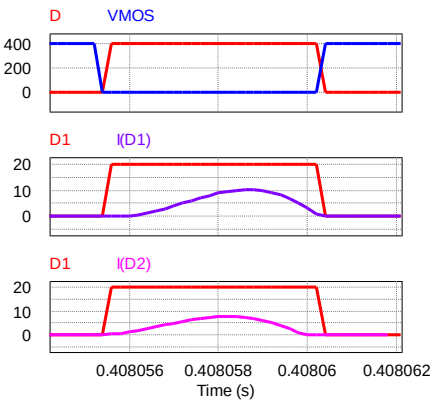

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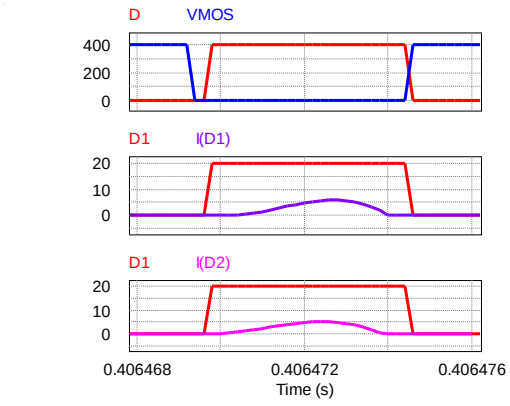

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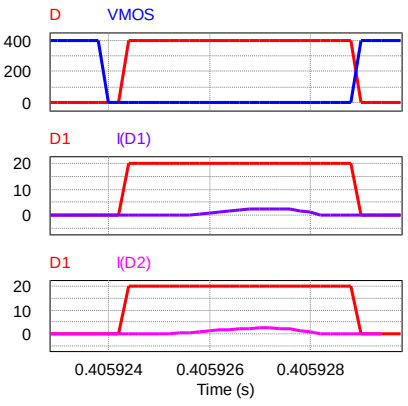

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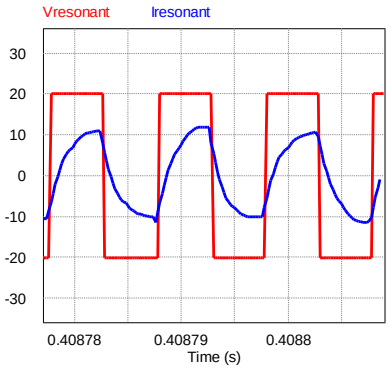
Figure 4-17 Simulation waveforms of the drive signal, voltage across the corresponding switch and secondary

diodes.



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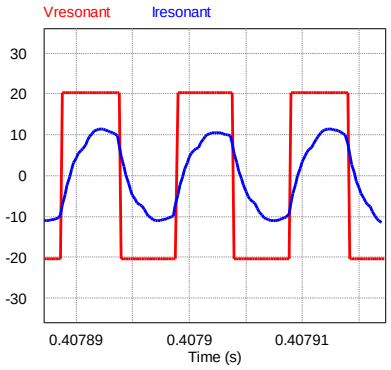

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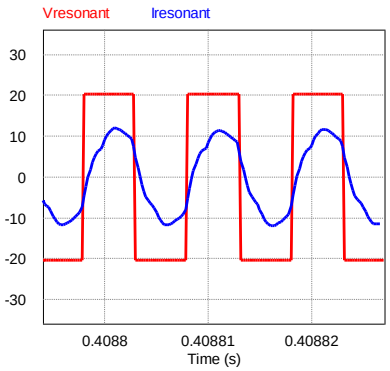

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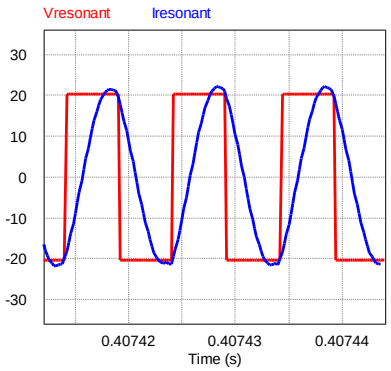

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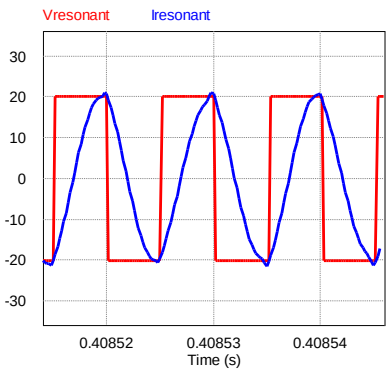

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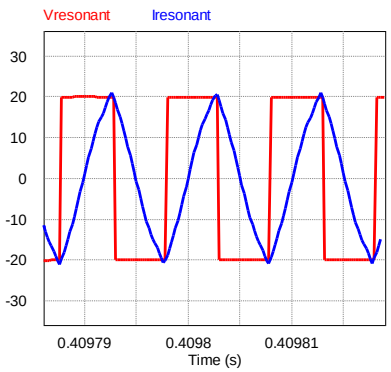


(f)

Figure 4-18 Simulation waveforms of the total resonant tank input voltage and input current.

The measured results for the six operation points are shown in Table 4-6. Meanwile, Figure 4-19 shows the measured output voltage of LLC1 and LLC2 during the charging process; and Figure 4-17 shows the measured output power of the system during the charging process. It can be seen that the results agree with the theoretical analysis, the differences are relatively small.

Table 4-6 Measured values for six operation points.

Operation point	a	b	c	d	e	F
Charge mode	CC	CC	CC/CV	CV	CV	CV
Output power/W	2070	2333	3319	2002	1140	362
Output voltage of LLC1/V	210.5	210.6	210.5	211.1	212.2	214.3
Output voltage of LLC2/V	58.5	113.3	211.2	208.6	214.4	226.4
Output current/A	7.69	7.20	7.84	4.77	2.67	0.82
Equivalent load resistance/ohm	35	45	54	88	160	538

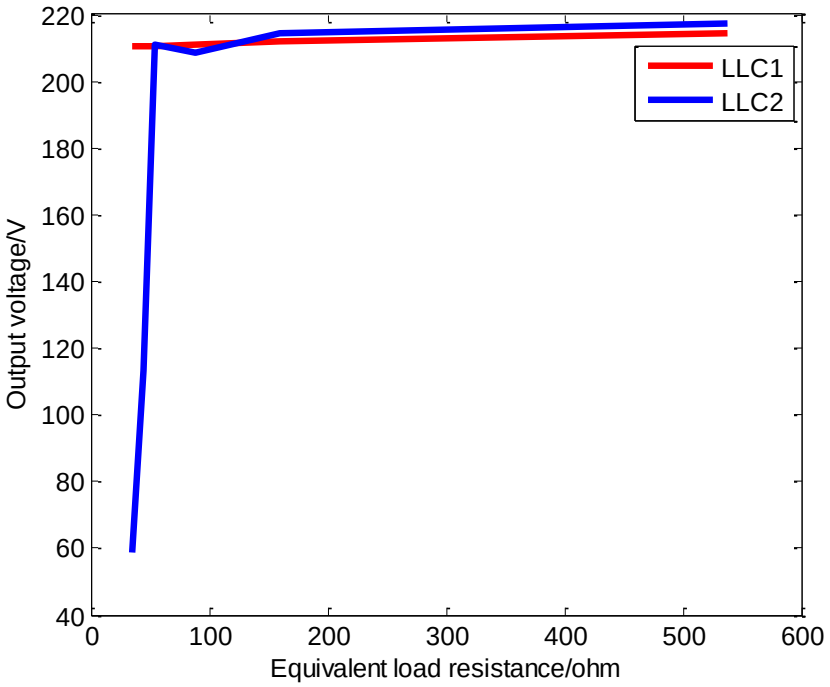


Figure 4-19 The measured output voltage of LLC1 and LLC2 during the charging process.

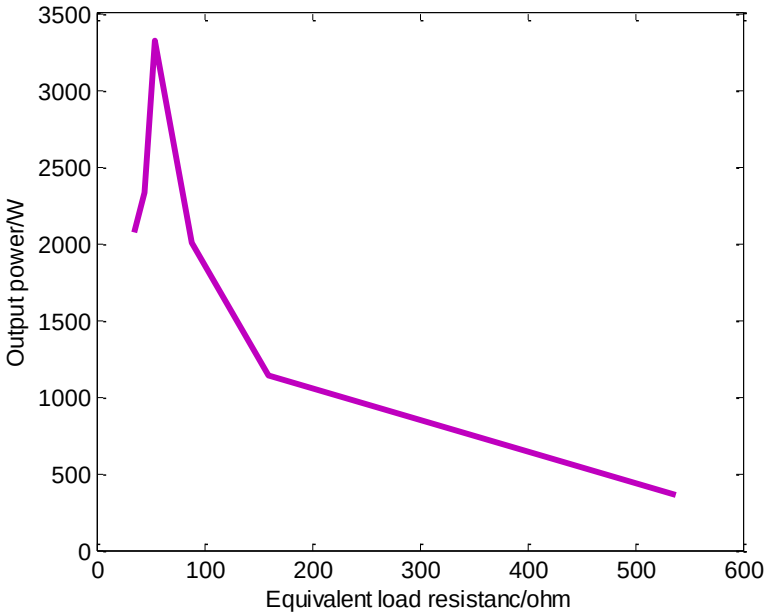


Figure 4-20 The measured output power of the system during the charging process.

4.5 Summary

In this chapter, the battery charging profile is discussed first, which points out the requirements for the battery charger; then, the proposed topology, which includes an interleaved totem-pole bridgeless PFC and two LLC resonant converters, is analyzed; in addition, the design considerations for the LLC resonant converters are presented, and the design procedures are shown in the flow chart in Figure 4-18. Based on the analysis, the primary switches can achieve ZVS and the secondary diodes can achieve ZCS druing the whole operation range, which can further improve the efficiency of the proposed topology. Finally, a simulation case is introduced to verify the theoretical analysis. From the simulation results, the open loop operation has an acceptable accuracy, which will make the control much more simple.

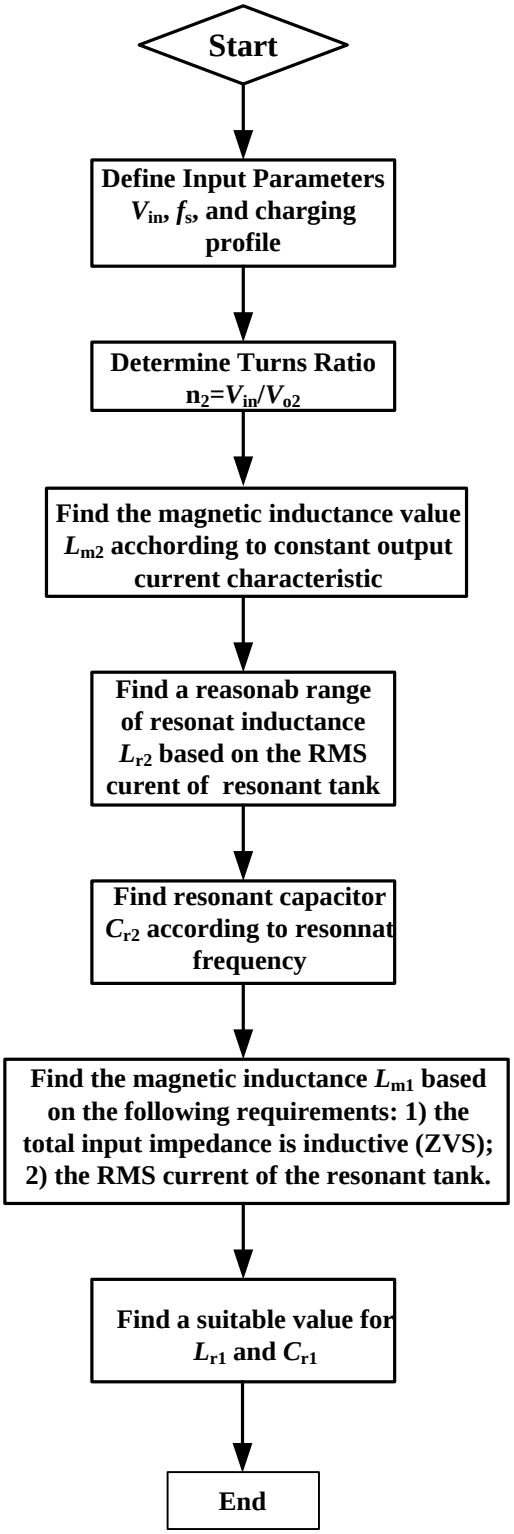


Figure 4-21 Design procedures of the proposed battery charger.

Chapter 5 Control Strategy for The Proposed On-board Battery Charger

For LLC resonant converter, there exist two most adopted control schemes [33], [34]. One is to employ switching frequency as a control parameter to regulate the output voltage. The impedances of the reactive elements of the resonant tank vary with the operating switching frequency, which can regulate the output voltage. In some cases, depending on the voltage ratio and the power handled by the resonant tank, the frequency excursion can be high, which makes the design of EMI filter more complicate. Another control scheme is phase shift. Usually, a full-bridge topology is adopted, and the gate signals of each branch are shifted in time to obtain a quasisquare output voltage with adjustable RMS value. The main disadvantage of this strategy is that the ZVS ranges of the active switches of the lagging phase legs in the primary side inverter are severely limited; in addition, it can only work for full-bridge topology and the control circuit is complex. In order to solve the above problems, magnetic control scheme is proposed. It has the following advantages: 1) the switching frequency is constant, which can maximize the system efficiency; 2) the EMI design is simple and its size is reduced due to constant switching frequency; 3) the control circuit is relatively simple; 4) ZVS operation for the primary switches can be achieved. However, the disadvantages of magnetic control cannot be ignored: 1) the occurrence of related power loss; 2) response speed is relatively slow.

In this chapter, the magnetic control is introduced first; then the design considerations of the variable inductor for the proposed topology is discussed; the spice model for the variable inductor

is studied, and the structure is simulated in LTspice; finally, a summary is drawn.

5.1 Introduction of The Magnetic Control Scheme

The idea of variable inductor can be track back to 1987. After that, variable inductors have been applied for many power electronics applications, such as dimming of fluorescent lamps, voltage control in DC-DC resonant converter, LED drivers [35]-[40].

For the variable inductance, it can be controlled by a dc bias current, which can change the effective inductance value by taking certain parts of the magnetic core to a close-to-saturation region. The effective magnetic reluctance is increased, which results in a lower value for the inductance. And a typical characteristic of inductance versus dc bias current is shown in Figure 5-1.

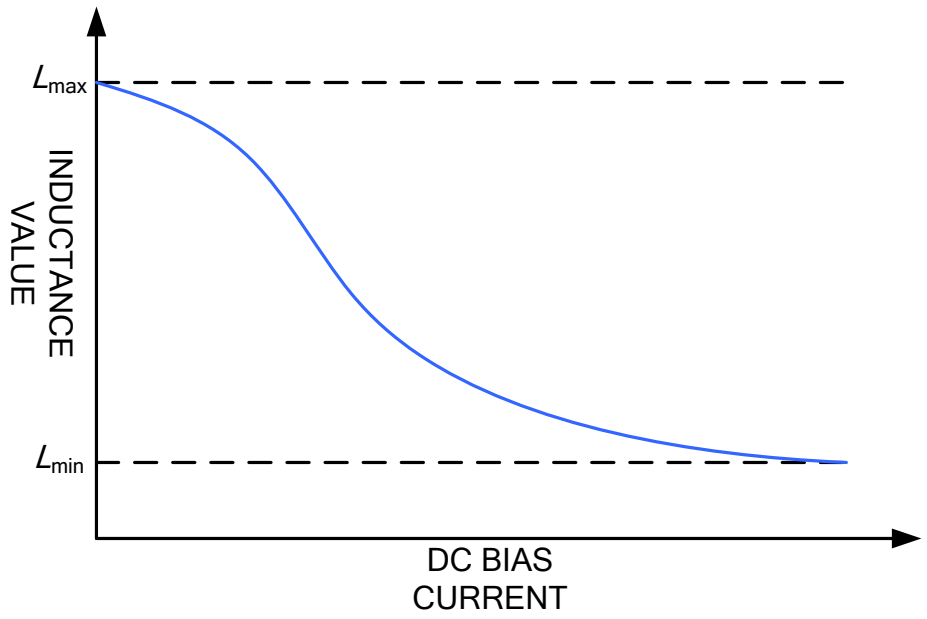


Figure 5-1 Inductance value versus dc bias current of a variable inductor.

The principle of the variable inductor can be shown in Figure 5-2. The basic idea is a voltage controlled current source. Firstly, during CC mode, the current feedback is compared with the

current reference, in this case, the current reference is 7.8A; then, the error goes through the PI controller and the limiter, the control signal is obtained; according to the control signal, the output current of the current source is adjusted, therefore, the inductance across point A and B is adjusted, the goal of magnetic control is achieved. The details of the variable inductor are shown in Figure 5-3.

The structure of the variable inductor uses a double E core. The control winding or auxiliary winding is divided into two identical portions with the number of turns N_{DC}, which is mounted on the lateral legs of the core. The inductor winding or main winding with the number of turns N_{AC} is placed on the air-gapped middle of the core. The dc bias current allows the modification of the inductance of the main winding. In addition, the dc bias current is inversely proportional with the inductance value.

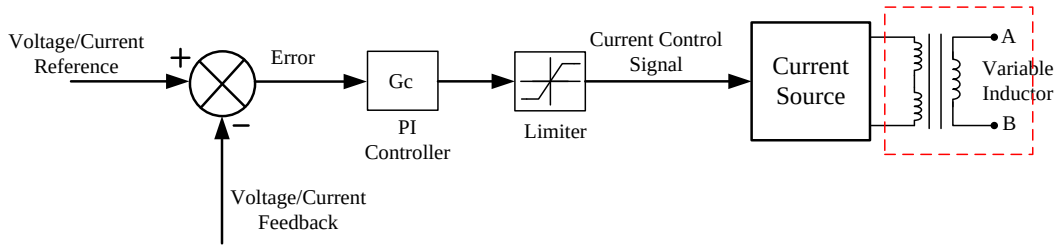


Figure 5-2 Operation principle of the magnetic control scheme.

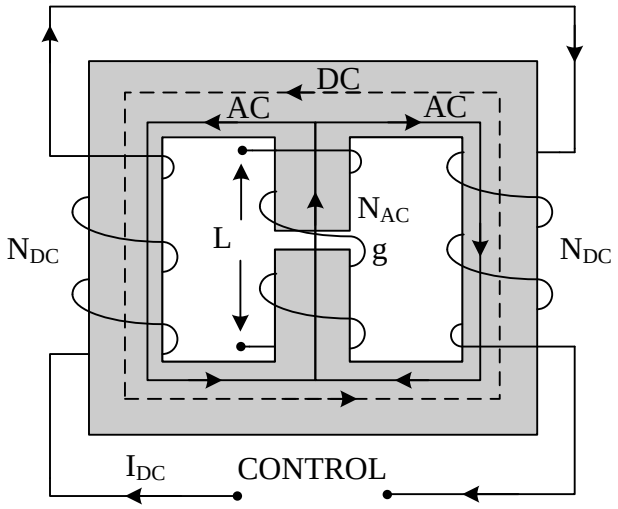


Figure 5-3 Structure of the variable inductor.

5.2 Design Considerations for The Variable Inductor

In this part, the design procedures for variable inductor are discussed.

1) Maximum inductance

The first step is to determine the maximum inductance required in the system. Based on the previous analysis in Chapter 4, the maximum inductance is obtained during CV mode, that is 210*u*H. In order to have some margin and also to allow for an operation in a more linear region. The maximum inductance value equals to 240*u*H is selected.

2) Magnetic core and material

The next step is to select a suitable core and material. In this research, an ETD29 core was selected due to its characteristics of small size and low losses. And the selected material is N87 from TDK. Table 5-1 provides the information related to the selected core and material.

Table 5-1 ETD29 and N87 material information

Effective length l_e/mm	70.4
Effective area A_e/mm^2	76.0
Effective volume V_e/mm^2	5350
Average turn length l_n/mm	52.8
Winding area A_w/mm^2	97
Outer arm length l_o/mm	53.5
Outer arm area A_o/mm^2	42.1
Center arm length l_c/mm	26.7
Center arm area A_c/mm^2	75.4
Brauer's model parameters	k_1=0.062 k_2=42.995 k_3=302.904
Optimum frequency range/kHz	25-500

3) Flux density

It is noteworthy to mention that the flux density inside the material is related to the core losses. Besides, the ac component of the flux density will produce an instantaneous inductance variation around the operation point. Therefore, the higher the ac flux density, the higher the inductance change. In this research, the flux density equals to 200mT is selected. And the expected core losses can be calculated based on the datasheet as shown in Figure 5-4, which is about 2.05W at 100°C.

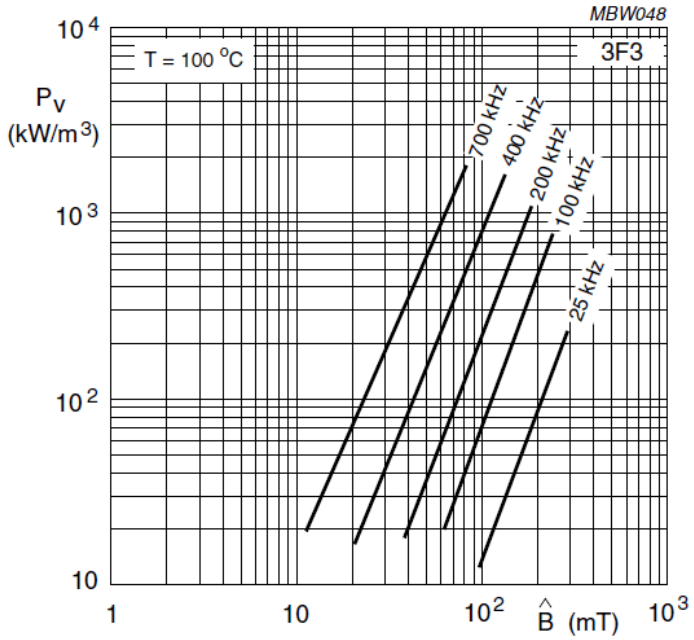


Figure 5-4 Typical core loss data.

4) Number of turns

Now, the turns of the main winding can be calculated according to the following expression:

$$N_p = \frac{L_{\max}\hat{I}}{\hat{B}A_e} = \frac{240\times 7}{0.2\times 76} = 110 \tag{5-1}$$

And the airgap can be calculated by using the following expression:

$$l_g \approx \mu_0 A_e \frac{N_p^{\,2}}{L_{\max}} = 4.9mm \tag{5-2}$$

5) Control Winding

For the control winding, since the dc bias current is relatively small (the maximum dc bias current is around 1A), a 0.2mm diameter wire with turns ratio NDC=80 are selected.

5.3 Spice Modeling of The Variable Inductor

In this part, the Spice model of the variable inductor is discussed; and the structure is simulated in

LTspice, the simulation results agree with the theoretical analysis. For a variable inductor, it is composed of the following components: airgap, linear reluctor, nonlinear reluctor and winding [41]. The description for each component is discussed.

1) Airgap

Conventionally, the airgap can be modeled as a resistor. Its value is corresponding to the reluctance value. The airgap is characterized by its length (l_g), area (A_g), and fringing factor (v_g). It can be expressed as

$$\mathfrak{R}_a = \frac{l_g}{\mu_0 A_g v_g} \tag{5-3}$$

where $\mu_0 = 4\pi 10^{-7}\,\mathrm{H/m}$ is the permeability of the free space.

2) Linear reluctor

Most of the case, linear reluctor can be used to model a linear magnetic material without considering saturation effect. It is similar to airgap, which can be modeled as a resistor. However, its value is related to its length (l_o), area (A_o), relative permeability (μ_r), fringing factor (v_o). It can be defined as

$$\mathfrak{R}_l = \frac{l_o}{\mu_r \mu_0 A_0 v_0} \tag{5-4}$$

3) Nonlinear reluctor

It is used to model a magnetic material section including the B-H curve behavior. It is characterized by its length (l_m), area (A_m), and the magnetic material parameters k_1, k_2, k_3 that model the B-H curve according to Brauer's equation. The reluctance of this type element can be expressed as

$$\mathfrak{R}_m(B) = \frac{l_m}{\mu_d(B) A_m} \tag{5-5}$$

where $\mu_d(B)$ is the absolute differential permeability of the material, expressed as a function of the magnetic flux density.

According to Brauer's equation, for N87 material, $\mu_d(B)$ can be expressed as

$$\mu_d(B) = \frac{dB}{dH} = [k_1(1+2k_2B^2)e^{k_2B^2} + k_3]^{-1} \tag{5-6}$$

According to [41], Figure 5-5 shows a comparison results between manufacture's datasheet information and Brauer's model for N87 material. It can be seen that the maximum error is obtained at B=0.3T, the value is about 26%

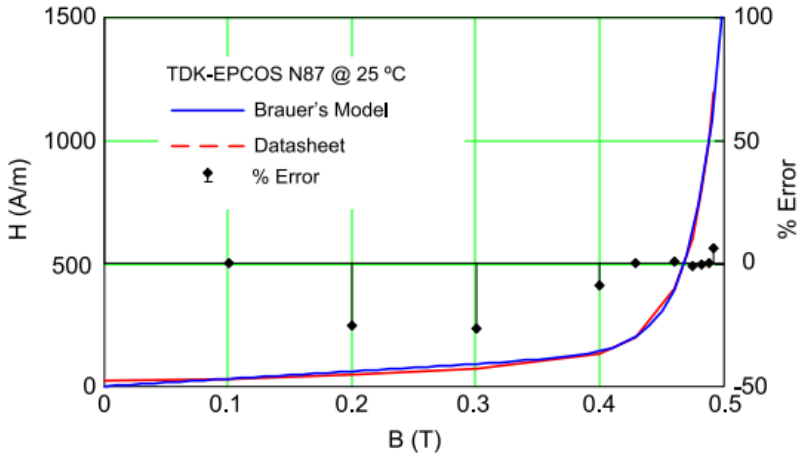


Figure 5-5 Comparison between datasheet information and Brauer's model [41].

4) Winding

It is used to model the interaction between the electric and magnetic parts of the system. It has only one parameter, which is the turns of the winding. Ignoring the losses, the winding model can be expressed as

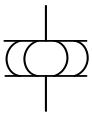
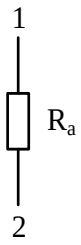
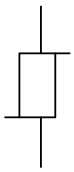
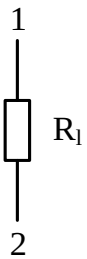
$$F_w(t) = N_w \cdot i_w(t) \tag{5-7}$$

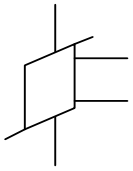
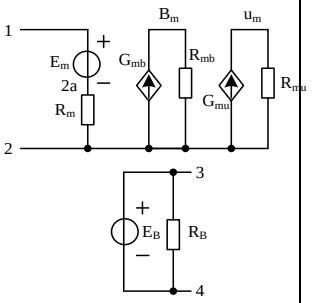
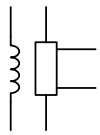
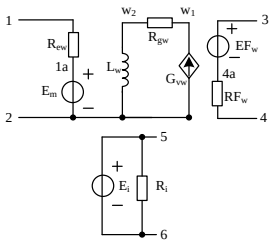
$$v_w(t) = N_w \cdot \frac{d\phi_w(t)}{dt} = N_w A_w \frac{dB_w(t)}{dt} \tag{5-8}$$

where F_w is the magnetomotive force (MMF) created by the winding inside the magnetic core, N_w is the turns of the winding, v_w and i_w are the winding voltage and current respectively, ϕ_w and B_w are the magnetic flux and magnetic flux density respectively, A_w is the area of the core.

The detailed description of each element are summarized in Table 5-2, including symbol in LTspice, equivalent circuit and Spice model [41].

Table 5-2 Spice model and LTspice symbol of the components [41].

Ltspice symbol and name	Equivalent circuit	Spice model
 Airgap		;Airgap .subckt airgap 1 2 ;vg, fringing factor ;lg, length ;Ag, area .param pi=3.1415926 .param u0=4*pi*1e-7 Rg 1 2 {lg/(u0*Ag*vg)} .ends airgap
 Linear reluctor		;Linear reluctor .subckt reluctor 1 2 ;vo, fringing factor ;lo, length ;Ao, area .param pi=3.1415926 .param u0=4*pi*1e-7 Rr 1 2 {lo/(u0*ur*Ao*vo)} .ends reluctor

 Nonlinear reluctor		;NON-LINEAR RELUCTOR .subckt nonreluctor1 1 2 3 4 ;2,positive mmf pin ;1, negative mmf pin ;3, 4, B output ;k1, k2, k3, material coefficients .func ud(B) {1/(k1*(1+2*k2*B*B)*exp(k2*B*B)+k3)} Em 1 2a value={(lm1/(V(um,2)*Am2))*I(Em)} Rm 2a 2 1m; small resistance to avoid voltage loop Gmb 2 Bm value={I(Em)/Am1} Rbm Bm 2 1 Gmu 2 um value ={ud(V(Bm,2))} Rmu um 2 1 EB 3 4 value={V(Bm,2)} RB 3 4 10k .ends nonreluctor
 Winding		;WINDING .subckt winding1 1 2 3 4 5 6 ;1,2 electric pins ;3,4 magnetic pins ;5,6 inductance value pins ;Nw1, number of turn EFw 3 4a value={Nw1*I(EVw)} RFw 4a 4 1m GVw 2 w1 value={-I(EFw)} Rgw w1 w2 1m Lw w2 2 {Nw1} EVw 1a 2 value={V(w2,2)} Rew 1 1a 1m Ei 5 6 value={-Nw1*I(EFw)/I(EVw)} Ri 5 6 10k .ends winding

Based on the components discussed above, the variable inductor can be easily implemented in LTspice as shown in Figure 5-6. It can be seen that the model contains three nonlinear reluctors to represent the left, center and right arms, an airgap element is used to model the airgap in the center

arm, and three windings to model the left, center and right wingdings respectively. In addition, a linear reluctor is used to model the leakage flux that is not shared by main and auxiliary windings, which provides increased accuracy to the model especially at high bias currents.

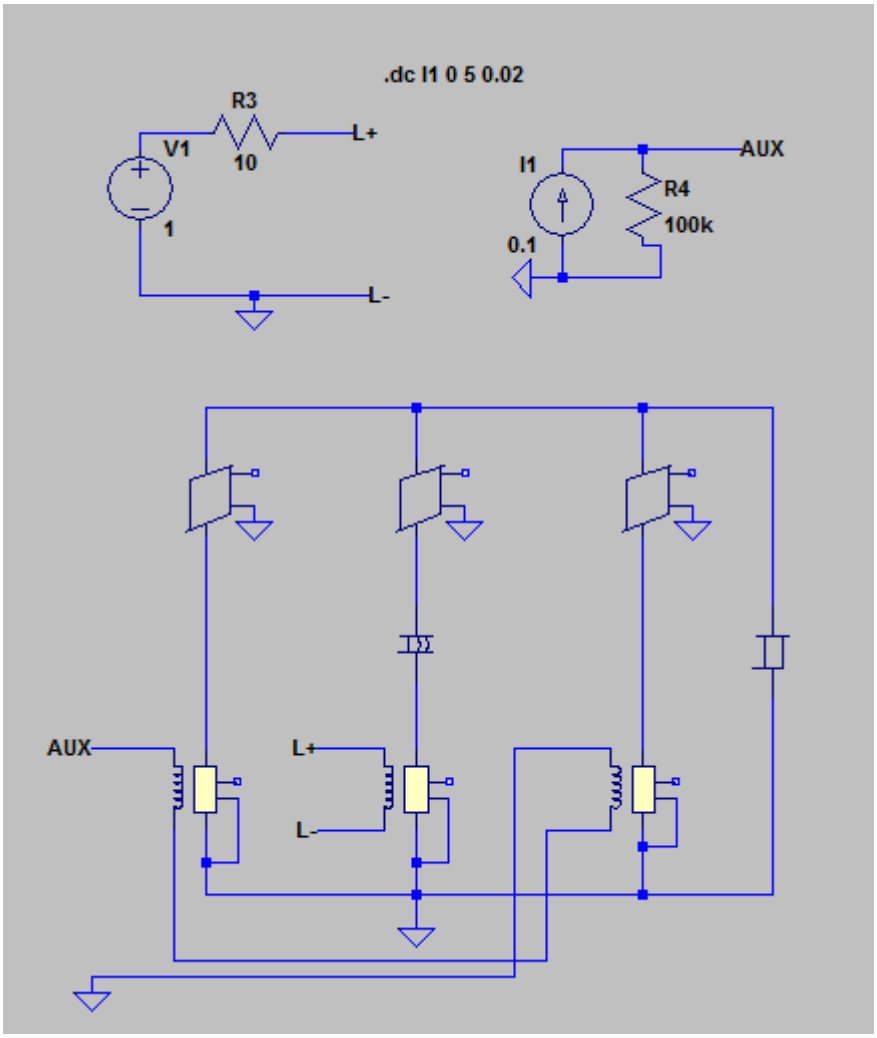


Figure 5-6 Variable inductor model implemented in LTspice.

The dc bias current ranges from 0A to 1.5A, and Figure 5-7 shows the characteristic of variable inductance versus the dc bias current. It can be seen that the inductance value is decreasing with the increase of the dc bias current, and the inductance range is from 35uH to 250uH.

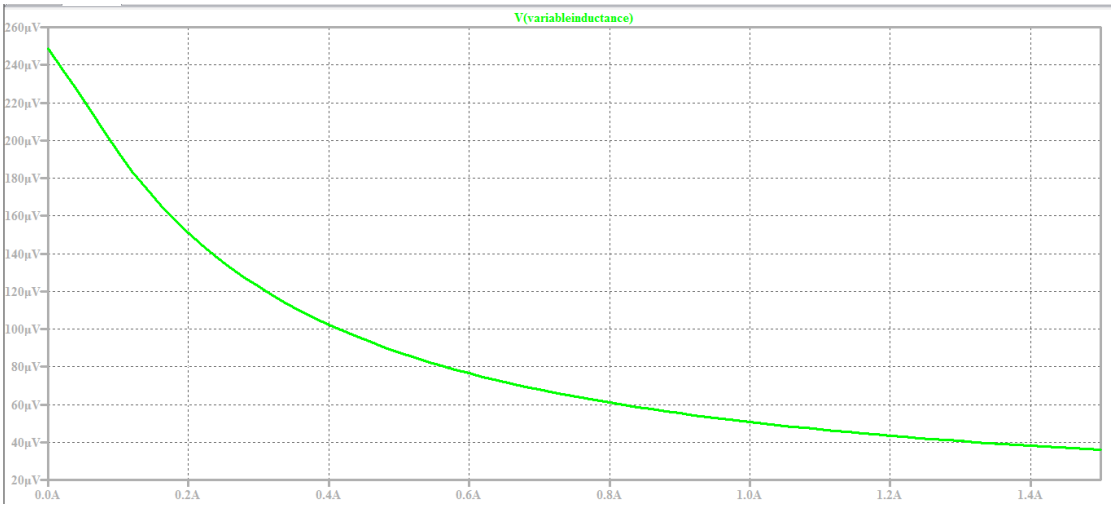


Figure 5-7 Simulation results for the variable inductor.

5.4 Summary

In this chapter, the magnetic control scheme is introduced. Firstly, the operation principle and structure are discussed. Then the design considerations for the variable inductor of the proposed topology are presented. Moreover, the Spice model for the variable inductor is obtained, and the simulation is implemented in LTspice. The estimated power loss is about 2.5W, which is acceptable for 3.3kW operation.

Chapter 6 Conclusions and Future Work

This thesis proposed a high frequency, high efficiency and high power factor battery charger for EVs and PHEVs. The proposed topology is composed of an interleaved totem-pole bridgeless PFC and two LLC resonant converters. The operation principles, analysis, and design considerations are presented in detail. High power factor is achieved by using bridgeless PFC technology, from the simulation results, the power factor is greater than 0.98 during the whole operation range; high efficiency characteristic is obtained due to the small reverse recovery charger of SiC MOSFETs in PFC unit, and ZVS and ZCS operation for primary switches and secondary diodes respectively. Since the interleaved technology for PFC unit and two LLC resonant converters are adopted, the system power level can be improved. The modeling and simulation for the variable inductor are implemented in LTspice. Furthermore, the simulation results agree with the theoretical analysis. Therefore, hardware implementation and experimental validation are the focus of the future work.

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