

May 2019

A State Evaluation Method for Solder Layer in MOSFET

Zhenyu Deng
University of Wisconsin-Milwaukee

Follow this and additional works at: <https://dc.uwm.edu/etd>



Part of the [Electrical and Electronics Commons](#)

Recommended Citation

Deng, Zhenyu, "A State Evaluation Method for Solder Layer in MOSFET" (2019). *Theses and Dissertations*. 2172.

<https://dc.uwm.edu/etd/2172>

This Thesis is brought to you for free and open access by UWM Digital Commons. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of UWM Digital Commons. For more information, please contact open-access@uwm.edu.

A STATE EVALUATION METHOD FOR SOLDER
LAYER IN MOSFET

by

Zhenyu Deng

A Thesis Submitted in
Partial Fulfillment of the
Requirements for the Degree of

Master of Science
in Engineering

at

The University of Wisconsin-Milwaukee

May 2019

ABSTRACT

A STATE EVALUATION METHOD FOR SOLDER LAYER IN MOSFET

by

Zhenyu Deng

The University of Wisconsin-Milwaukee, 2019

Under the Supervision of Professor Adel Nasiri

MOSFET is the core component in power equipment. It is widely used in electrical vehicles (EV), wind generation, rail transit and so on. The long-term impact of temperature and stress cause fatigue in the device during operation. Because of the low melting point of 96.5Sn3.5Ag, solder layer aging and failure is one of the main failure modes. So, it is important to figure out the failure mechanism and the effects of defects in the solder layer.

A finite element (FE) model considered the temperature dependence of materials was built in COMSOL software to support the subsequent studies. Effects of voids in solder layer and fatigue are studied and analyzed based on the FE model. The results show the junction temperature, case temperature, on-resistance and thermal resistance between junction and case increase with the rise of voids' areas and fatigue degree. Besides that, all of them have a similar trend, which means on-resistance can be a criterion for thorough failure replacing the thermal resistance. And the on-resistance is more sensitive than thermal resistance because its growth rate is much higher than that of thermal resistance.

Based on the simulation and analyzed, on-resistance, case temperature and on-current were selected as the characteristic parameter to reflect the healthy state of MOSFET. They were used as the inputs for the evaluation model. And the growth rate of on-resistance was chosen as the output parameter. Combine the failure rate curve, the range from health to thorough failure was be divided into five pieces with different intervals. For evaluation, adaptive neuro-fuzzy inference system (ANFIS) was adopted to establish the model. By validation and comparing with some common classification algorithms, it was verified and

showed high accuracy.

© Copyright by Zhenyu Deng, 2019
All Rights Reserved

TABLE OF CONTENTS

ABSTRACT	II
LIST OF FIGURES	VII
LIST OF TABLES.....	IX
CHAPTER 1 INTRODUCTION	1
1.1 BACKGROUND	1
1.2 LITERATURE REVIEW	2
1.2.1 Researches about Failure Mechanism	2
1.2.2 Researches about State Monitoring and Evaluation Methods	5
1.3 DISSERTATION OBJECTIVES AND OUTLINE	6
CHAPTER 2 MULTIPHYSICS FIELDS COUPLING AND FE MODEL.....	8
2.1 INTRODUCTION	8
2.2 FIELDS COUPLING MODEL FOR MOSFET	9
2.2.1 Package Structure of MOSFET	9
2.2.2 Thermal and Mechanical Features	12
2.2.3 Multiphysics Fields Coupling and Solving Process	13
2.3 FE MODEL BUILDING AND VALIDATION	16
2.3.1 Setting for Material Parameters	16
2.3.2 Boundary Conditions.....	18
2.3.3 Validation of the FE Model.....	19
CHAPTER 3 MOSFET'S FAILURE MODES AND CHARACTERISTICS ANALYSIS	22
3.1 EFFECTS OF VOIDS IN SOLDER LAYER	22
3.1.1 Voids in Solder Layer Center	23
3.1.2 Voids in Solder Layer Edges.....	27
3.2 EFFECTS OF SOLDER LAYER FATIGUE.....	30
3.3 FAILURE MECHANISM ANALYSIS OF SOLDER LAYER.....	32
3.4 THERMAL NETWORK MODELS AND PARAMETERS SELECTION	35
3.4.1 Thermal Network Models.....	35
3.4.2 Parameters Selection and Sensitivity Analysis	36
CHAPTER 4 STATE EVALUATION MODEL FOR MOSFET	39
4.1 ANFIS ALGORITHM AND STRUCTURE	40
4.2 EVALUATION MODEL BASED ON ANFIS	41
4.2.1 Data for Machine Learning.....	41

4.2.2	Rules for Classification Intervals	42
4.2.3	Structure of the Model.....	44
4.3	RESULTS ANALYSIS AND COMPARISON	45
4.3.1	Results Analysis	45
4.3.2	Comparison of Common Classification Algorithms in Matlab.....	46
CHAPTER 5 CONCLUSION.....		49
5.1	SUGGESTION FOR FUTURE WORK.....	49
REFERENCES.....		51

LIST OF FIGURES

Figure 1.1 Failure Rate of Components in Converter	1
Figure 2.1 Framework for Research in Chapter 2	8
Figure 2.2 Sectional View of MOSFET's Structure	10
Figure 2.3 Materials' CTE Difference.....	10
Figure 2.4 Coupling Effect of Multiphysics Fields.....	14
Figure 2.5 Analysis Flowchart of Coupling Model	14
Figure 2.6 MOSFET and Model in COMSOL	15
Figure 2.7 Meshing Controlled by Multiphysics Fields (Case hidden)	20
Figure 2.8 Normalized On-resistance from Datasheet.....	20
Figure 2.9 Normalized On-resistance Obtained from FE Model	21
Figure 3.1 Initial Voids under X-ray[36].....	23
Figure 3.2 Temperature Distribution under Different Center Voids Ratios (Units: °C).....	24
Figure 3.3 Junction and Case Temperature with Different Void's Area.....	26
Figure 3.4 On-resistance and Thermal Resistance with Different Void's Area.....	26
Figure 3.5 Growth Rates of On-resistance and Thermal.....	26
Figure 3.6 Temperature Distribution of Die with Different Center Voids Area	27
Figure 3.7 Diagram of Voids in Edges	27
Figure 3.8 Junction and Case Temperature with Different Edge Voids' Area.....	28
Figure 3.9 On-resistance and Thermal Resistance with Different Edge Voids' Area	28
Figure 3.10 Growth Rates of On-resistance and Thermal.....	29
Figure 3.11 Temperature Distribution of Die with Different Edge Voids' Area (Units:°C)....	29
Figure 3.12 Junction and Case Temperature with Different Fatigue Degree	31
Figure 3.13 On-resistance and Thermal Resistance with Different Fatigue Degree	31
Figure 3.14 Growth Rates of On-resistance and Thermal.....	31

Figure 3.15 Temperature Distribution of Die with Different Fatigue Degree (Units:°C)	32
Figure 3.16 3-D Temperature Distribution and Sectional View	33
Figure 3.17 Von Mises Stress Distributions of Solder Layer	34
Figure 3.18 Junction and Case Temperatures under Cyclic Power.....	34
Figure 3.19 Solder Layer Strain under Cyclic Power	35
Figure 3.20 Trend of Solder Layer and Von Mises Stress with T_j	35
Figure 3.21 Thermal Network Models	36
Figure 3.22 Relationship between R_{on} and Z_{jc} in Different Aging Modes	37
Figure 4.1 State Assessment Structure Diagram.....	39
Figure 4.2 The Structure of ANFIS.....	40
Figure 4.3 Failure Rate Curve	43
Figure 4.4 Flow Chart of the Evaluation Model.....	44
Figure 4.5 RMSE during Training	45
Figure 4.6 Error between Predicted and Tested Data.....	45
Figure 4.7 Results of Aging Degree	46
Figure 4.8 Confusion Matrix of the Model Output.....	46
Figure 4.9 Confusion Matrixes of Common Classification Algorithms	47

LIST OF TABLES

Table 2.1 Geometry Parameters of Different Parts	16
Table 2.2 Properties of Materials	17
Table 2.3 96.5Sn3.5Ag Solder Parameters for Anand Model	18
Table 3.1 Simulation Results with Different Voids Area in Solder Layer Center	25
Table 3.2 Simulation Results with Different Edge Voids in Solder Layer	28
Table 3.3 Simulation Results with Different Fatigue Degrees of Solder Layer	30
Table 4.1 Classification Intervals for Healthy State	43
Table 4.2 Healthy Condition of Characteristic Parameters	44
Table 4.3 Results of the Common Classification Algorithms	48

ACKNOWLEDGMENTS

Firstly, I would like to express my sincere gratitude to my advisor, Pro. Adel Nasiri, for his kindness action accepting me to be one of the members in his lab. He is intelligent and always gives great guidance to solve problems. Throughout my study here, he can always give his professional guidance on my research. Moreover, he influenced me with his rigorous attitude, unwavering commitment, and broad knowledge in performing high-level research. Also, he is a kind and considerate mentor, he always ordered pizza and drinks for us if the group meeting extends to noon. I am pretty lucky to have him as my advisor.

I am grateful to Dr. David Yu and Seyed Hosseini for sparing time to be my committee member and gave me comments on my thesis. They are all experts in their academic fields and have great contributions. Besides, Dr. Yu gave me so much help when I just came to the University of Wisconsin- Milwaukee.

In addition, I want to thank Dr. Robert Cuzner for giving me so many advices and helping me figure out some questions during our group meeting. Also thanks to Fanglve Ju for his help and suggestion during my studying in UWM. Special thanks go to Betty Warras, Gary, Yang Zhang and Chris Jin for their help during my study here.

Finally, I would like to thank my family for their care and encouragement in the past years and their confidence in me.

Chapter 1 INTRODUCTION

1.1 Background

Power converters are key units in electricity conversion, control and transmission. They are widely used in renewable energy power generation, rail transit, aerospace, electric vehicle (EV) and other fields [1]. Its safety and reliability are important for the efficient use of renewable energy.

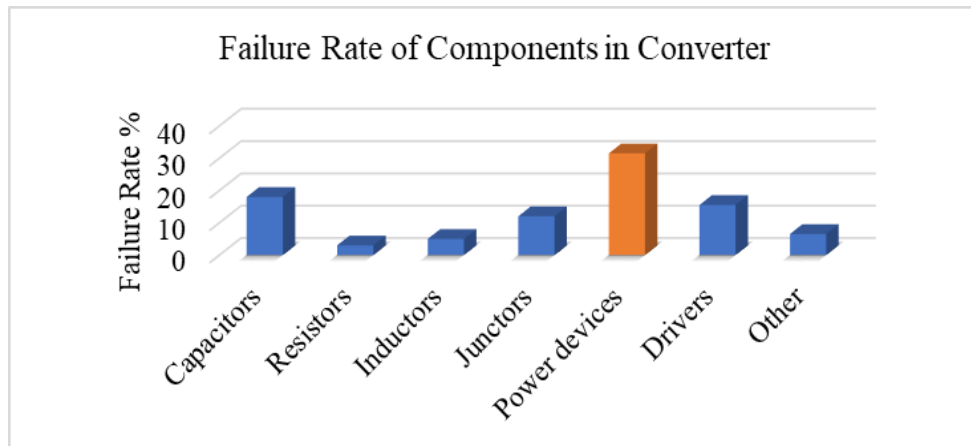


Figure 1.1 Failure Rate of Components in Converter

Research shows that the ratio of power converter failure to electrical equipment failure in renewable energy generation grid-connected systems is as high as 15% [2]. And the power device is one of the core components in the converter. As shown in Figure 1.1, the failure rate of power devices is the highest, which is more than 30% and twice more than the second, capacitors [3]. According to statistics, E. Wolfgang et al. pointed out that industrial economic losses due to power device failure account for at least half of the total system cost [4]. Among them, the failure rate of power device and PCB is as high as 50%. And the second, capacitor, accounts for around 16%. At the same time, the safety and the reliability of power devices still have a large gap compared with users' requirements, especially in the field of high-reliability requirements such as military and aerospace. Therefore, how to improve the reliability of power

devices reasonably and effectively plays an important role in the power devices' safety and reliable operation when they are used in drivers and renewable energy.

1.2 Literature Review

1.2.1 Researches about Failure Mechanism

I. Aging Failure

The aging failure of MOSFET devices involves many factors such as electricity, heat, and stress. And they are closely related to each other. The aging mode of MOSFET devices can be divided into two categories: parameter drift and structure aging.

Typical structure failures include chip failures, fatigue and aging of solder layers, and drop of bond wires. The main reason is the mismatch of coefficient of thermal expansion (CTE) of different materials. There is always temperature change on devices during operation. Especially, some devices work in a harsh environment, which may cause a huge temperature fluctuation on devices. When the devices subjected to temperature change, there are thermomechanical stresses between different materials [5]. With the rapid development of power electronic devices under market demand, they are gradually developing towards modularization and integration. Therefore, thermomechanical stress caused by heat generation of power devices becomes an important problem. It is generally believed that thermal fatigue is a major factor in the aging failure of devices.

There are a series of studies about structure failure mechanism, focusing on electro-thermal and thermal parts. The literature [6-7] pointed out that the voids, cracks and delamination of the solder layer will cause the heat transfer channel of the device to be blocked. The heat generated by itself is not able to dissipate in time. And the junction temperature is at a high value for a long time, which accelerates the aging process of the device and reduces reliability. The literature [8] shows that the fatigue degree of the solder layer is positively correlated with the junction-case thermal resistance (Z_{jc}) of the power device in steady-state.

Usually, the initial crack appeared at solder layer's edge and gradually spreads to the central region under the concentration action of thermal stress. Eventually, the solder layer is detached, causing irreversible damage to the structure.

II. Research Methods

At present, there are two methods widely used by researchers around the world. They are accelerated life testing and the finite element (FE) method.

A. Accelerated Life Testing

The period of natural aging failure of power devices is so long, which makes it impossible to meet the requirements of production and scientific research. For power devices, the widely used accelerated tests have two major types of cycle tests, power and temperature. The temperature cycle test causes the device temperature to fluctuate by externally loading the temperature shock, simulating the thermal shock of the device in actual work. The power cycle is to load a periodic current into the device so that the chip can generate heat by itself and cause thermal shocks. This test can effectively simulate the process of active heating of the chip layer, which is closer to the actual working conditions. It can be used to detect the solder layer's performance and the thermal interaction between different layers.

Literature [9] analyzed the failure mechanism of IGBT modules, the aging evolution process and the trend of characteristic parameters. The results show that the damage accumulation process and the alteration of thermal resistance of the power device are nonlinear. According to the literature [10-12], the thermal resistance of the device raise obviously and cracks appear in the solder layer when the junction temperature fluctuation is small. When the fluctuation of junction temperature $\Delta T_j \geq 100^\circ\text{C}$, the bond wires lift-off becomes the main form of the device's failure.

Combined with accelerated aging test and statistics, a number of power device life prediction models are proposed. Coffin-Manson model [13], Bayere model [11] and Norris-

Landzberg model [14] are analytical models widely used. The Bayere model considers the test parameters more comprehensive, including junction temperature fluctuations, maximum junction temperature, load current, and blocking voltage [11]. The physical life model based on internal fatigue and mechanical properties of materials mainly includes the model based on plastic strain and creep strain [15], the model based on fracture parameters [16], and the energy-based fatigue model [17]. Based on the temperature cycle test, the literature [9] improved the Coffin-Manson model and established a segmentation evaluation model for the reliability of the device considering the fatigue accumulation effect of the solder layer and the sustained impact of the small amplitude temperature. The life prediction model requires clear parameters and a large number of samples. Some parameters are more complicated to acquire. When the actual operating conditions change greatly, the evaluation model has a large error.

B. Researches based on FE

Finite element analysis is an approximate numerical analysis method for simulating complex engineering applications and actual physical systems. Reliability modeling based on FE method can quantitatively simulate the manufacturing process of device and complex working environment, which greatly reduces the cost in research and development, parameter optimization and testing. Currently, commercial software commonly used in multiphysics simulation modeling are COMSOL Multiphysics, ANSYS and ABAQUS. Among them, COMSOL provides a multiphysics interface for industrial applications such as electrical field, thermal field, stress field, chemical and other fields for a different profession.

In [18], ANSYS was used to establish the electro-thermal coupling model of power MOSFET. And the corresponding relationship between environmental conditions (temperature, humidity, etc.) and aging failure of MOSFET devices was proposed. In [19], based on the electro-thermal fields coupling FE method, the relationship between the temperature and the failure degree of solder layer is analyzed. Due to the complex structure of the power device,

most of the FE models do not consider the size of the actual research objects, the dependence of the material parameters on the temperature and the viscoplasticity of the solder layer. The results of those simulations may have large errors.

1.2.2 Researches about State Monitoring and Evaluation Methods

At present, the monitoring and evaluation methods on the health status of power devices are mainly based on three aspects: based on electrical and thermal characteristics, based on sensor technology and based on the reliability model. Condition monitoring technology is able to capture the weak features that are hidden in large amounts of data and diagnose the aging degree of the device. Condition monitoring and evaluation is the basis for overhaul. Based on timely and accurate assessment and prediction, it can enhance the pertinence and effectiveness of maintenance which can improve the reliability of system operation and comprehensive economic benefits.

I. Evaluation Methods based on Electric and Thermal Parameters

The device is subjected to temperature and stress for a long time during operation. Because of the cumulative effect of damage, the fatigue of the solder layer is aged or the bond wires are detached, which causes changes in the device characteristics such as electrical and thermal parameters [20-21].

Literature [22] and [23] use conduction voltage drop as an indicator of power devices for health status detection. In [24], a real-time failure prediction system for IGBTs in EVs is proposed by monitoring V_{on} changes.

The fatigue in the solder layer will cause Z_{th} to rise. The monitoring technology based on the thermal parameters can reflect the aging state of the solder layer. The increase of the thermal resistance is generally regarded as a criterion for solder layer failure. It is believed that a 20% increase in Z_{th} can define the failure of the solder layer [15]. Literature [2] shows that the failure of the solder layer can modify the electrical and thermal parameters such as the conduction

voltage drop and power loss associated with the thermal resistance and junction temperature. The literature [25] discuss the effect of solder layer aging on the thermal-mechanical performance of IGBT modules and propose a failure monitoring method based on statistical characteristics of temperature gradients. Literature [26] shows that some failure mechanisms can extend the switching time. Since most of the power devices are packaged inside the module, the thermal parameters such as Z_{th} and T_j cannot be directly measured, which cannot meet the requirements of real-time monitoring.

II. State Evaluation Models

The development and application of big data technology provide new ideas for state evaluation and reliability analysis of power devices. Literature [27] proposed a state evaluation model for IGBT modules based on GA-BP algorithm. It diagnoses anomalies by taking the electrical parameters as inputs and the case temperature as an output. However, there are numerous factors that can affect the case temperature such as environment temperature and aging heatsink. Literature [28] proposed an algorithm based on static neural network to monitor the condition of devices in a full-bridge rectifier. It compares the difference between the theoretical value and the measured value to achieve the evaluation.

In summary, the evaluation method based on electrical and thermal characteristics is not easy to achieve online measurement. The sensor-based evaluation methods need to comprehensively consider the measurement error, the isolation of the detection circuit and the impact on the structure. The reliability model-based method is closely related to operating conditions such as temperature, current and load.

1.3 Dissertation Objectives and Outline

In this dissertation, some of the aging characterization and state evaluation issues are addressed. The detailed process for structuring a state evaluation with easier monitoring and high accuracy are following.

The structure of MOSFET and steps for building an FE model considering the dependence

of some properties on the temperature in COMSOL software will be discussed in Chapter 2.

In Chapter 3, the effects of voids in different locations of the solder layer will be simulated and analyzed. The aging process of the solder layer and its effects will be discussed. The variety of characteristic parameters and their sensitivities under defects or fatigue in the solder layer will be compared.

Chapter 4 shows the structure of the state evaluation model based on ANFIS. Rules for healthy state classification will be discussed. The results of the model established in this thesis and other common classification algorithms will be compared at last.

Chapter 5 summarizes the research work and provides suggestions to improve the model in future research.

Chapter 2 Multiphysics Fields Coupling and FE Model

2.1 Introduction

Power devices are the core components of aerospace, wind power, subway traction and other practical operating systems. In actual operation, due to the power loss of the chip, the device suffers from long-term cyclic fluctuations in power and temperature. Because of the mismatch of the CTEs of each layer, the fluctuation of temperature produces alternating thermal stress. Under the long-term effect of temperature and stress, fatigue in the solder layer is accumulated, which leads to solder layer aging. Therefore, there are multiple physic fields that can affect the healthy state of the device in the actual operation. Most of the existing researches on the electrical, thermal and mechanical properties are mainly based on the simulation with a simplified model or the single physic field. The interaction between different fields is not considered. Model building on multiphysics fields coupling may give more accurate analysis on defects, aging process and failure mechanism.

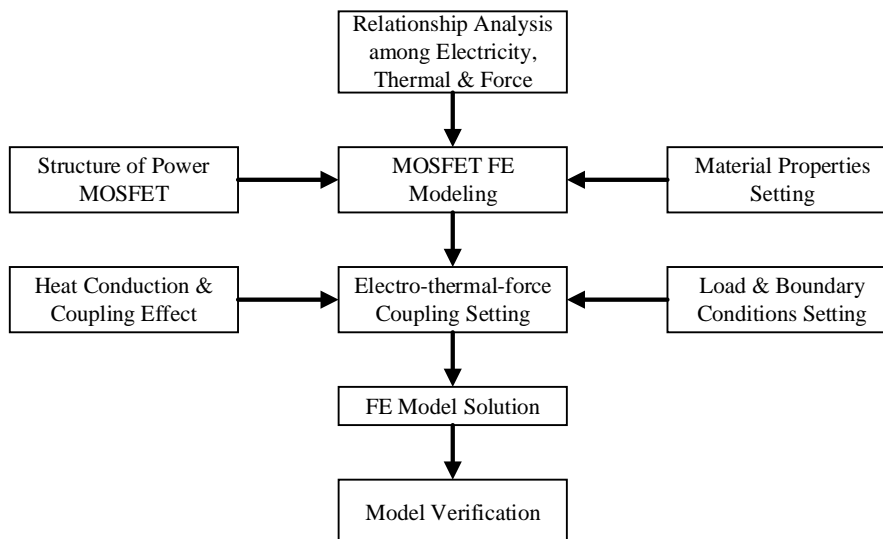


Figure 2.1 Framework for Research in Chapter 2

In this chapter, a simulation model of the MOSFET has been established in COMSOL

software. The coupling relationship between the electrical and thermal fields is analyzed. And the temperature dependence of the materials and the viscoplasticity are considered in the simulation. Finally, the validity of the model is verified, which can ensure accurate simulation for subsequent researches. The process is shown in

Figure 2.1.

2.2 Fields Coupling Model for MOSFET

2.2.1 Package Structure of MOSFET

The internal package structure of MOSFET is shown in Figure 2.2. We can see that the device is formed by stacking various components, including bond wires, metal film layers, chips, solder layers, copper layers and epoxy resin shell and other components.

I. Solder layer

It fixes the chip on the copper layer and provides a crucial path for the heat dissipation of the chip. 96.5Sn3.5Ag-based lead-free solder is widely used. It has several advantages like heat reliability, long life and environmentally friendly. With the rapid development of the welding, the silver sintering technology has gradually replaced the traditional soldering technology [29]. The sintered connecting layer is made of silver material, which has a high melting point and greatly improves the electrical and thermal conductivity of the device. It has become a high-reliability soldering technology in the power module package.

II. Chip Layer

On top of the solder layer, it is the core component of the entire MOSFET device. At present, most manufacturers use silicon materials to manufacture chips.

III. Metal Film Layer

In the production process of the chip, the conductive metal film with a thickness of 3~5 μ m is formed on the silicon wafer by a deposition method, called metallization. It has a high step-

covering ability and strong adhesion to the substrate. And the connection between metal and silicon can form a lower barrier and reduce the contact resistance of the device, which results in a significant decrease in the on-resistance.

IV. Bond Wires

Bond wires realize electrical connection and extraction between the electrodes and the chip. They connect the chip to the pins wire bonding and realize the current sharing by connecting a plurality of leads in parallel.

Different components are made from different materials, so they have different thermal expansion coefficients (CTE). Figure 2.3 shows their CTEs and the differences of the contacting layers.

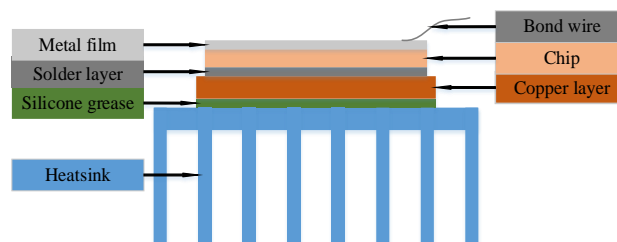


Figure 2.2 Sectional View of MOSFET's Structure

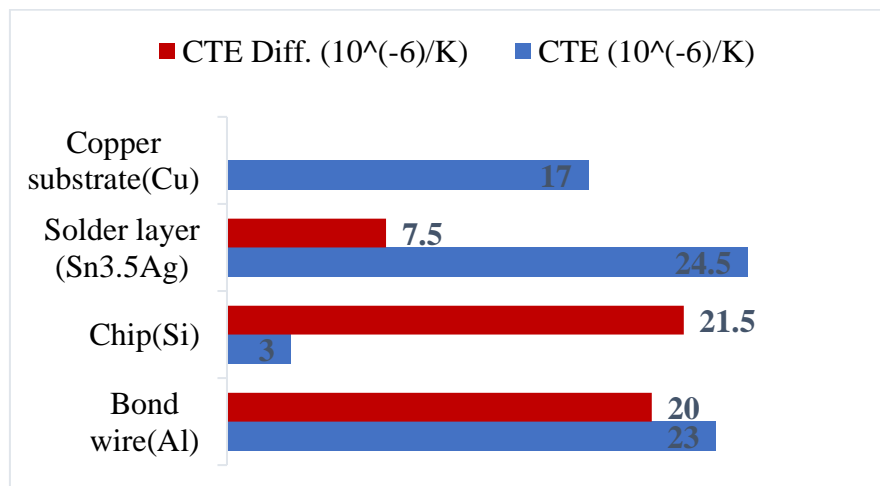


Figure 2.3 Materials' CTE Difference

In order to reduce the cost, the bond wires are basically connected by aluminum leads. If we want to reduce the conduction loss and increase the heat dissipation capability, we can only increase the area of wire or the number of wires. The increase in the number of wires causes

various parasitic effects. In recent years, with the continuous improvement of process technology, devices are shifting to miniaturization and integration. And the parasitic effects such as crosstalk signals, voltage drops, and transmission line effects are becoming more and more obvious. In the actual operation, MOSFET device operates at a high switching frequency and a large on-current. The heat generated by the device causes the junction temperature to rise. The heat is partially passed through the solder layer, the copper base to the heat sink. The heat sink dissipates most of the heat into the surrounding environment. The other way to dissipate heat is to transfer it along the wires through the pins to the PCB.

According to the datasheet of IXFK80N60P3, the range of the junction temperature of this device is $-55^{\circ}\text{C}\sim 150^{\circ}\text{C}$ in operation. As we can be seen from Figure 2.2, the differences in CTEs between the bond wire and the solder layer contacting with the chip are larger than others. If we assume the temperature of 100°C , the difference in thermal expansion between the die and the bond wire is 7463 ppm^1 , and the value between the chip and the solder layer is 8022.7 ppm . The higher temperature of the power device, the greater the difference in thermal expansion between materials, which is the root cause of failure in the package level of the power device. Under the long-term impact of alternating temperature and current, the bond wire and the solder layer generate alternating thermal stress due to the mismatch of CTEs, resulting in thermal fatigue of the solder layer material, deformation, delamination, and failure. When the solder layer is fatigued, the area for heat transfer between the chip and the package case is greatly reduced. Then, the main heat dissipation path is destroyed, which results in a large amount of heat accumulation at the chip and cannot be effectively dissipated in time. So that the bond wire and the chip are weak. The values of compression and stretching of the thermal stress at the weak points increases. Eventually, it will lead to the peeling and detachment of the bond wires, which causes the power device fails.

¹ Part per million.

2.2.2 Thermal and Mechanical Features

According to statistics, around 55% of failure is caused by a high temperature [30]. Most of the heat generated by the chip transfer to heat sink through the solder layer and the copper baseplate. The process of the inner heat dissipation can be described by the follow equation:

$$\rho c \frac{\partial T}{\partial t} + \nabla \cdot (\lambda \nabla T) = Q + q_s T \quad (2.1)$$

Where ρ is the density of material; c is the heat capacity; λ is the thermal conductivity; Q is the total heat; q_s is the absorption coefficient.

The material undergoes thermal expansion under the action of temperature. At a certain temperature T , the strain caused by the thermal expansion of each layer inside the module can be presented by the equation:

$$\varepsilon = \alpha \times (T - T_{\text{ref}}) \quad (2.2)$$

Where α is the CTE. T_{ref} is the reference temperature. ε is the strain vector.

According to Figure 2.3, we can know the CTEs are different between layers. And the temperature distribution is uneven. So there is thermal stress inside the device. It can be calculated by:

$$\sigma = D \times (\varepsilon_{\text{total}} - \varepsilon) \quad (2.3)$$

Where σ is the stress vector. D is the elastic stiffness matrix. $\varepsilon_{\text{total}}$ is the total strain vector.

Different from other materials, the solder layer has a low melting point (around 221 °C). In addition to elastic deformation, it also has obvious viscoplasticity which relates to temperature and operating time. The Anand model was widely used to describe the property [31]:

$$\dot{\varepsilon}^{in} = A \left[\sinh \left(\xi \frac{\sigma}{s} \right) \right]^{\frac{1}{m}} e^{-\frac{Q}{RT}} \quad (2.4)$$

Where $\dot{\varepsilon}^{in}$ is the inelastic strain rate, ξ is a multiplier of stress, σ is the applied stress, s

is a single scalar as an internal variable to represent the averaged isotropic resistance to plastic flow, and m is the strain rate sensitivity of stress. And the parameters for Anand model used in this paper is in Table 2.3.

2.2.3 Multiphysics Fields Coupling and Solving Process

I. Multiphysics Fields Coupling

In the working process, the power device involves the mutual coupling between multiple physical fields. For example, the power loss generated by the current field in the form of Joule heat is the heat source in the temperature field. The material properties in the device are highly dependent on temperature. For example, the resistivity $\rho(T)$ of the chip changes correspondingly with the change of the temperature distribution. The thermal conductivity $k(T)$ decreases with the increase of temperature, which further affects the temperature distribution. Electro-thermal coupling is a dynamic balancing process. It not only involves the generation and transfer of power loss, but also affects the thermal performance of the device. Therefore, the electro-thermal coupling effect is the premise and basis to accurately obtain the temperature distribution of the device [32]. The electro-thermal coupling model is used to analyze the circuit performance and thermal performance under the effect of the current field.

The external environment and its own power loss affect the fluctuation and distribution of the device's temperature. The mismatch of materials' CTEs in each layer causes the device to withstand the thermal strain caused by the temperature fluctuation ΔT during operation. At the same time, the CTE is positively related to temperature, which further leads to different degrees of the expansion and contraction in different materials. The mutual constraint of the materials causes thermal stress inside the device. And the position of each node changes with the deformation, which causes the node potential to change accordingly. Thereby, it affects the change and the distribution of temperature. The mutual coupling relationship between the current field, the temperature field and the stress field in a MOSFET device is shown in Figure

2.4. In order to obtain the distribution of the device's power loss, temperature and stress more accurately, it is necessary to consider the effect of electro-thermal-force coupling.

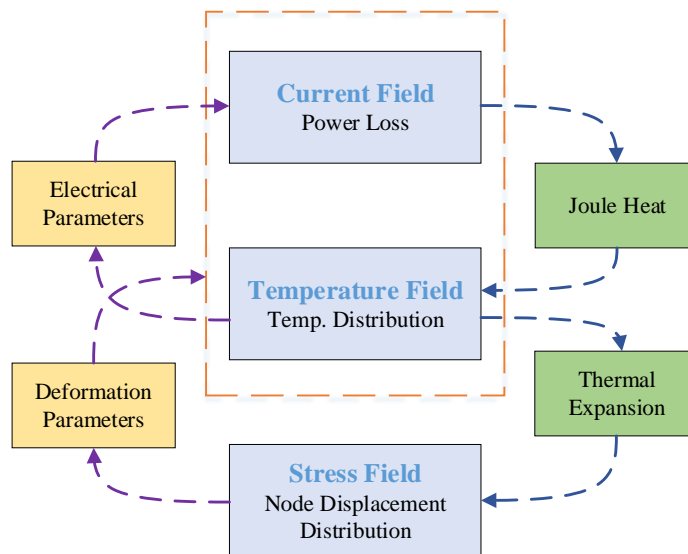


Figure 2.4 Coupling Effect of Multiphysics Fields

II. Solution Process for Multiphysics Coupling

According to the multiphysics coupling relationship mentioned above, the FE element analysis is used to analyze the coupling characteristics of the power device in electro-thermal-mechanical multiphysics fields. The 3-D model of the MOSFET is carried out by using COMSOL software, which has strong visibility and intuitiveness. The analysis flow is shown in

Figure 2.5.

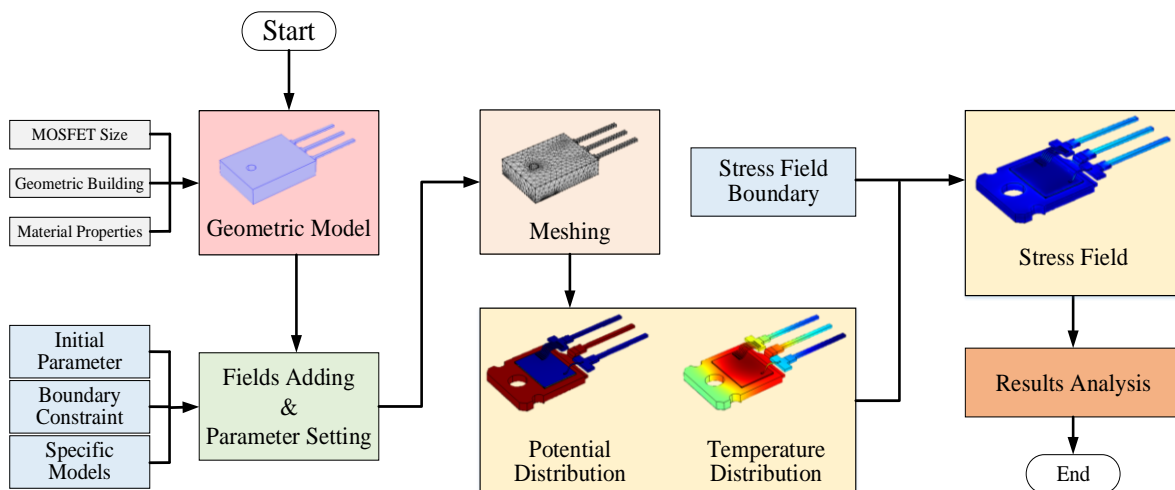


Figure 2.5 Analysis Flowchart of Coupling Model

In this paper, the power device with the package type of TO-264 is simulated. The physical model and FE model are shown in Figure 2.6. It is stacked from different materials, consisting

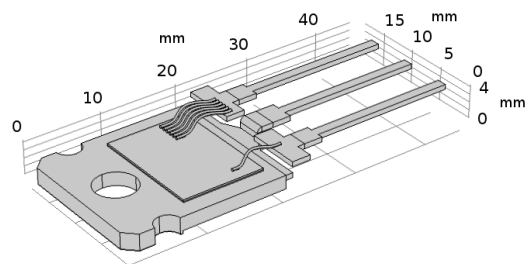
of the metal film, silicon chip, solder layer, copper baseplate, molding compound and bond wires. In operation, the devices mainly have electro-thermal coupling and thermo-mechanical coupling. Firstly, a geometric model is established in COMSOL software. The material properties of the device are defined. At the same time, the dependence of some materials on temperature is considered. Then, current, thermal and mechanical fields are added. And the corresponding initial conditions and boundary constraints are set, which in accordance with the actual operation, including current, voltage, ambient temperature and heat dissipation. After that, appropriate meshing has been done. The sizes of mesh are different for different parts. Next, the FE model is computed.

From

Figure 2.5, we can know that the temperature distribution is the bridge between the current field and stress field. Since the coupling of the three physics fields needs to consume a huge computation and resource. It needs to waste a great lot of time and even causes non-convergence. In this simulation, the electro-thermal coupling field is solved and analyzed first. And then, the result of the temperature distribution of the device is introduced into the stress field as an initial condition to solve the thermal stress distribution.



Picture of Real MOSFET



Model Built in COMSOL

Figure 2.6 MOSFET and Model in COMSOL

2.3 FE Model Building and Validation

2.3.1 Setting for Material Parameters

The key point for FE modeling lies in and the accuracy of material properties and correct

model size. In this paper, the size parameters of the device's plastic package and external pins are obtained from the device datasheet. The sizes of each part are shown in Table 2.1.

Table 2.1 Geometry Parameters of Different Parts

Components	Materials	L/mm	W/mm	H/mm	Radius/mm
Chip	Si	14.24	10.48	0.2	--
Solder Layer	96.5Sn3.5Ag	14.24	10.48	0.12	--
Metal Film	Al	14.24	10.48	0.004	--
Copper Layer	Cu	18.6	20.4	2.04	--
Case	Epoxy	19.9	26	5	--
Bond Wires	Al	--	--	--	0.18

The on-resistance is almost determined by the chip resistance. Therefore, it can be regarded as a uniform resistance after ignoring the difference between the upper and the bottom of the silicon. It can be expressed as:

$$R_{\text{die}} = \rho \frac{d}{S} \quad (2.1)$$

Where: R_{die} is the chip resistance; ρ is the resistivity; d and S are the chip thickness and area, respectively.

According to the output characteristic curve in the datasheet, R_{on} varies with the on-current and the junction temperature. The resistivity is a function related to current and temperature. The dependence of electrical parameters on temperature and other variables must be considered in the modeling.

As shown in Table 2.2, some material properties depend on temperatures, such as conductivity, thermal conductivity and CTE. In order to simulate the model accurately, this paper sets the thermal conductivity of silicon and copper and the CTE of silicon as linear. The equations are as follows:

$$TC_{\text{si}} = \begin{cases} 313 - 0.558 * T, & 300 < T < 350 \\ 246 - 0.368 * T, & 350 \leq T \leq 400 \end{cases} \quad (2.2)$$

$$TC_{Cu} = \begin{cases} 431 - 0.1 * T, & 300 < T < 350 \\ 417 - 0.06 * T, & 350 \leq T \leq 400 \end{cases} \quad (2.3)$$

$$CTE_{Si} = \begin{cases} (0.437 - 0.00732 * T) \times 10^{-6}, & 300 < T < 350 \\ (1.116 - 0.00538 * T) \times 10^{-6}, & 350 \leq T \leq 400 \end{cases} \quad (2.4)$$

Table 2.2 Properties of Materials

Materials	κ^1 W/(m·K)	ρ^2 kg·m ⁻³	C^3 J/(kg·K)	Electric Cond. S/m	Young's Modulus GPa	Poisson's Ratio	CTE 10 ⁻⁶ ·K ⁻¹		
	T ⁴	κ					T	CTE	
Si	300K	145.6	2329	700	T & Current	170	0.28	300K	2.633
	350K	117.7						350K	2.999
	400K	99.3						400K	3.268
96.5Sn 3.5Ag	50	7440	230	9.1e6	107-0.193T	0.37	16.28+0.0204T		
Cu	Temp.	Cond.	8700	385	T	110	0.35	17	
	300K	401							
	350K	396							
	400K	393							
Al	238	2700	900	T	70	0.33	23		
Epoxy	0.67	1211	500	5e-15	9.3	0.39	59		

The solder layer plays a key role in the electrical, mechanical and thermal connection between different materials. The quality of the solder layer directly affects the performance and reliability of the device. 96.5Sn3.5Ag alloy solder has the advantages of high strength, resistance to thermal fatigue and creep [32]. However, the melting point of the solder is lower than other materials, around 221°C. In order to accurately describe the mechanical behavior of the solder layer, its viscoplastic properties must be considered.

In the thermmal-force coupling model, the rest of the material except the solder layer is set as an elastic material. Table 2.2 gives the corresponding material properties. In this paper,

¹ Thermal conductivity.

² Density.

³ Specific heat capacity.

⁴ Temperature (unit: K).

Anand model is selected to describes the mechanical properties of the solder layer[33]. This model can accurately and effectively analyze the viscoplastic properties of solder layers, which provides a theoretical basis for the analysis of the failure mechanism. In [33], the tensile test of the solder layer was carried out at different temperatures and strain rates. The experimental data were used to fit the Anand model parameters of 96.5Sn3.5Ag. The parameters are shown in Table 2.3.

Table 2.3 96.5Sn3.5Ag Parameters for Anand Model

Parameters	Definitions	Values	Units
A	Viscoplastic rate coefficient	22300	sec ⁻¹
Q	Activation energy	74000	J/mol
ζ	Multiplier of stress	6	-
m	Stress sensitivity	0.182	-
S_s	Deformation resistance saturation coefficient	73.81	MPa
S_{init}	Deformation resistance initial value	39.09	MPa
h_0	Hardening constant	3321.15	MPa
α	Hardening sensitivity	1.82	-
n	Deformation resistance sensitivity	0.018	-

2.3.2 Boundary Conditions

Because the size has a huge difference between the device and the heatsink, especially the bond wires. So, the heatsink is not contained in the simulation model, which can save calculation resources and improve efficiency. In order to simulate the effect of the heatsink equivalently, a convective heat transfer coefficient for the bottom surface of the copper baseplate is set. The coefficient is different in different operation condition. It can be calculated by the equation (2.5):

$$q = hA\Delta T = \Delta T / Z_{th} \quad (2.5)$$

Where: q is the total heat; h is the convective heat transfer coefficient; A is the effective heat exchange area of the device; ΔT is the temperature difference between the fluid and the surface of the solid; $Z_{th} = 1/hA$ is the convective heat transfer resistance. The plastic package is set to naturally exchange heat with air. The heat transfer coefficient is $12.5\text{W}/(\text{m}^2\cdot\text{K})$. The pins mainly dissipate heat through the PCB. And the coefficient is $200\text{W}/(\text{m}^2\cdot\text{K})$.

The inherent heat dissipation capability of the device can be measured by the junction-case steady-state thermal resistance Z_{jc} . It can be described by the heat transfer equation (2.6):

$$Z_{jc} = \frac{T_j - T_c}{P} = \frac{T_j - T_c}{V_{on} \cdot I_d} = \frac{T_j - T_c}{I_d^2 \cdot R_{on}} \quad (2.6)$$

Where: P is the power loss of the entire device; T_j is the average temperature of the top surface on the chip; T_c is the average temperature of the copper substrate directly below the chip; V_{on} is the turn-on voltage drop; I_d is the on-current. Z_{jc} is constant when a MOSFET is healthy. It only depends on the device's material and structure. Operation condition has no influence on it.

2.3.3 Validation of the FE Model

In the simulation, the mesh size directly effects on the accuracy of the results and the computational efficiency. It can be set by the user or by the software. In this simulation, the mesh size is set by the latter. The size is controlled by fields, shown in Figure 2.7. We can see various sizes in the FE model. At the corner of the chip and the place contacting with bond wires are fine. The meshes in copper baseplate and pins are coarse. There are 144968 domain elements, 32794 boundary elements and 3747 edge elements.

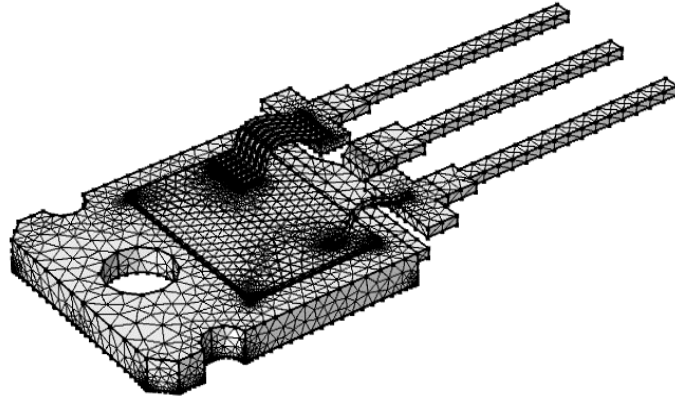


Figure 2.7 Meshing Controlled by Multiphysics Fields (Case hidden)

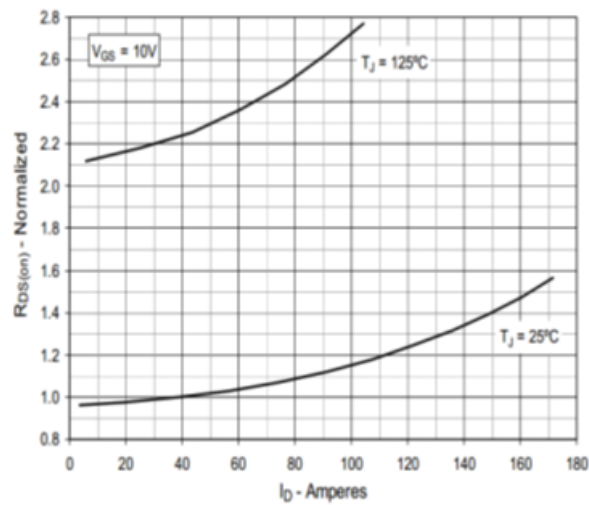


Figure 2.8 Normalized On-resistance from Datasheet

According to the datasheet of the device, we can get the output characteristic curve, shown in Figure 2.8. It gives the on-resistance when the T_j is 25°C and 125°C , respectively. The on-resistance is normalized in the figure. The basis on-resistance is measured under the $T_j=25^\circ\text{C}$ and $I_d=40\text{A}$, $70\text{ m}\Omega$.

In order to verify the FE model built in COMSOL, we set $T_j=25^\circ\text{C}$ and $T_j=125^\circ\text{C}$ respectively. And the gate voltage $V_{gs}=10\text{V}$. The normalized R_{on} obtain from FE simulation is shown in Figure 2.9. We can see the error is in an extremely small range. Above all, we can take the FE model as an accurate and valid model. It can give promise to subsequent simulation and analysis.

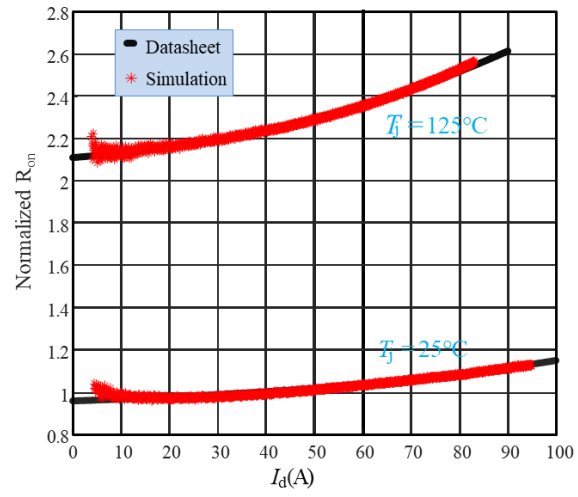


Figure 2.9 Normalized On-resistance Obtained from FE Model

Chapter 3 MOSFET's Failure Modes and Characteristics Analysis

When the device is in different failure modes and different degrees of failure, its electric and thermal properties will change. Once the device begins to age, the performance of the device will change accordingly and show certain fault characteristics. The characteristic parameters of the device are the reflection of these changes. Solder layer fatigue is one of the main failure modes in the device's package level. For this reason, it is necessary to consider the effects of solder layer aging on device reliability. At present, the evaluation of the power device state is mainly dependent on a single characteristic parameter. And most studies do not consider the influence of the aging degree of the power device on its thermal characteristics.

A lot of studies have been carried out by researchers on the health state of power devices. The investigation found that the junction-case steady-state thermal resistance Z_{jc} can be used as a characteristic parameter to describe the aging degree of the solder layer. At present, there are several failure criteria for soldered power devices. The increase of R_{on} by 5% is for the aluminum bond wire to failure. And the increase of Z_{jc} by 20% is defined as the thorough failure of the solder layer. In this paper, the failure evolution process and failure characteristics of MOSFET device are studied and analyzed through the simulation of different failure modes, failure degree and failure position.

3.1 Effects of Voids in Solder Layer

During the manufacturing process of the power device, the solder layer forms initial defects such as micro cracks and voids [34]. The appearance of defects will cause the heat transfer path of the solder layer to be destroyed and the thermal resistance to increase. Because the heat accumulation of the chip cannot be diffused, the temperature is locally concentrated.

Even hot spots may occur in severe cases. It can be seen from the X-ray tomography of the unused devices that the distribution of initial voids in the solder layer is random, the size is different, and the edges have fine cracks, as shown in Figure 3.1. Although the location, shape and distribution of the initial voids are random and the area is small, the voids will accelerate their expansion under the long-term impact of power and temperature. This will result in an increase in voids area and a more significant heat accumulation, which can cause the fatigue of the solder layer. When the damage is accumulated to a certain value [35], the device fails.

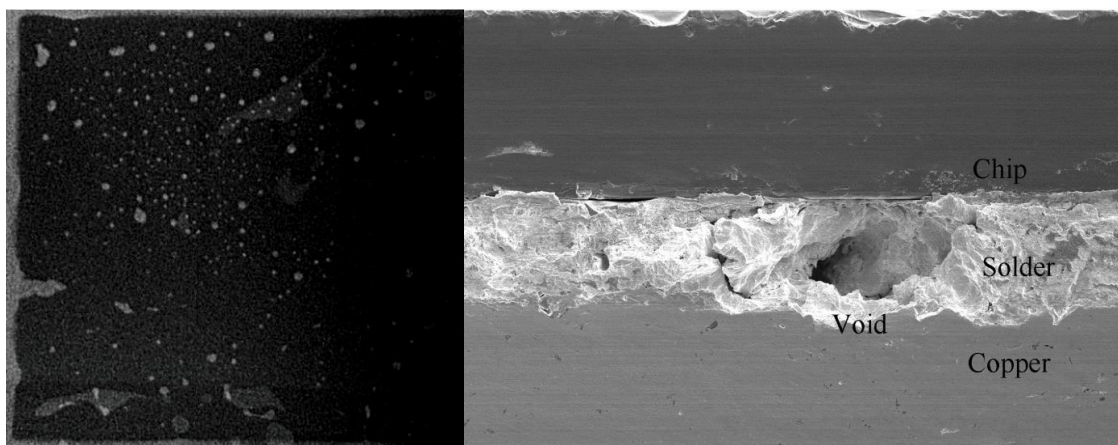


Figure 3.1 Initial Voids under X-ray[36]

The location, shape and size of the solder layer voids may have a great influence on the device's characteristics. In order to simplify the research, two voids distribution (in center and in corner and edges) are studied and analyzed separately. And the voids are assumed as penetrating cylinder.

3.1.1 Voids in Solder Layer Center

The void ratio can be defined as the percentage of the total voids area to the area of the solder layer. In order to simplify the analysis, voids in this section are located in the center of the solder layer. The percentage of void's area from 0% to 50% is simulated and analyzed. In the simulation, the on-current (I_d) is 25 A and ambient temperature is 25°C. The 3D temperature distributions are shown as follows.

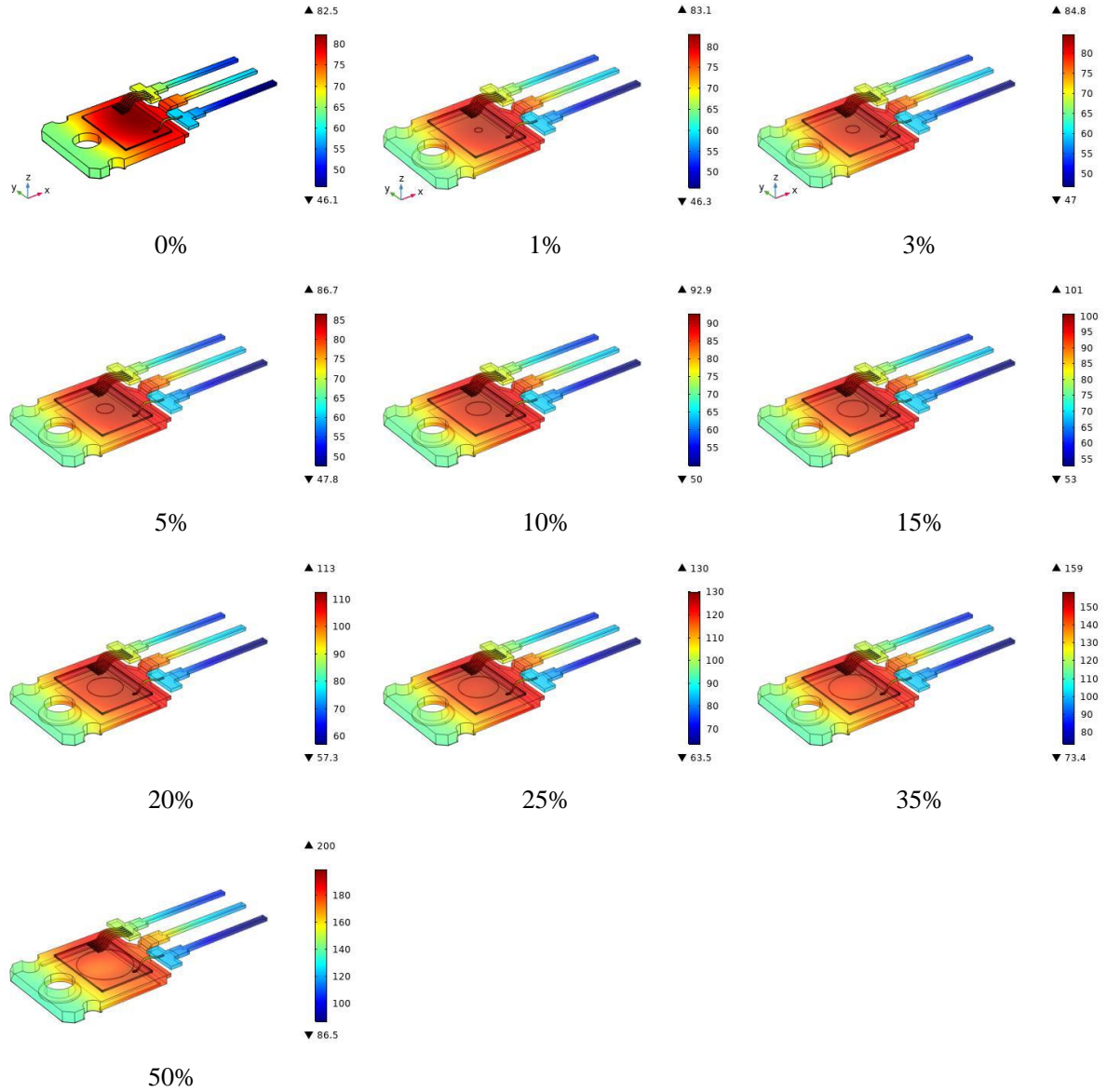


Figure 3.2 Temperature Distribution under Different Center Voids Ratios (Units: °C)

Comparing with the absolute values, the relative change of the characteristic parameters under different aging degrees is more concerned. By the equations (3.1) and (3.2), the growth rates of the junction-case thermal resistance and the on-resistance are calculated, shown in Table 3.1.

$$\Delta Z_{jc} / Z_{jc} = \frac{Z_{jc}(i) - Z_{jc-ini}}{Z_{jc-ini}} \times 100\% \quad (3.1)$$

$$\Delta R_{on} / R_{on} = \frac{R_{on}(i) - R_{on-ini}}{R_{on-ini}} \times 100\% \quad (3.2)$$

Where Z_{jc-ini} and R_{on-ini} are initial values of the healthy device. $Z_{jc}(i)$ and $R_{on}(i)$ are measured values under different aging degree respectively.

Table 3.1 Simulation Results with Different Voids Area in Solder Layer Center

Ratio	0	1%	3%	5%	10%	15%	20%	25%	35%	50%
Radius (mm)	0	0.69	1.195	1.542	2.182	2.670	3.086	3.45	4.082	4.879
T_j (°C)	80.65	80.74	82.42	84.31	90.29	98.0	109.4	125.9	152.1	188.1
T_c (°C)	73.75	74.15	75.59	77.21	82.32	88.95	98.66	112.85	134.91	164.42
Z_{jc} (°C/mW)	97.3	97.5	98.6	99.4	102	105.7	110.4	114.7	129.5	153.2
R_{on} (mΩ)	109.6	111.2	114.3	118.2	123.0	145.2	163.5	185.7	232.7	327.9
$\Delta Z_{jc}/Z_{jc}$ (%)	0	0.2	1.3	2.1	4.8	8.7	13.5	17.9	33.1	57.5
$\Delta R_{on}/R_{on}$ (%)	0	1.5	4.3	7.9	18.6	32.6	49.3	69.5	112.4	199.3

In Figure 3.3, Figure 3.4 and Figure 3.5, we can see that junction temperature, case temperature, on-resistance, thermal resistance and their growth rates have a similar trend. All of them raise with the increase of the void's area. We can notice that they show a significant rise when the void's area is more than 20%. When the voids ratio is 20%, the junction temperature is 109.4°C, which is 28.75°C higher than the healthy device. And the case temperature also shows an increase of 23.91°C. Literature [37] said the failure rate of power device shows an exponential rise with the increase in temperature. Besides that, we also notice that R_{on} and Z_{jc} are 163.5 mΩ and 110.4 °C/mW respectively. Their growth rates are 49.3% and 13.5% correspondingly. According to the criterion, when the growth rate of thermal resistance ($\Delta Z_{jc}/Z_{jc}$) reaches 20%, the device can be regarded as a thorough failure. From Table 3.1, when voids ratio is 25%, the $\Delta Z_{jc}/Z_{jc}$ is 17.9%.

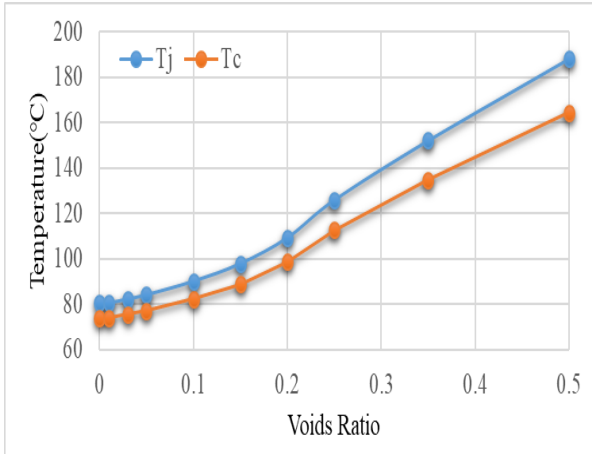


Figure 3.3 Junction and Case Temperature with Different Void's Area

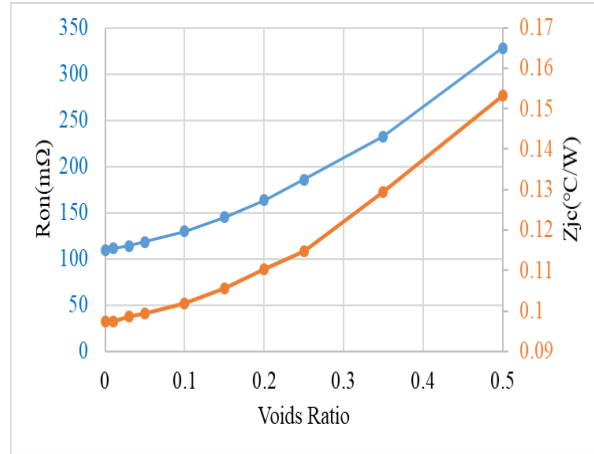


Figure 3.4 On-resistance and Thermal Resistance with Different Void's Area

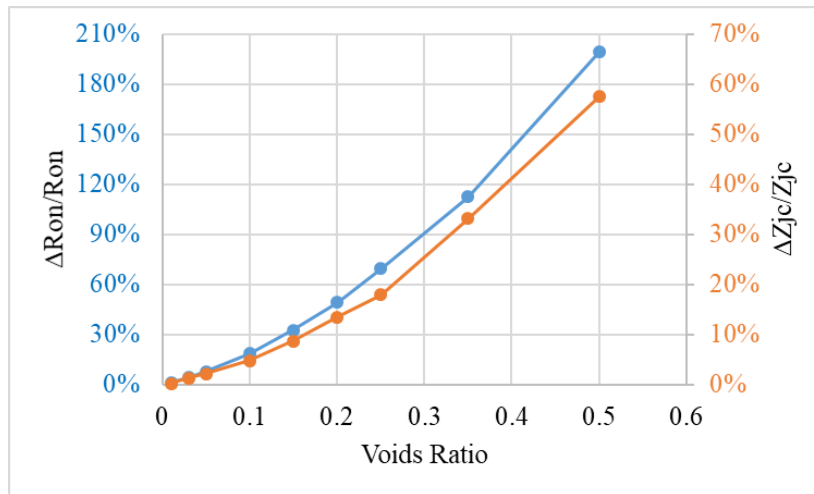


Figure 3.5 Growth Rates of On-resistance and Thermal Resistance with Different Void's Area

Figure 3.6 shows the temperature distributions of the die under different center voids ratio. It can be seen that the temperature profile is arc and gradually decreases outward. When a void appears in the center of the solder layer, the maximum value of temperature increases with the area of voids. Besides that, we can also see an obvious hot spot when the ratio is more than 15%. The larger the void area, the more obvious hot spot. And the location of hot spot moves from the center toward the right top corner, which leads to higher thermal stress on the corner. When the percentage is more than 20%, we can see some change in the temperature profile. Because the void affects the heat transfer path, there is a huge temperature difference on the right side. Right-top corner's temperature is more than 200 °C, around 2.5 times more than the

healthy device's.

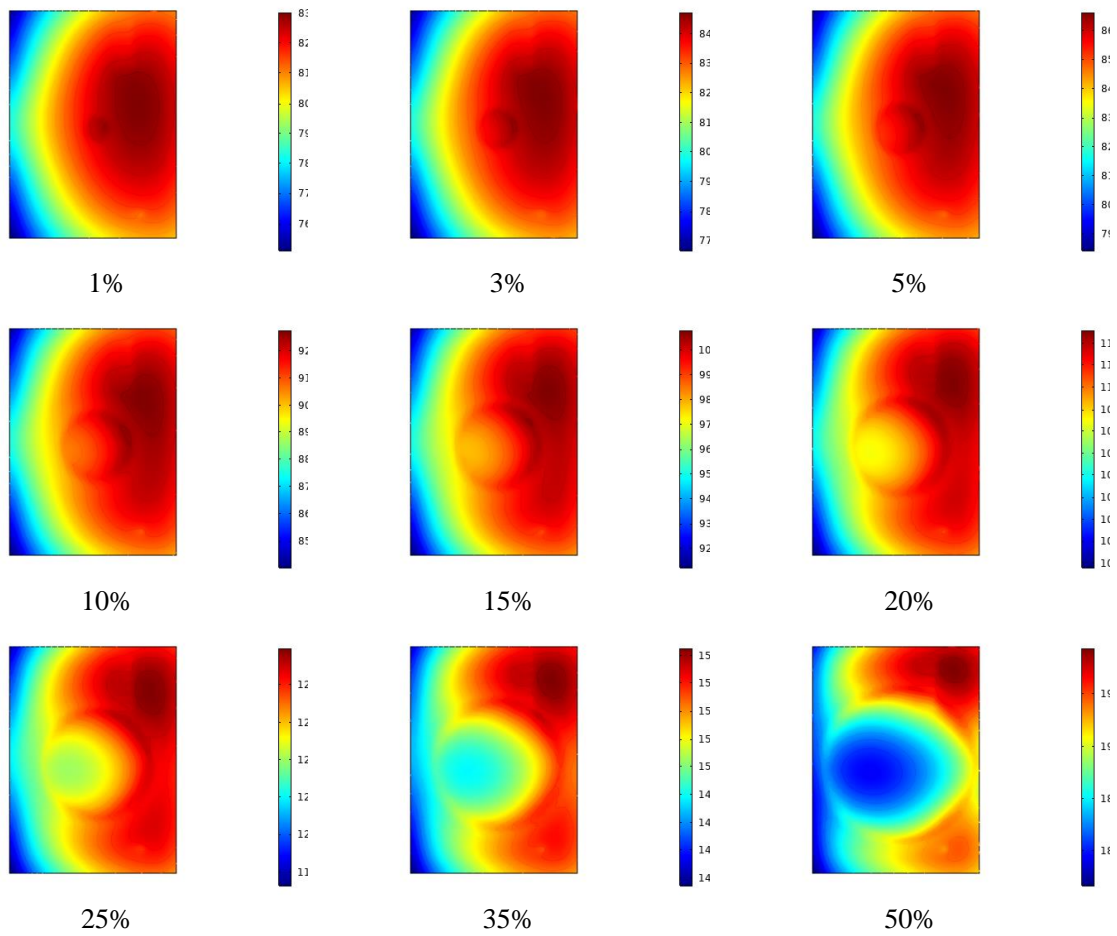


Figure 3.6 Temperature Distribution of Die with Different Center Voids Area

3.1.2 Voids in Solder Layer Edges

Figure 3.7 shows the voids in edge used in the simulation. By using this distribution, the effect of voids is uniformly located in the edges. According to the criterion, the area of voids in edges cannot be more than 10% of the solder layer's area.

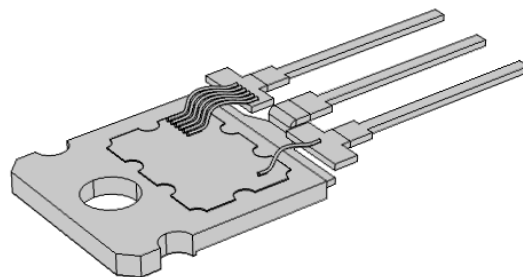


Figure 3.7 Diagram of Voids in Edges

Table 3.2 shows the simulation results of the voids in edges. It can be seen that there is a similar law with the characteristics of the voids in the center, shown in Figure 3.8 Junction and Case Temperature with Different Edge Voids Figure 3.8~Figure 3.10. Comparing with Table 3.1, we can notice that the voids in edges show a larger effect on growth rates of on-resistance and thermal resistance, especially the $\Delta Z_{jc}/Z_{jc}$. When the void's area is 5% in two types, the $\Delta Z_{jc}/Z_{jc}$ s are 2.1% and 4.72, respectively. And the $\Delta R_{on}/R_{on}$ s are 7.9% and 6.92% correspondingly. There is not much difference between the T_j and the T_c .

Table 3.2 Simulation Results with Different Edge Voids in Solder Layer

Ratio	0	0.25%	0.75%	1.25%	2.5%	5%	7.5%	10%
Radius(mm)	0	0.1723	0.2984	0.3853	0.54493	0.7706	0.94383	1.090
$T_j(^{\circ}\text{C})$	80.11	80.18	80.46	80.81	81.78	84.03	86.80	89.95
$T_c(^{\circ}\text{C})$	73.59	73.68	73.91	74.20	75.03	76.95	79.32	82.00
$Z_{jc}(^{\circ}\text{C}/\text{mW})$	95.61	95.77	96.09	96.51	97.55	100.13	105.58	113.60
$R_{on}(\text{m}\Omega)$	109.8	110.1	110.6	111.3	113.1	117.4	122.7	136.7
$\Delta Z_{jc}/Z_{jc}$	0	0.17%	0.50%	0.94%	2.03%	4.72%	10.43%	18.81%
$\Delta R_{on}/R_{on}$	0	0.26%	0.73%	1.32%	3.00%	6.92%	11.73%	24.50%

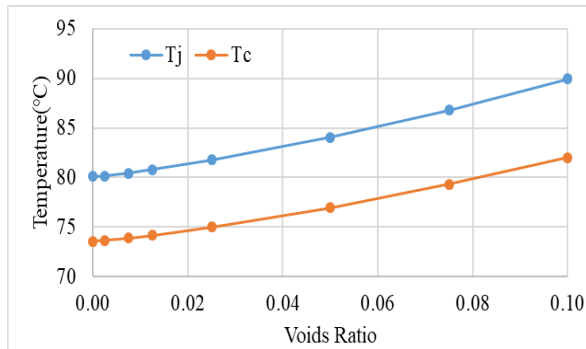


Figure 3.8 Junction and Case Temperature with Different Edge Voids' Area

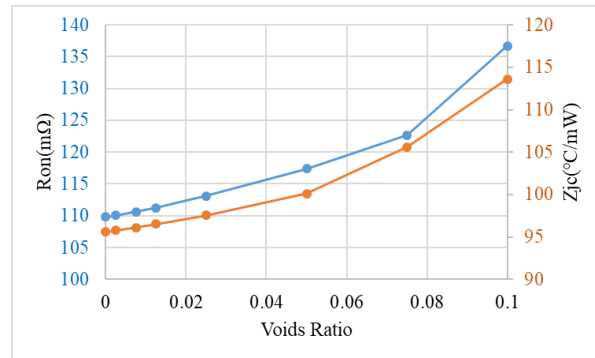


Figure 3.9 On-resistance and Thermal Resistance with Different Edge Voids' Area

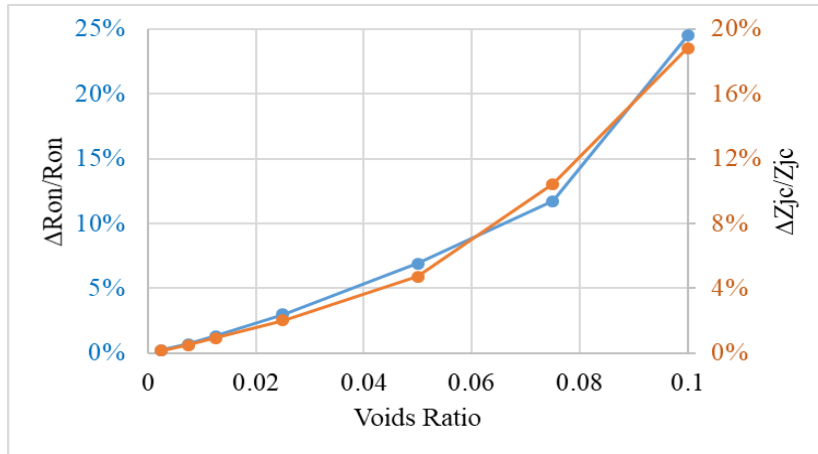


Figure 3.10 Growth Rates of On-resistance and Thermal Resistance with Different Edge Voids' Area

Comparing Figure 3.6 and Figure 3.11 Temperature Distribution of Die with Different Edge Voids Figure 3.11, it can be seen that the voids in edges decrease the heat dissipation capability, which leads to higher thermal resistance and on-resistance than the voids in the center. And the area of high temperature rises with the increase of voids area.

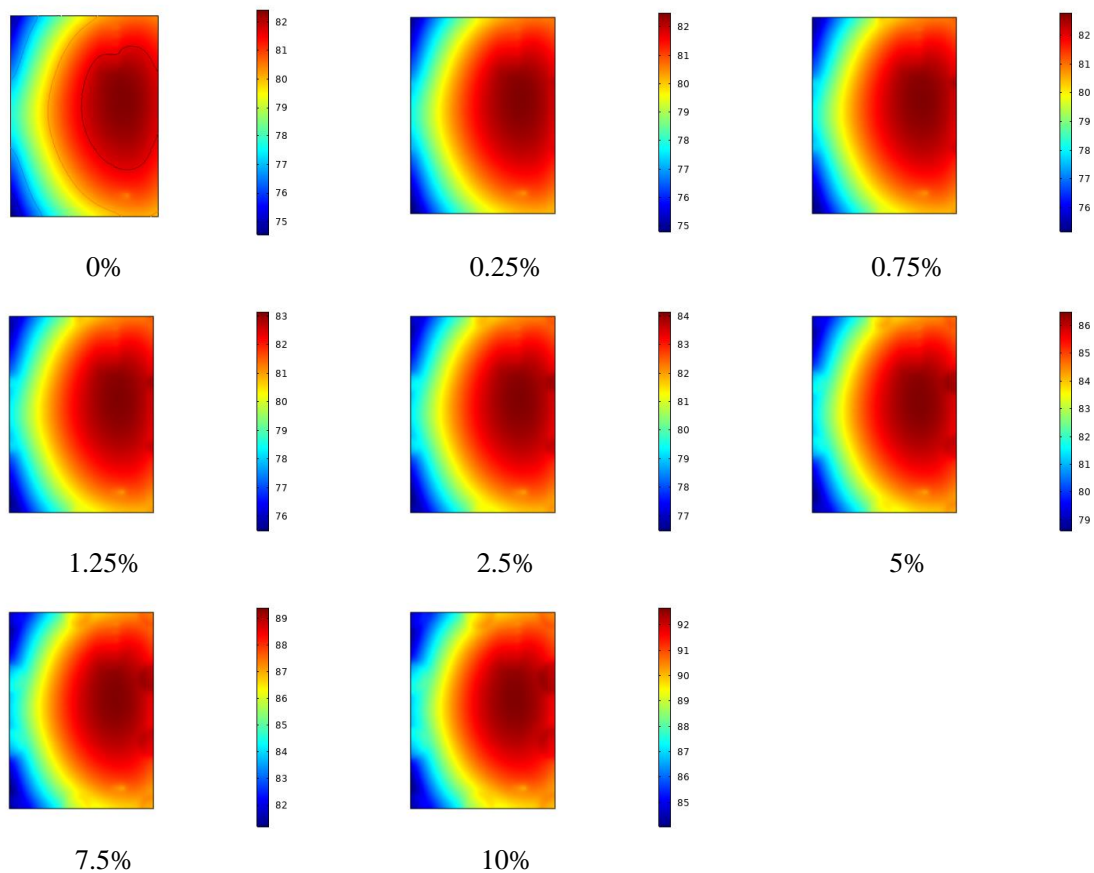


Figure 3.11 Temperature Distribution of Die with Different Edge Voids' Area (Units:°C)

3.2 Effects of Solder Layer Fatigue

Due to the low melting point of the solder layer (96.5Sn3.5Ag, 221°C), creep deformation and stress relaxation can occur at room temperature. In an actual working environment, the inelastic deformation and stress relaxation effect are more pronounced. The fatigue delamination of the solder layer is one of the aging failure modes of devices caused by the long-term effects of periodic temperature and stress. The failure mode is an accumulation process of inelastic strains such as plastic deformation and creep deformation. As the aging degree of the power device increases, the heat dissipation gradually deteriorates. And the heat dissipation performance can be characterized by Z_{jc} . Literature [38] pointed out that there is a positive relationship between the fatigue degree of the solder layer and T_j .

There are two methods to simulate the solder layer fatigue: adding heatsinks with a certain thermal resistance under the solder layer or reducing the solder layer area [38]. For the simulation in this paper, the latter was used. The on-current and ambient temperature are $I_d=25A$ and $T_a=25^\circ C$, respectively. The simulation results are shown as follows.

Table 3.3 Simulation Results with Different Fatigue Degrees of Solder Layer

Ratio	0	5%	10%	15%	20%	25%	30%	35%	40%	50%
Area ($S \cdot mm^2$) ¹	1	0.975 ²	0.949 ²	0.922 ²	0.894 ²	0.866 ²	0.837 ²	0.806 ²	0.775 ²	0.707 ²
$T_j(^{\circ}C)$	80.1	82.1	87.1	95.0	106.8	123.5	142.8	152.6	170.9	192.1
$T_c(^{\circ}C)$	73.6	75.2	79.5	86.2	96.3	110.4	126.8	134.9	149.7	166.9
Z_{jc} ($^{\circ}C/mW$)	95.5	97.3	99.9	103.9	105.2	108.8	114.6	117.6	123.1	137.2
$\Delta Z_{jc}/Z_{jc}$ (%)	0	2.0	4.6	8.8	10.2	14.0	20.1	23.1	29.0	43.8
$R_{on}(m\Omega)$	109.9	113.5	123.1	138.0	160.5	192.0	228.4	246.1	278.9	346.6
$\Delta R_{on}/R_{on}$ (%)	0	3.2	11.9	25.5	46.0	74.7	107.7	123.8	153.7	215.3

¹ $S = 10.48 \times 14.24$

Figure 3.12 shows the temperature changes of junction and case under different fatigue degree. All of them rise when the fatigue extent increases. And the T_j has a similar trend with the T_c . In Figure 3.13, we can see the trends of on-resistance and thermal resistance with the change of fatigue degree. They show the same change law with the temperature trend. Also, we can notice that R_{on} is more sensitive than the Z_{jc} . Figure 3.14 shows their growth rates, which can present their sensitivity intuitively. By the way, there is a huge increase in all the parameters when the fatigue degree exceeds 20%. So the fatigue process and the changes of R_{on} and Z_{jc} are nonlinear, in accordance with [9].

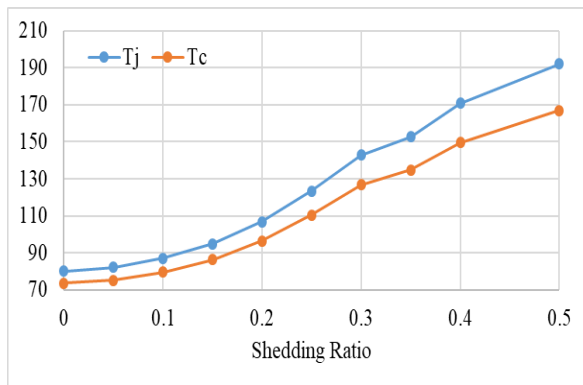


Figure 3.12 Junction and Case Temperature with Different Fatigue Degree

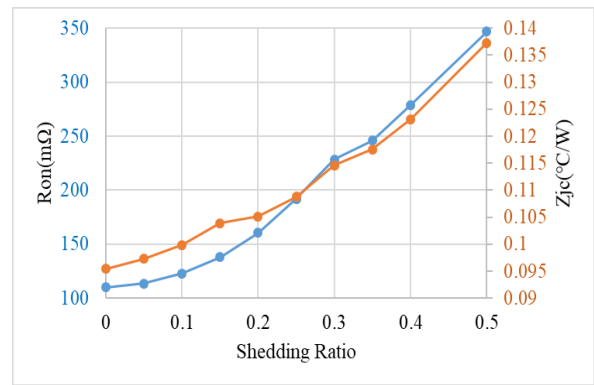


Figure 3.13 On-resistance and Thermal Resistance with Different Fatigue Degree

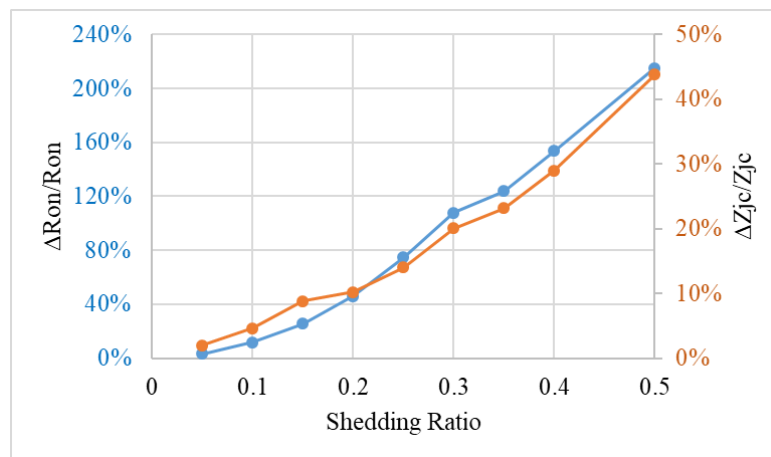


Figure 3.14 Growth Rates of On-resistance and Thermal Resistance with Different Fatigue Degree

Figure 3.15 gives the temperature distributions of the die with different fatigue degrees. It can be seen that the temperature increases with the increase of the fatigue degree. When the extent is 35%, the value is around twice as high as the temperature in a healthy state. Besides

that, the area of high temperature reduces. And the profile of high temperature moves from the right side toward the center. So, there is higher thermal stress in the center, which accelerates the expansion of cracks in the solder layer.

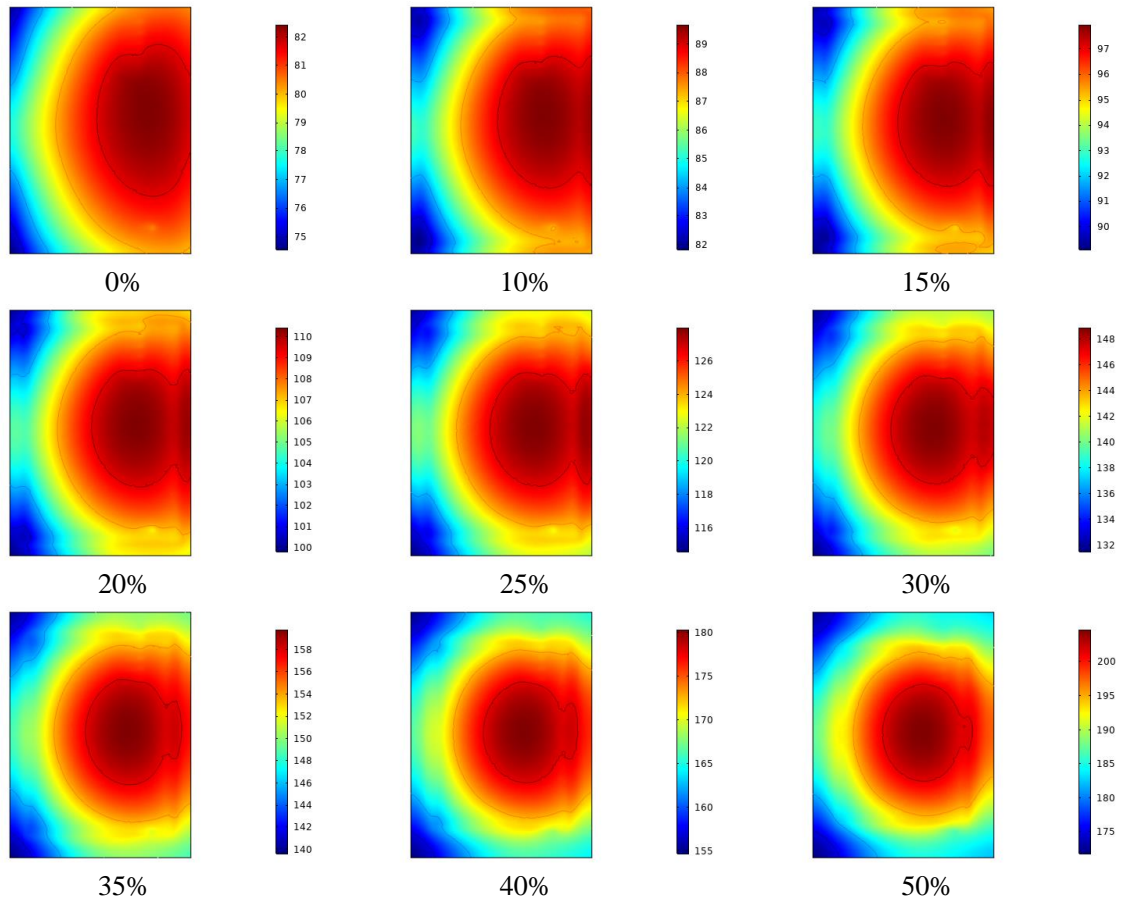


Figure 3.15 Temperature Distribution of Die with Different Fatigue Degree (Units:°C)

3.3 Failure Mechanism Analysis of Solder Layer

In the electro-thermal coupling analysis, the simulation parameters are set as conduction current $I_d=30A$, ambient temperature $T_a=25^\circ C$ and forced convective heat transfer coefficient $h_{ca}=5000W/(m^2 \cdot K)$. The three-dimensional temperature distribution of the MOSFET is shown in Figure 3.16. Under the action of the current, the heat generated by the chip mainly flows through the solder layer to the copper substrate. And a small part heat transfer along the bond wires to pins. The average T_j of the chip is $147.25^\circ C$. And the average T_c is $132.73^\circ C$. The power loss of the model is $152.27W$ and the junction-case thermal resistance is $0.954^\circ C/W$.

Ignoring the case package, the transverse section of the model is cut from the symmetrical central axis along the long side of the chip. As shown in Figure 3.16, the temperature of each layer gradually reduce. And the highest temperature of chip's upper surface is off-center and the value is 80.24 ° C. The temperature at the edge of the copper baseplate is lower and the value is 70.96 ° C.

The temperature distribution obtained from electro-thermal coupling is input to the stress field to obtain the three-dimensional thermal stress distribution of the solder layer, as shown in Figure 3.17. It can be seen that the large thermal stress is mainly concentrated at the edge of the upper surface of the solder layer contacting with the chip. When the temperature changes greatly, there are cracks at the edge of the solder layer if thermal stress on the chip and the solder up to a certain value. With the long-term circulation of temperature and stress, the cracks extend toward the center and the corners of the solder layer will warp upwards. Eventually, it leads to the delamination of the solder layer. The main reason is the coefficient of thermal expansion is larger than other materials.

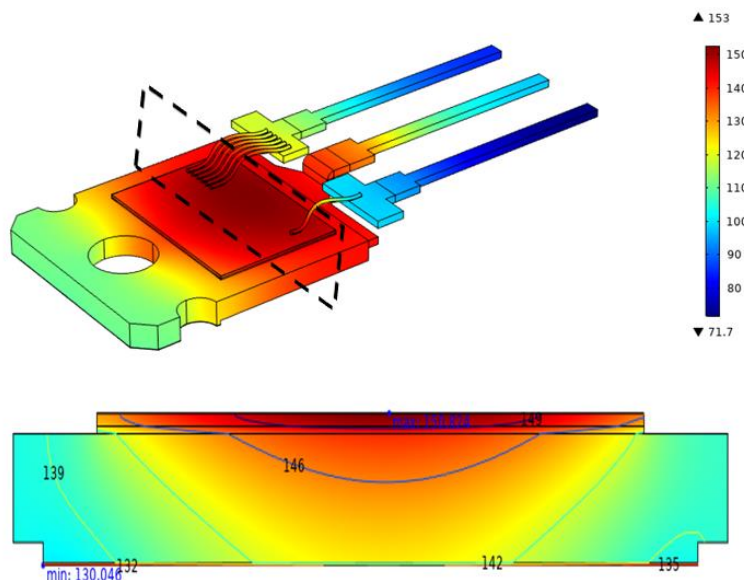


Figure 3.16 3-D Temperature Distribution and Sectional View

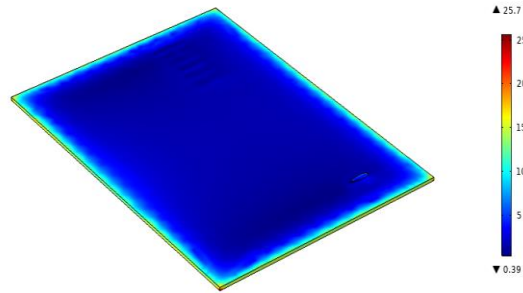


Figure 3.17 Von Mises Stress Distributions of Solder Layer

Multiphysics field coupling simulation needs so much time. In order to save time and calculation resource, we can take the power loss obtained from above as the power of heat source. By this way, we do not need the electric field in this simulation. Figure 3.18 shows the temperature fluctuation under cyclic power. We can see that fluctuation cycle of junction temperature and case temperature are the same as the power cycle. And they have the same trend. When T_j more than 110°C , the difference between T_j and T_c becomes larger with the increase of T_j , which absolutely increase the stress and strain on the solder layer. Figure 3.19 shows the trend of solder layer strain during the cycle. The maximum strain happens at the peak of T_j , around 1.8%. And Figure 3.20 shows the trends of solder layer strain and Von Mises stress with T_j . We can see that both of the strain and stress keep rising when T_j increase. When T_j more than 170°C , the Von Mises stress is about 65 MPa, around 12.8% more than the value in the healthy device (57.6 MPa). Meanwhile, the strain is near 2% less than the healthy device.

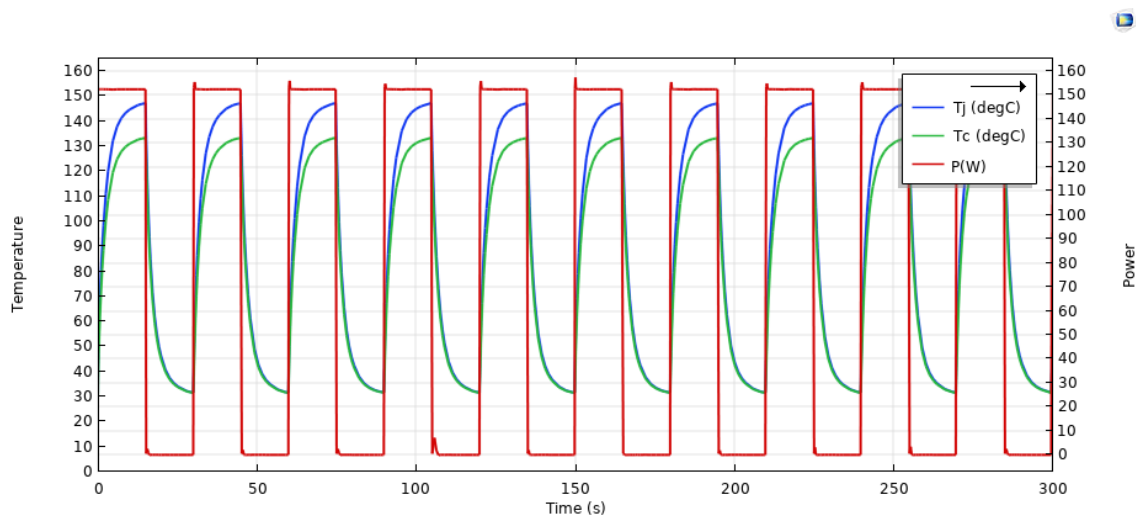


Figure 3.18 Junction and Case Temperatures under Cyclic Power

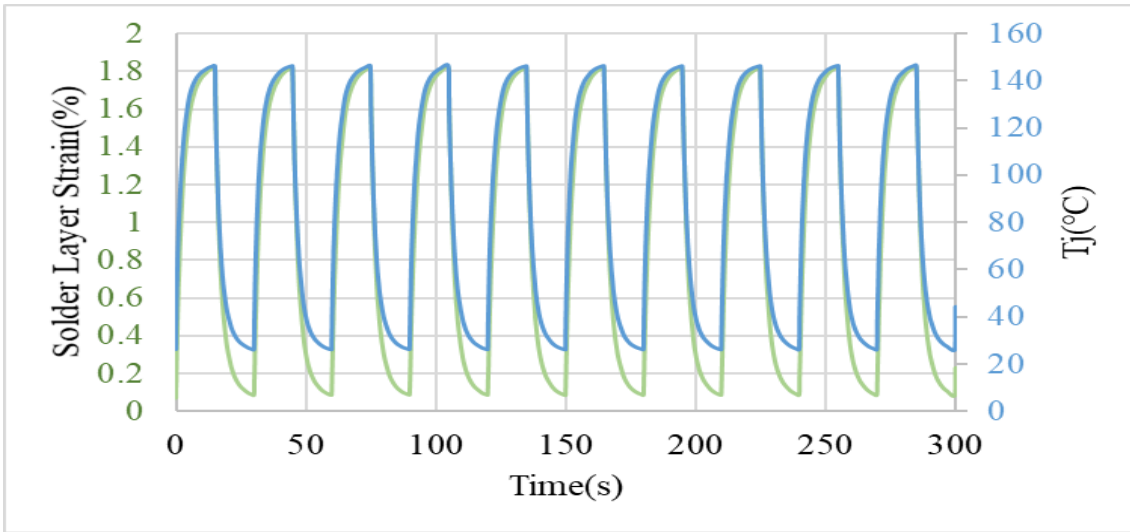


Figure 3.19 Solder Layer Strain under Cyclic Power

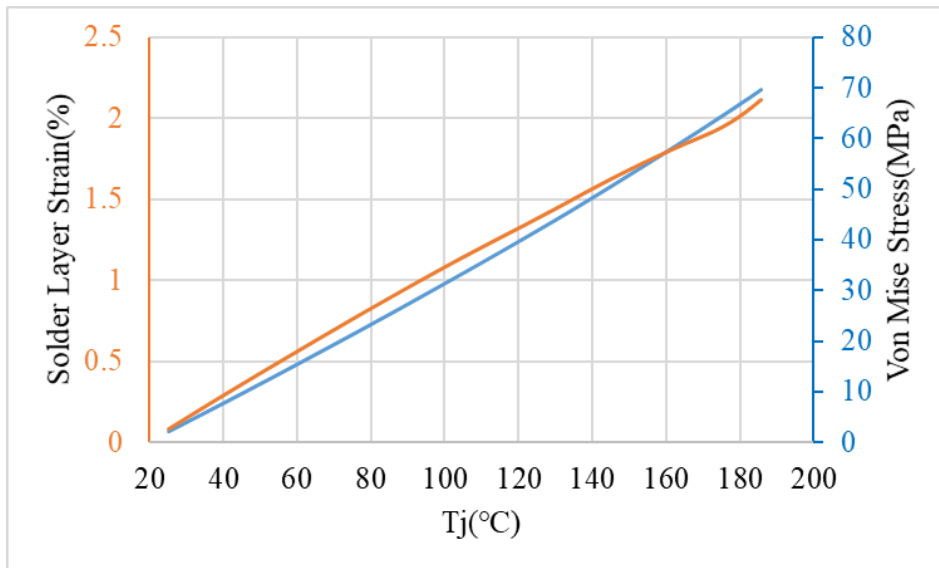


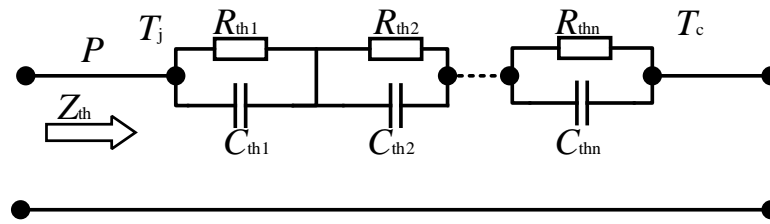
Figure 3.20 Trend of Solder Layer and Von Mises Stress with T_j

3.4 Thermal Network Models and Parameters Selection

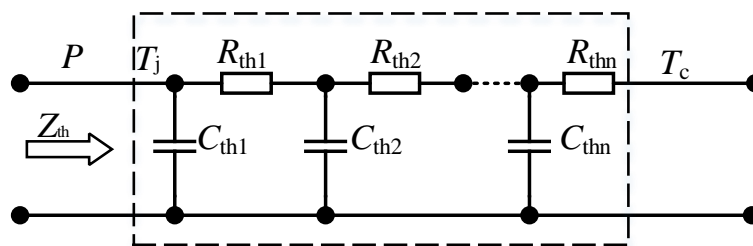
3.4.1 Thermal Network Models

There are two types of thermal network model used in thermal analysis equivalently: Foster model[40] and Cauer model[41]. Their structures are shown in Figure 3.21. The Cauer model corresponds to the actual structure of the package. The Foster model is only a mathematical fit to the transient thermal resistance curve and does not have any practical physical meaning. But the Foster thermal network has clear mathematical expressions that are

more convenient and easier to obtain in terms of numerical calculations.



(a) Foster Model



(b) Cauer Model

Figure 3.21 Thermal Network Models

When the solder layer with fatigue, the junction-case thermal resistance Z_{jc} changes to $Z_{jc} + \Delta Z_{jc}$. This can lead the junction temperature and the total heat loss to increase, which is the main reason causing case temperature to rise [41]. According to the output characteristic curve of the device, when the I_d is fixed, the on-resistance is only related to the T_j . The obvious change of T_j will definitely make an obvious change on R_{on} . And the change has a positive feedback effect.

3.4.2 Parameters Selection and Sensitivity Analysis

The power device characteristic parameters mainly include operating parameters generated by the device itself and external working environment. Accurate selection of input and output characteristic parameters is a prerequisite for ensuring the validity and representativeness of the state assessment model.

According to the analysis under different failure modes in Section 3.1 and Section 3.3, it is known that voids in center or edges and solder layer aging will lead to an increase in junction

temperature, case temperature, on-resistance and junction-case thermal resistance. From Figure 3.3, Figure 3.8 and Figure 3.12, the case temperature keeps a similar trend with the junction temperature. It means we can use the T_c to replace the T_j . Because it is very difficult to measure the T_j . However, the T_c is much easier to get. Based on Figure 3.4, Figure 3.9 and Figure 3.13, no matter what types of failure modes, R_{on} and Z_{jc} rise with the rise of fatigue degree. And the trend of R_{on} has a similar trend with the Z_{jc} . From Figure 3.22, we can see that the relationship between R_{on} and Z_{jc} is linear under different aging modes. So we can use R_{on} to present the change of the Z_{jc} .

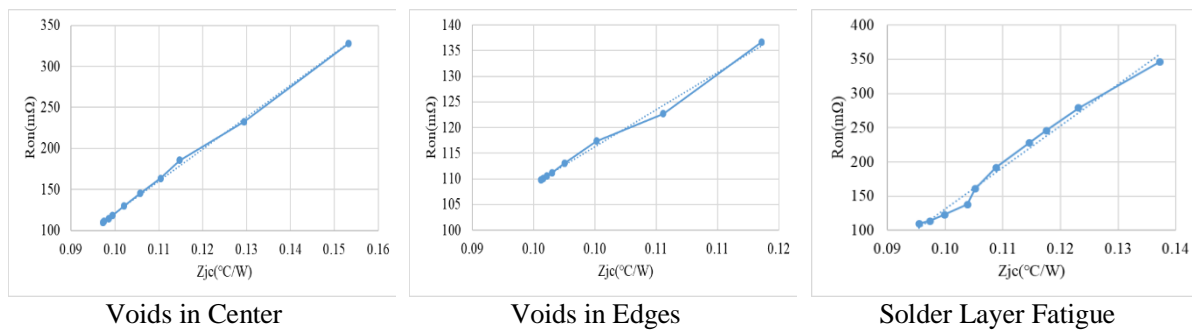


Figure 3.22 Relationship between R_{on} and Z_{jc} in Different Aging Modes

Based on the analysis of growth rates of R_{on} and Z_{jc} in Section 3.1 and Section 3.3, we can know that the growth rate of R_{on} is larger than the rate of Z_{jc} during the aging process. So $\Delta R_{on}/R_{on}$ is more sensitive than $\Delta Z_{jc}/Z_{jc}$. The value of $\Delta R_{on}/R_{on}$ is several times larger than the value of $\Delta Z_{jc}/Z_{jc}$. Even though most researches take the $\Delta Z_{jc}/Z_{jc}=20\%$ as the criterion for the thorough failure. But it is hard to measure the junction-case thermal resistance. It needs to remove the package or use an infrared camera, which is not desirable in engineering. So it is advisable to use R_{on} to describe the aging state instead of Z_{jc} .

According to the datasheet, the on-resistance is related to the junction temperature and the drain current. From equation (3.3), R_{on} is only related to the T_j when I_d is fixed. Obvious changes in T_j must cause a significant change in R_{on} , which is positive feedback. When the device is put into operation, the heat dissipation capability of the heat sink is basically

unchanged. So, there is a relationship among R_{on} , T_j and I_d .

$$Z_{jc} \uparrow = \frac{(T_j - T_c) \uparrow}{(I_d^2 \cdot R_{on}) \uparrow} \Rightarrow \frac{(T_j \uparrow - T_c)}{I_d^2 \cdot (R_{on(I_d, T_j \uparrow)}) \uparrow} \quad (3.3)$$

Based on the above analysis, R_{on} , T_j and I_d are selected as the parameters for the healthy state evaluation of the MOSFET device.

Chapter 4 State Evaluation Model for MOSFET

The characteristics of a power device depend on multiple parameters at the same time. With machine learning methods, we can find some weak links by using the data generated during operation to help diagnose the health state of the device. Literature [27] proposed to use GA-BP method to diagnose the device. This method needs a large data and resource to training. In [2], the authors use the temperature gradient and probability density to estimate the health state. However, this model needs to remove the package case and use an infrared camera to measure the temperature distribution of the device, which is impossible in applications.

There are three key steps included in state monitoring technology: selecting the parameters, designing the evaluation system and quantifying the output[42]. According to the analysis in Chapter 3, once the device begins to age, the performance of all aspects will change accordingly and show certain fault characteristics. The changes in thermal and mechanical parameters of the device are the comprehensive reflection. The development of those changes is a process of gradual degradation. By monitoring the corresponding external parameters, the aging degree and reliability of the device can be evaluated.

The characteristic parameters and operating condition are used as inputs of the evaluation model, such as conduction voltage drop and ambient temperature. The parameter that can reflect the degradation degree of the device is selected as the output. So a multi-input-single-output evaluation system can be built. In this paper, the ANFIS (Adaptive Neuro-Fuzzy Inference System) [43] is used to establish a state evaluation model for the MOSFET device, as shown in Figure 4.2.

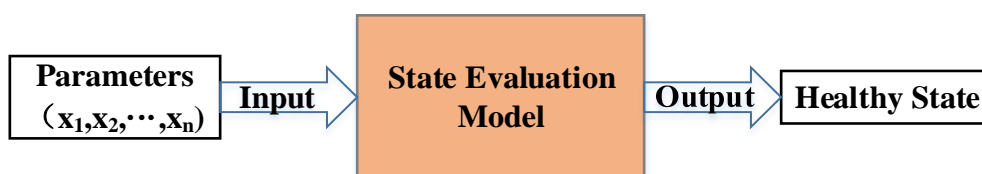


Figure 4.1 State Assessment Structure Diagram

4.1 ANFIS Algorithm and Structure

ANFIS is a kind of artificial neural network which combines neural networks with fuzzy logic principles. So it has the benefits of learning capability to approximate nonlinear functions and inference function. During the learning process, each cycle consists of two phases: the forward propagation of the input signal and the back propagation of the error signal based on the gradient descent. The structure is shown in Figure 4.2.

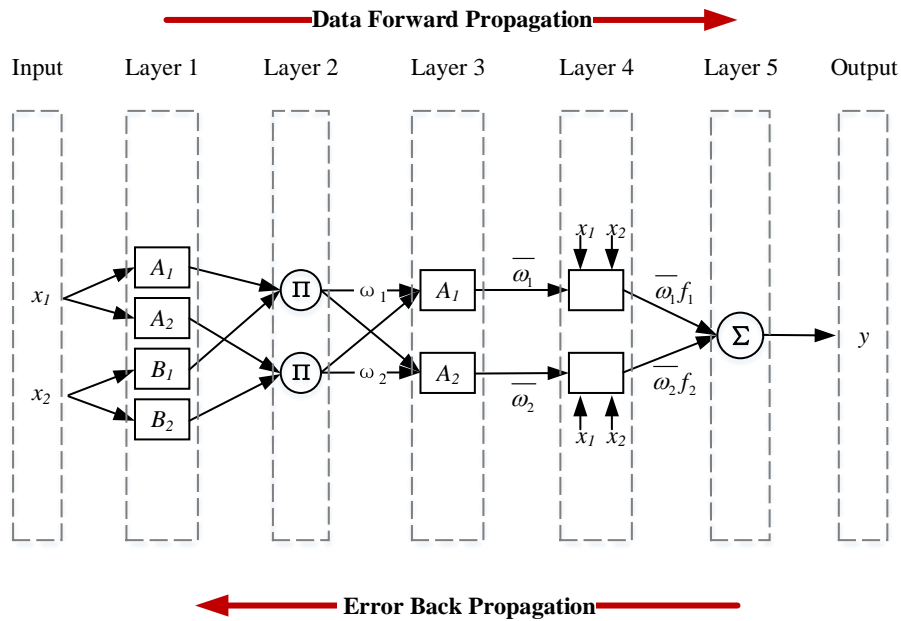


Figure 4.2 The Structure of ANFIS

Take the two-input-single-output network as an example. The key steps of training are as follows:

Layer1: fuzzification layer. The input variables x_1 and x_2 are subjected to the fuzzification operation by the membership function. The fuzzy sets (A_1, A_2, B_1, B_2) indicates the degree of each neuron belonging to a certain fuzzy rule. It is called membership grad.

$$O_{1,i} = u_{A_i}(x_1), \quad i = 1, 2 \quad O_{1,i} = u_{B_{(i-2)}}(x_2), \quad i = 3, 4 \quad (4.1)$$

The Gaussian function $u_{A_i}(x_1) = e^{[-(x_1 - d_i) / \sigma_i]^2}$ is used in this paper, which is the most

common membership function in ANFIS. $\{d_i, \sigma_i\}$ is a set of parameters belonging to membership function $u_{A_i}(x_1)$.

Layer2: rule reference layer. The input signal is multiplied to calculate the rule firing strength represented by the nodes in this layer.

$$O_{2,i} = w_i = u_{A_i}(x_1)u_{B(i)}(x_2), \quad i = 1, 2 \quad (4.2)$$

Layer3: normalized layer. Nodes in this layer are used to calculate the normalized firing strength under some given rules.

$$O_{3,i} = \bar{w}_i = w_i / \sum_i w_i, \quad i = 1, 2 \quad (4.3)$$

Layer4: rule layer. It is obtained by multiplying the last layer. The initial variables (x_1 , x_2) are used to calculate the adaptive value with weight.

$$O_{4,i} = \bar{w}_i f_i = \bar{w}_i (p_i x_1 + q_i x_2 + r_i), \quad i = 1, 2 \quad (4.4)$$

Layer5: output layer. The last layer of ANFIS adds up all the output values of the upper nodes. This layer has only one output node.

$$O_{5,i} = \sum_i (\bar{w}_i f_i) = \sum_i \left(w_i f_i / \sum_i w_i \right), \quad i = 1, 2 \quad (4.5)$$

This algorithm combines the learning algorithm of the neural network and the simple form of fuzzy reasoning. It clarifies the physical meaning of the nodes and weight in the neural network and avoids the feature of ‘black box’. Therefore, this system not only has the learning mechanism and adaptive ability of the neural network, but also has the logical reasoning ability of the traditional fuzzy system[44]. It is widely used in the pattern recognition and classification training system.

4.2 Evaluation Model Based on ANFIS

4.2.1 Data for Machine Learning

It is impossible to obtain the properties of the MOSFET under different working

conditions. For machine learning method, we need to use a large number of data to train the model. According to Chapter 2, we have established an accurate FE model. So we can obtain data by simulation.

When a power device is put into operation, the heat dissipation capability of the heat sink keeps basically unchanged. According to [45], the convective heat transfer coefficient for the bottom surface is set as $h_{ca}=8000\text{W}/(\text{m}^2\cdot\text{K})$. In steady state, we think the case temperature is as the same as the ambient temperature. So we can change the ambient temperature to change the case temperature. Based on the analysis in Section 3.1 and Section 3.3, we need to obtain the R_{on} , T_c and I_d under various conditions. For this reason, we set different sets of R_{on} , T_c and I_d in simulation.

In order to obtain the data with a different aging degree, 5 sets of simulation with different solder layer area are preset. Because of the criterion for solder layer failure, the range of $\Delta Z_{jc}/Z_{jc}$ is set as 0~20%. Taking the interval as 5°C , the ambient temperature range is set as from -30°C to 80°C for each model. The on-current is set from 5A to 50A with the same interval. By using the parameters scanning study in COMSOL, we obtained 2500 sets of data after removing some wrong data.

4.2.2 Rules for Classification Intervals

Statistical studies on a large number of device failure data show that the failure rate curve is similar to the bathtub curve [46]. The curve consists of three stages, as shown in Figure 4.6. The first period, called early failure rate (EFR), is related to the initial defect caused by manufacturing. The second stage is called the intrinsic failure rate (IFR) period. In this period, the failure rate relates to intermittent overloads. The last period has a high failure rate, called the wear-out period. After the long-term operation, the performance of the device degrades due to the accumulation of the fatigue. In this period, the failure rate shows an exponential trend. The main task of condition monitoring is to measure the change process of electrical and

thermal parameters during the wear out period to judge the health of the device.

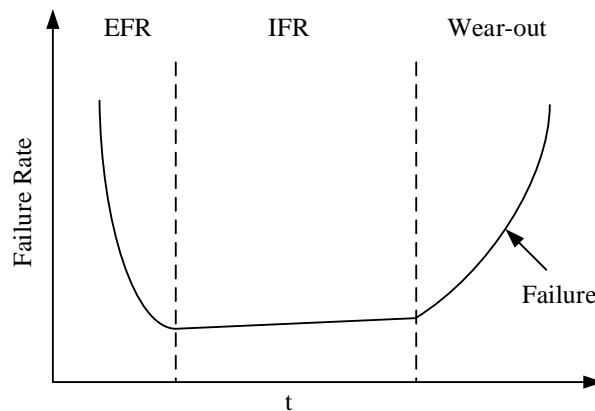


Figure 4.3 Failure Rate Curve

According to the division method in [9], the health state is divided into five levels. Due to the failure rate curve, the intervals do not have the same size. When $\Delta Z_{jc}/Z_{jc}$ reaches 20%, the corresponding growth rate of on-resistance $(\Delta R_{on}/R_{on})_F$ is regarded as the criterion for failure. So the intervals are $0.15(\Delta R_{on}/R_{on})_F$, $0.35(\Delta R_{on}/R_{on})_F$, $0.55(\Delta R_{on}/R_{on})_F$, $0.75(\Delta R_{on}/R_{on})_F$ and $(\Delta R_{on}/R_{on})_F$ respectively. We take those as the indication for each state of the device, as shown in Table 4.1. And the aging rate is defined as the percentage of $\Delta R_{on}/R_{on}$ and $(\Delta R_{on}/R_{on})_F$, as follow:

$$f = \frac{\Delta R_{on}/R_{on}}{(\Delta R_{on}/R_{on})_F} \quad (4.6)$$

Table 4.1 Classification Intervals for Healthy State

Level	Healthy State	Aging Degree	Intervals
I	Healthy	$0 \leq f \leq 0.15$	$0 \leq g \leq 0.15(\Delta R_{on}/R_{on})_F$
II	Light Aging	$0.15 < f \leq 0.35$	$0.15(\Delta R_{on}/R_{on})_F < g \leq 0.35(\Delta R_{on}/R_{on})_F$
III	Moderate Aging	$0.35 < f \leq 0.55$	$0.35(\Delta R_{on}/R_{on})_F < g \leq 0.55(\Delta R_{on}/R_{on})_F$
IV	Severe Aging	$0.55 < f \leq 0.75$	$0.55(\Delta R_{on}/R_{on})_F < g \leq 0.75(\Delta R_{on}/R_{on})_F$
V	Failure	$0.75 < f \leq 1$	$0.75(\Delta R_{on}/R_{on})_F < g \leq (\Delta R_{on}/R_{on})_F$

According to the criteria in Table 4.1, the aging degree is divided for all the sample data, as shown in Table 4.2.

Table 4.2 Healthy Condition of Characteristic Parameters

Rank	I_d (A)	T_c (°C)	R_{on} (mΩ)	$\Delta Z_{jc}/Z_{jc}$	$\Delta R_{on}/R_{on}$	f	Level
1	5	-30.0	38.22	0	0	0	I
2	5	-30.0	39.62	2.27%	1.13%	0.031	I
3	5	-30.0	42.38	4.85%	6.29%	0.209	II
4	5	25.0	80.03	3.39%	6.74%	0.046	I
5	5	25.0	105.19	17.43%	22.71%	0.703	IV
6	5	25.0	128.32	20.32%	31.28%	1	V
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2500	50	80	231.09	20.11%	132.37%	1	V

The characteristic parameters obtained by the simulation are used as the raw data of the evaluation model. The 2000 sets of data in Table 4.2 were randomly selected for training. And 170 sets of data were randomly selected as the test samples.

4.2.3 Structure of the Model

When using ANFIS algorithm to evaluate the state of MOSFET devices, there are two main steps. First, some data after filtering are used to train the network and establish an effective fuzzy system model. The relationship between the input and output is simulated. Second, the trained network is used to predict the result of the test data. Then the accuracy and validity of the model are evaluated.

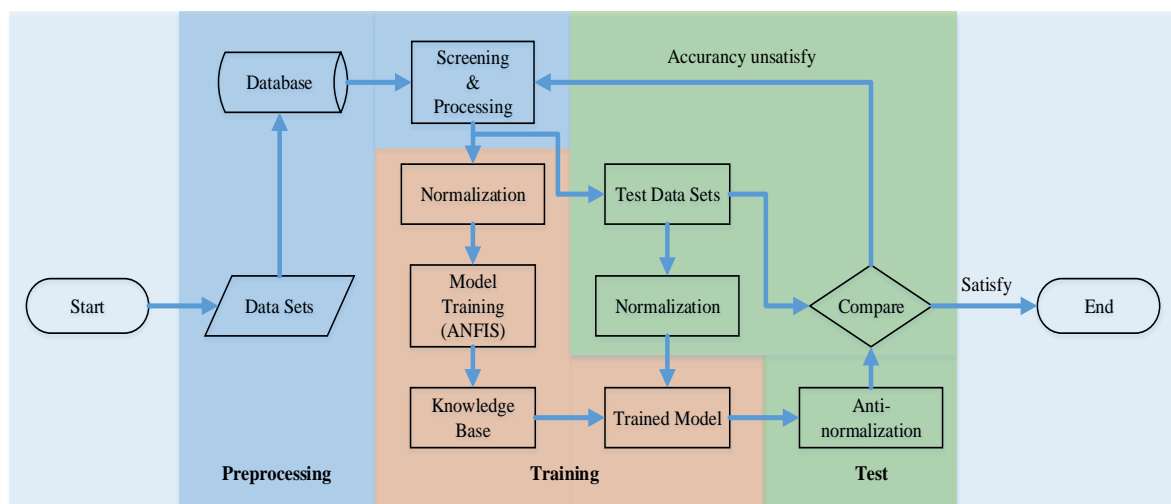


Figure 4.4 Flow Chart of the Evaluation Model

According to the previous analysis, we select the case temperature T_c , on-current I_d and on-resistance R_{on} as the input parameters. And the aging degree f is selected as the output. So, there are 3 input nodes and 1 output node. The specific process is shown in Figure 4.4.

4.3 Results Analysis and Comparison

4.3.1 Results Analysis

In the training process, this paper uses the Gaussian function as the membership function and set the training trial is 500. And 170 sets of data selected randomly were test sets and were used to test the accuracy and validity of the model. It can be seen from Figure 4.5 that the root mean square error (RMSE) decreases rapidly during the first 100 training sessions. And then it gradually approaches the convergence at a small rate. After 500 sessions, the training error is 0.0118. Figure 4.6 shows the distribution of the absolute error between the actual aging degree and the predicted aging degree of the test samples. It can be seen that the maximum error is less than 0.08, which is an acceptable value. At the same time, most of the errors are less than 0.02. So we can think the trained model has high accuracy and can effectively predict the aging state of the device.

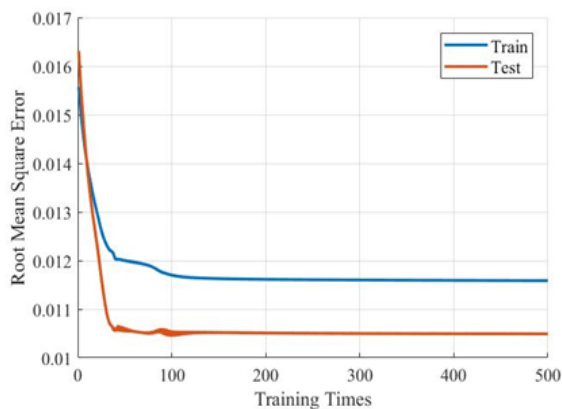


Figure 4.5 RMSE during Training

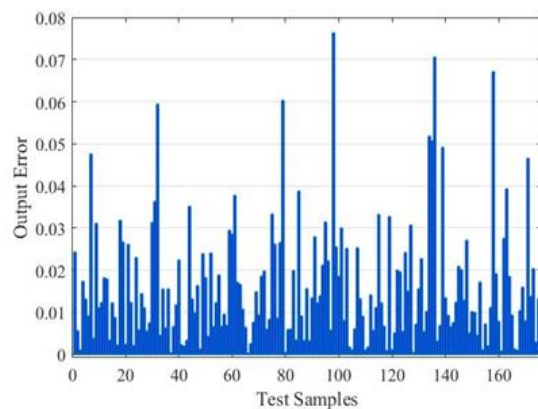


Figure 4.6 Error between Predicted and Tested Data

Figure 4.7 shows the results of aging state obtained by ANFIS. It can be seen that the aging degree given by the evaluation model is basically consistent with the actual situation. All

the predicted output are close to the actual state with a reasonable error range. Figure 4.8 is confusion matrixes of the output. It shows the differences between the true classes and predicted classes. From that, we notice that there are only 7 errors among 170 sets of test data. Besides that, the accuracy for each level is high enough. And there is no error more than two levels. The lowest accuracy for all classes is 88.89%. The accuracy of the evaluation model is 96%, which is acceptable for evaluation models and engineering applications. In summary, the healthy state of the MOSFET can be evaluated by the model proposed in this paper.

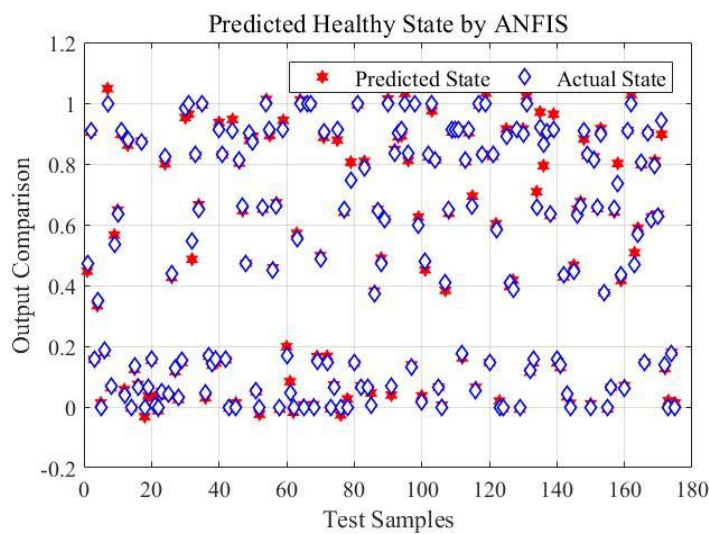


Figure 4.7 Results of Aging Degree

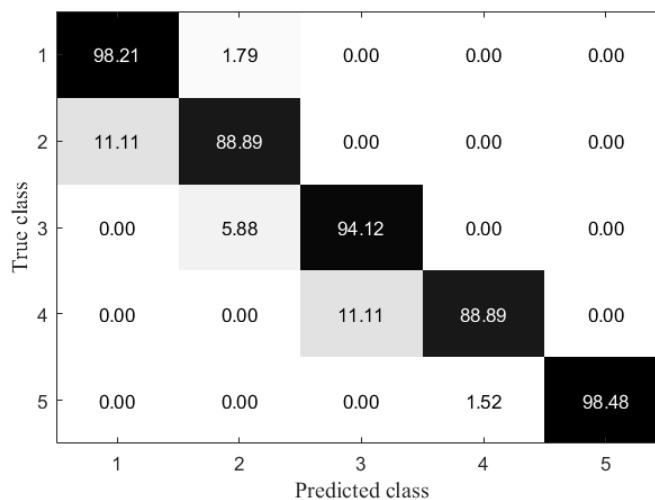
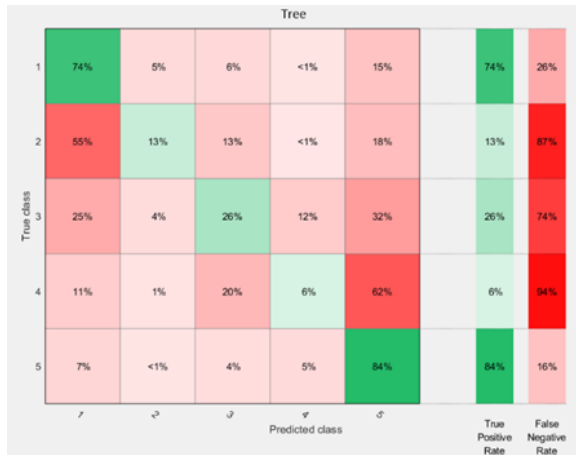


Figure 4.8 Confusion Matrix of the Model Output

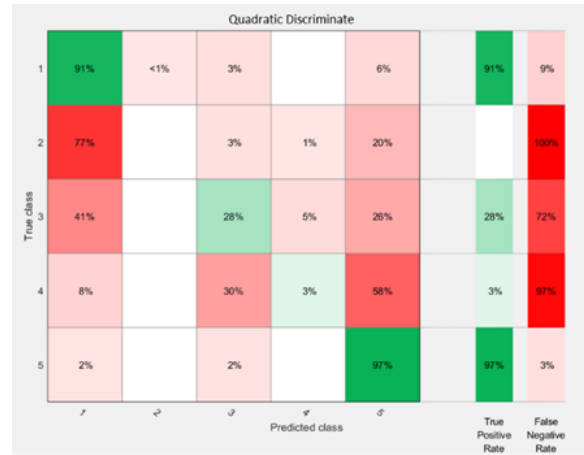
4.3.2 Comparison of Common Classification Algorithms in Matlab

In Matlab, there are lots of artificial intelligence algorithms have been contained in its

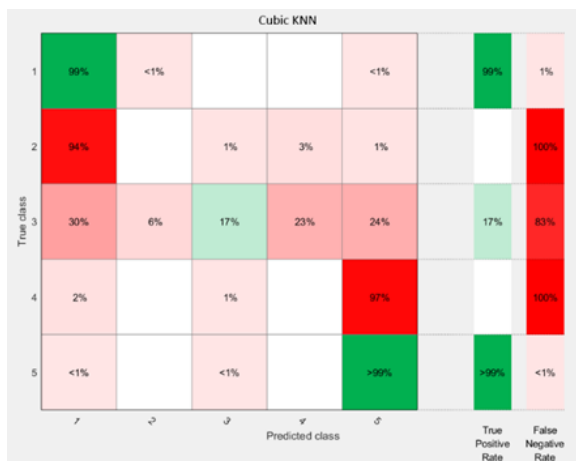
toolbox. Using the classifier application in Matlab, all classification algorithms are compared. The results are shown as follows. They are decision tree, quadratic discriminant, cubic k-nearest neighbors (KNN), bagged tree, support vector machine (SVM) and quadratic SVM, respectively.



(a) Decision Tree



(b) Quadratic



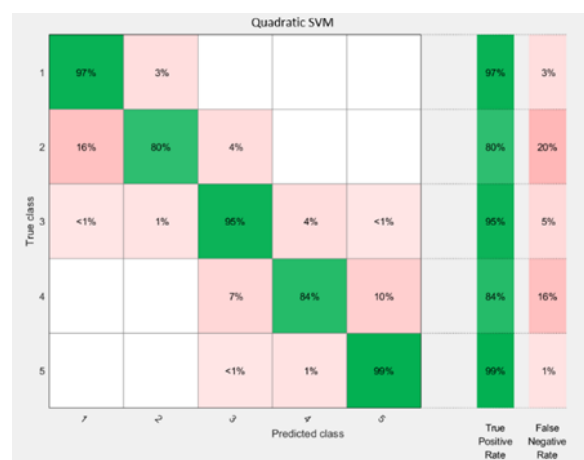
(c) Discriminant



(d) Cubic KNN



(e) SVM



(f) Quadratic SVM

Figure 4.9 Confusion Matrixes of Common Classification Algorithms

Figure 4.9 (a) shows the result of the decision tree. We can see it has a bad accuracy, especially for the recognition from level II to level IV. From (b) and (c), we can notice that they have a pretty high accuracy of discrimination for level I and level V. But they can hardly distinguish level II and level IV. Even though they can tell level III, the accuracy is only around 26%. For (d) and (e), they show better performance than the formers. However, they also show low accuracy of discrimination for level II and level IV. The last one, quadratic SVM, has the highest accuracy among the six algorithms. The accuracy of quadratic SVM in this model is about 94.1%. Nevertheless, it is worse than ANFIS. All the accuracy of them is listed in Table 4.3.

Table 4.3 Results of the Common Classification Algorithms

Accuracy Algorithms	I	II	III	IV	V	Total
Decision Tree	74%	13%	26%	6%	84%	58.6%
Quadratic Discriminant	91%	NaN ¹	28%	3%	97%	67.1%
Cubic KNN	99%	NaN	17%	NaN	99%	68.9%
Bagged Tree	92%	32%	49%	24%	97%	75.2
SVM	99%	36%	83%	57%	99%	87.1%
Quadratic SVM	97%	80%	95%	84%	99%	94.1%
ANFIS	98%	89%	94%	89%	99%	96.0 %

¹ NaN: No value in here.

Chapter 5 Conclusion

MOSFET as the core component in a huge of power devices, researches on its performance, the aging process and state evaluation are extremely significant for maintenance and improving reliability. Works in this paper focus on the failure mechanism in the solder layer. Because of the low melting point of the solder layer, its reliability and failure process is pretty important.

In this thesis, we built the multiphysics coupling model in COMSOL software. The temperature dependence and viscoplasticity are considered for accurate simulation, which is closer to the actual operation condition of the MOSFET. The effects of voids in different location of the solder layer are studied in detail. And the solder layer fatigue, relationship between on-resistance and thermal resistance are analyzed. With the increase of voids area and fatigue degree of solder layer, the junction temperature, case temperature, stress and strain have an obvious rise. Meanwhile, the on-resistance and thermal resistance increased. And the growth rate of on-resistance is distinctly larger than that of thermal resistance. Because they have the same trend, the thermal resistance can be replaced by on-resistance as the criterion for the failure of MOSFET.

Based on those results, a state evaluation model using ANFIS was established. By validation and comparison with some common classification algorithms, the model was considered to have high accuracy and can be used to evaluate the healthy state of the MOSFET.

5.1 Suggestion for Future Work

We only consider the relation between thermal resistance and on-resistance. For the working environment, only the ambient temperature was introduced to the FE model. Humidity and vibration are very important in some case, which may cause a big error. The strain rate and

creep rate have a large influence on the deformation, which will bring some change from mechanical field to thermal field and current field. The differences among materials are not studied in this thesis.

For machine learning method, a large amount of data are needed. More characteristic parameters, like power fluctuation, switching frequency and history data, can be considered. Big data method can be introduced to the research to find more links between parameters to improve the accuracy and expand the scope of application.

References

1. Chakraborty, Arindam. "Advancements in power electronics and drives in interface with growing renewable energy resources." *Renewable and Sustainable Energy Reviews* 15.4 (2011): 1816-1827.
2. Bing Gao. "Study on Failure Evaluation Method of IGBT Module based on Temperature Gradient and Statistic Characteristic." (2017)(In Chinese)
3. Yang, Shaoyong, et al. "An industry-based survey of reliability in power electronic converters." *IEEE transactions on Industry Applications* 47.3 (2011): 1441-1451.
4. Wolfgang, E. "Examples for failures in power electronics systems." *ECPE tutorial on reliability of power electronic systems, Nuremberg, Germany* (2007): 19-20.
5. Ciappa, Mauro, and Alberto Castellazzi. "Reliability of high-power IGBT modules for traction applications." *IEEE 45th Annual International Reliability Physics Symposium*. 2007.
6. Morozumi, Akira, et al. "Reliability of power cycling for IGBT power semiconductor modules." *IEEE Transactions on Industry Applications* 39.3 (2003): 665-671.
7. Ming Chen, et al. "Failure mechanism and life prediction model for MOSFET." *Journal of Xi'an Jiaotong University*. "45.10 (2007):480-485.
8. Riedel, G. J., et al. "Reliability of large area solder joints within IGBT modules: Numerical modeling and experimental results." *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*. IEEE, 2012.
9. Lai, Wei, et al. "Low ΔT_j Stress Cycle Effect in IGBT Power Module Die-Attach Lifetime Modeling." *IEEE Transactions on Power Electronics* 31.9 (2016): 6575-6585.
10. Scheuermann, Uwe, and U. Hecht. "Power cycling lifetime of advanced power modules for different temperature swings." *PCIM Nuremberg* 5964 (2002).
11. Bayerer, Reinhold, et al. "Model for power cycling lifetime of IGBT modules-various factors influencing lifetime." *Proc. CIPS*. Vol. 11. 2008.
12. Kovacevic, I. F., Uwe Drofenik, and Johann W. Kolar. "New physical model for lifetime estimation of power modules." *The 2010 International Power Electronics Conference-ECCE ASIA*-. IEEE, 2010.
13. Ciappa, Mauro. "Selected failure mechanisms of modern power modules." *Microelectronics reliability* 42.4-5 (2002): 653-667.
14. Firouz, Yousef, Mohammad Tavakoli Bina, and Bahman Eskandari. "Efficiency of three-level neutral-point clamped converters: analysis and experimental validation of power losses, thermal modelling and lifetime prediction." *IET Power Electronics* 7.1 (2014): 209-219.
15. Lau, John H., and Peter A. Engel. "Solder Joint Reliability—Theory and Applications." (1992): 100-100.
16. Ramminger, S., N. Seliger, and G. Wachutka. "Reliability model for Al wire bonds subjected to heel crack failures." *Microelectronics Reliability* 40.8-10 (2000): 1521-1525.
17. Morrow, JoDean. "Cyclic plastic strain energy and fatigue of metals." *Internal friction, damping, and cyclic plasticity*. ASTM International, 1965.
18. de Filippis, Stefano, et al. "ANSYS based 3D electro-thermal simulations for the evaluation of power MOSFETs robustness." *Microelectronics Reliability* 51.9-11 (2011): 1954-1958.

19. Zheng, Libing, et al. "Investigation of the temperature character of IGBT solder delamination based the 3-D thermal-electro coupling FEM." *2010 Asia-Pacific Power and Energy Engineering Conference*. IEEE, 2010.
20. Yang, Shaoyong, et al. "Condition monitoring for device reliability in power electronic converters: A review." *IEEE Transactions on Power Electronics* 25.11 (2010): 2734-2752.
21. Xiang, Dawei, et al. "Monitoring solder fatigue in a power module using case-above-ambient temperature rise." *IEEE Transactions on Industry Applications* 47.6 (2011): 2578-2591.
22. Eleffendi, Mohd Amir, and C. Mark Johnson. "Evaluation of on-state voltage $V_{CE(ON)}$ and threshold voltage V_{TH} for real-time health monitoring of IGBT power modules." *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*. IEEE, 2015.
23. Bęczkowski, Szymon, et al. "Online V_{ce} measurement method for wear-out monitoring of high power IGBT modules." *2013 15th European Conference on Power Electronics and Applications (EPE)*. IEEE, 2013.
24. Xiong, Yali, et al. "Prognostic and warning system for power-electronic modules in electric, hybrid electric, and fuel-cell vehicles." *IEEE Transactions on Industrial Electronics* 55.6 (2008): 2268-2276.
25. Gao, Bing, et al. "A temperature gradient-based potential defects identification method for IGBT module." *IEEE Transactions on Power Electronics* 32.3 (2017): 2227-2242.
26. Ryan, Michael John. "Method and apparatus for power electronics health monitoring." U.S. Patent No. 6,405,154. 11 Jun. 2002.
27. Zhu, Chunyang, and Qiyi Guo. "Real-time recognition temperature state based on ga-bp algorithm [J]." *Computer Simulation* 2 (2011): 53.
28. Mohagheghi, Salman, et al. "Condition monitoring of power electronic circuits using artificial neural networks." *IEEE Transactions on power electronics* 24.10 (2009): 2363-2367.
29. Knoerr, Matthias, Silke Kraft, and Andreas Schletz. "Reliability assessment of sintered nano-silver die attachment for power semiconductors." *2010 12th Electronics Packaging Technology Conference*. IEEE, 2010.
30. Yang, Yongheng, et al. "Design for reliability of power electronic systems." *Power Electronics Handbook*. Butterworth-Heinemann, 2018. 1423-1440.
31. Brown, Stuart B., Kwon H. Kim, and Lallit Anand. "An internal variable constitutive model for hot working of metals." *International journal of plasticity* 5.2 (1989): 95-130.
32. Zhang, Liang, et al. "Reliability of lead-free solder joints in CSP device under thermal cycling." *Journal of Materials Science: Materials in Electronics* 25.3 (2014): 1209-1213.
33. Cheng, Z. N., et al. "Viscoplastic Anand model for solder alloys and its application." *Soldering & Surface Mount Technology* 12.2 (2000): 31-36.
34. Yu, Qiang, and Masaki Shiratori. "Fatigue-strength prediction of microelectronics solder joints under thermal cyclic loading." *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A* 20.3 (1997): 266-273.
35. Wu, Wuchen, et al. "Thermal stress related packaging failure in power IGBT modules." *Proceedings of International Symposium on Power Semiconductor Devices and IC's: ISPSD'95*. IEEE, 1995.
36. Deng, Hongfei, et al. "Simulation Research on IGBT Thermal Impact of Solder Voids Based on Fractal Theory." *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*. IEEE, 2018.
37. Dodd, Paul E., and Lloyd W. Massengill. "Basic mechanisms and modeling of single-event upset in digital microelectronics." *IEEE Transactions on Nuclear Science* 50.3 (2003): 583-602.

38. Wu, Wuchen, et al. "Thermal reliability of power insulated gate bipolar transistor (IGBT) modules." *Twelfth Annual IEEE Semiconductor Thermal Measurement and Management Symposium. Proceedings*. IEEE, 1996.
39. Xiang, Dawei, et al. "Monitoring solder fatigue in a power module using case-above-ambient temperature rise." *IEEE Transactions on Industry Applications* 47.6 (2011): 2578-2591.
40. Gorecki, Krzysztof, and Janusz Zarebski. "Nonlinear compact thermal model of power semiconductor devices." *IEEE Transactions on Components and Packaging Technologies* 33.3 (2010): 643-647.
41. Wu, Rui, et al. "A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations." *IEEE Transactions on Industry Applications* 52.4 (2016): 3306-3314. Avenas, Yvan, et al. "Condition monitoring: A decade of proposed techniques." *IEEE Industrial Electronics Magazine* 9.4 (2015): 22-36.
42. Jang, J-SR. "ANFIS: adaptive-network-based fuzzy inference system." *IEEE transactions on systems, man, and cybernetics* 23.3 (1993): 665-685.
43. Sobhani, Jafar, et al. "Prediction of the compressive strength of no-slump concrete: A comparative study of regression, neural network and ANFIS models." *Construction and Building Materials* 24.5 (2010): 709-718.
44. Bahman, Amir Sajjad, Ke Ma, and Frede Blaabjerg. "A lumped thermal model including thermal coupling and thermal boundary conditions for high-power IGBT modules." *IEEE Transactions on Power Electronics* 33.3 (2018): 2518-2530.
45. Lehmann, Jan, et al. "Method for electrical detection of bond wire lift-off for power semiconductors." *ISPSD'03. 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs, 2003. Proceedings.. IEEE, 2003.*