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A Fault-Tolerant Control Strategy for Three-level Neutral-Point Clamped (NPC) Inverter

Weijun Zhu
University of Wisconsin-Milwaukee

A FAULT-TOLERANT CONTROL STRATEGY FOR THREE-LEVEL NEUTRAL-POINT CLAMPED (NPC) INVERTER

by

Weijun Zhu

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ABSTRACT

A FAULT-TOLERANT CONTROL STRATEGY FOR THREE-LEVEL NEUTRAL-POINT CLAMPED (NPC) INVERTER

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The University of Wisconsin-Milwaukee, 2019
Under the Supervision of Dr. Lingfeng Wang

When the open-circuit fault occurs on neutral-point clamped (NPC) inverters, it can cause the distortion of output currents, excessively large fluctuation of output voltages, and unbalanced neutral-point potential. Currently, several existing fault diagnosis methods are able to identify the fault types, but they are unable to identify the switching devices where the open-circuit faults occur. Furthermore, even if the open-circuit faults can be identified, the implications caused by open-circuit faults need to be further addressed. This thesis is focused on diagnosing the open-circuit faults and mitigating the problems caused by these faults.

An effective fault diagnosis method is proposed in his study to identify the switching devices where the open-circuit faults occur. The characteristics of different distorted currents are firstly analyzed. By normalizing the sampling currents, calculating the average currents and comparing them with thresholds, different faulty switching devices can all be identified. To address the issues caused by these faults, a fault-tolerant control strategy is proposed. By replacing the impossible space vectors caused by these faults with other vectors which can generate the same output voltages, the problems of distortion of output currents and excessively

large fluctuation of output voltages can be solved. But the excessively large difference of neutral-point potential still exists.

To address the above issue, a model predictive control strategy is proposed to solve the problem of excessively large difference of neutral-point potential. A cost function is built to track the reference vector and suppress the difference of neutral-point potential. The Lagrange function is used to solve the action times of different space vectors. Furthermore, it is shown that when the neutral-point potential is initially unbalanced, the developed strategy is still able to make the potential balanced and greatly reduce its fluctuation.

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Chapter 1 Introduction

1.1Research Background

Nowadays, because of energy shortages and environmental crises, human's demanding for sustainable and clean energy has promoted the development of renewable energy [1]. Solar cells, wind power as major renewable energy are widely used in power generation systems [2-3]. These renewable energy systems have brought about tremendous changes to the infrastructure of the power grid shown in Fig. 1-1.

On the generation side, power converters can work as the interaction between power generation and grid; for power transmission and distribution, converters work as the key part of HVDC power transmission and Flexible AC Transmission Systems; for power consumption, power converters can work as driving device of conveyer belts, compressors, motors, and so on. Thus, there is a high need to study converters.

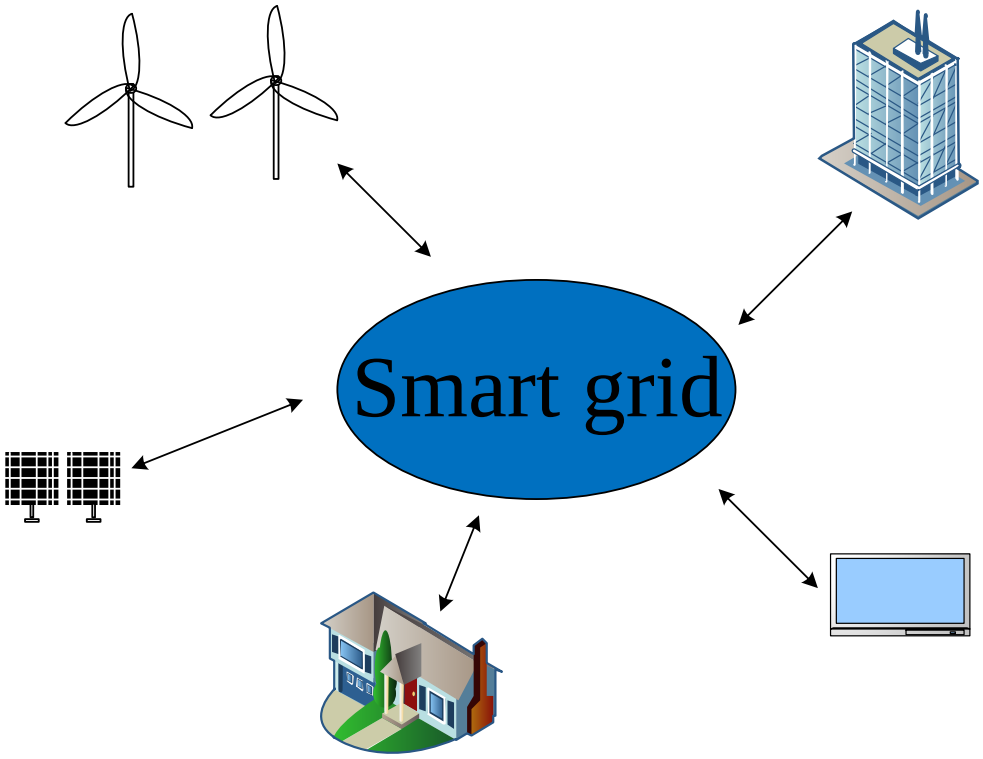


Fig. 1- 1 Infrastructure of smart grid

Multilevel inverters are widely applied in medium voltage applications because of their low output harmonic contents and high breakdown voltages. Also, they are attractive in low-voltage applications due to smaller *dv/dt*, smaller switching loss than two-level inverters [4-6].

Three-level inverter outputs phase voltages with three states and line-line voltages with five states as shown in Fig. 1-2. Because of the increasing levels, its total harmonic distortion (THD) decreases. Thus, it has smaller output filter size and can operate at low-voltage stress.

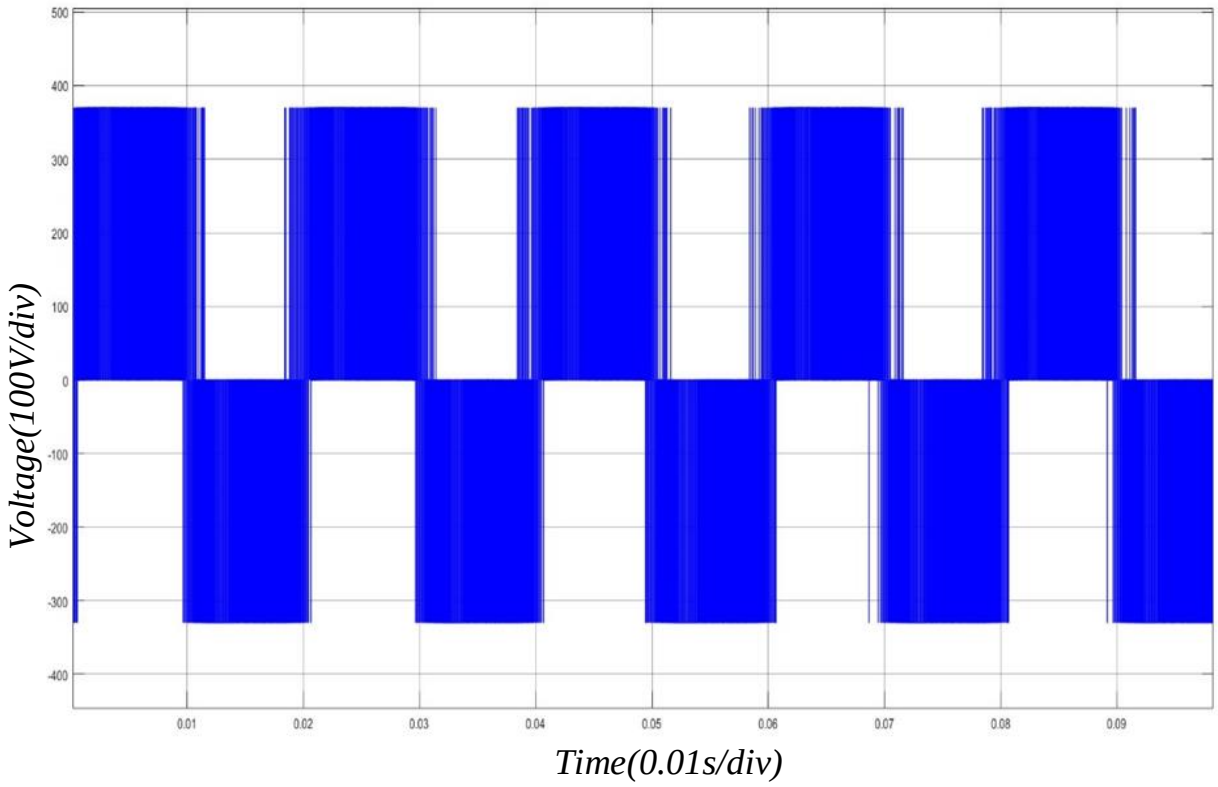


Fig. 1- 2 Phase voltage

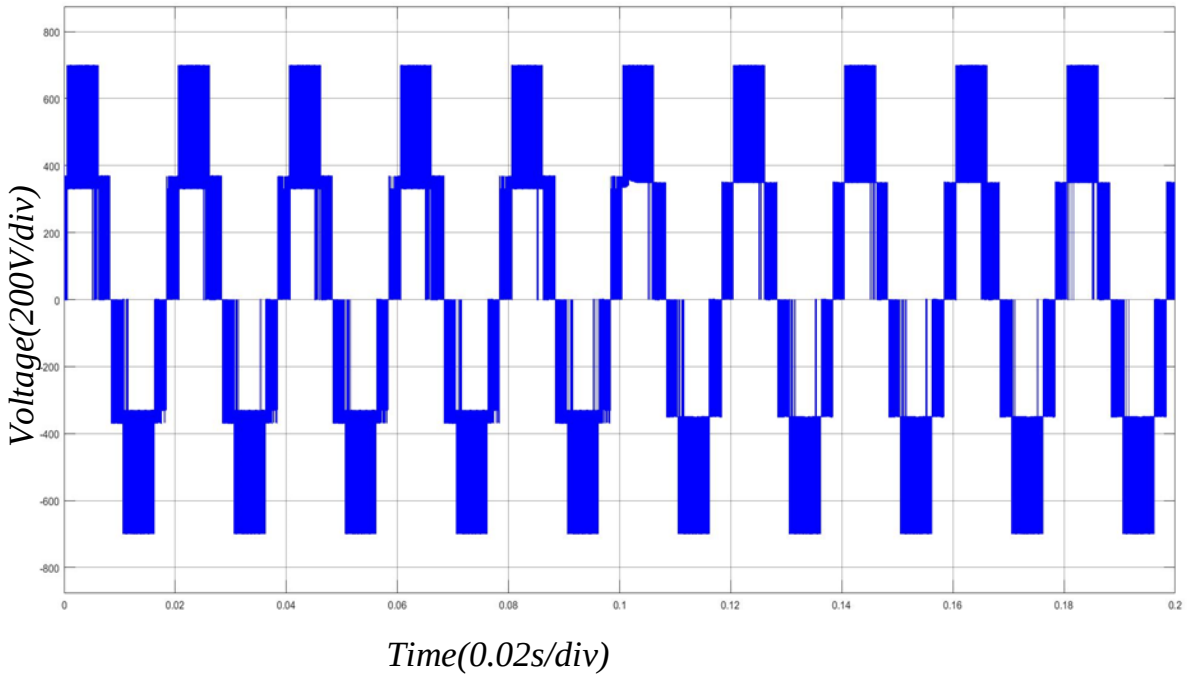


Fig. 1- 3 line-line voltage

1.2 Multi-Level Topologies

In general, multi-level inverter has four kinds of topologies, including Flying-Capacitor (FC) inverter, Neutral-Point Clamped (NPC) inverter, cascaded multilevel inverter and hybrid inverter.

1.2.1 NPC Inverter and FC Inverter

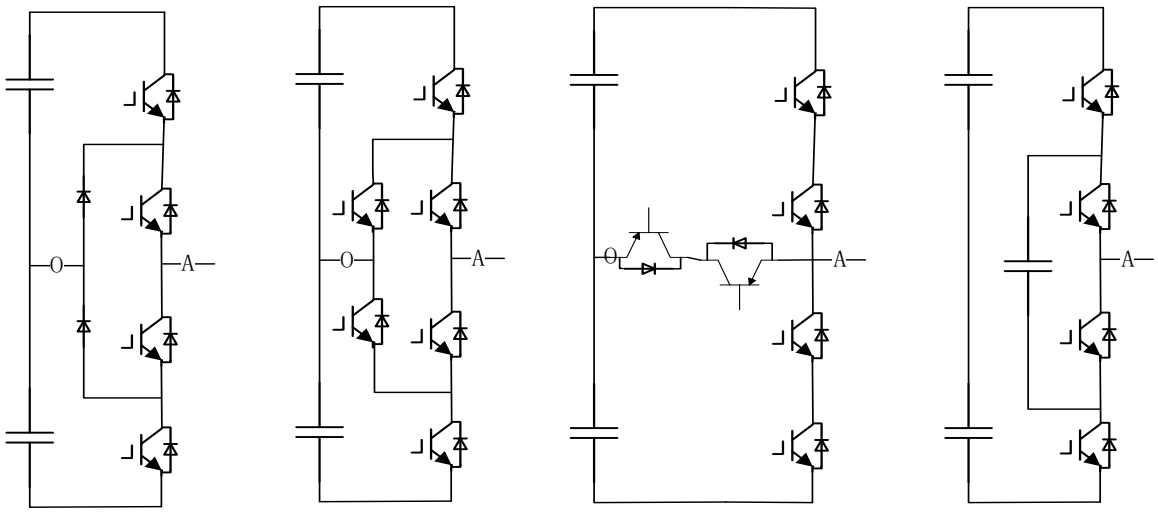
NPC inverter and FC inverter have similar characteristics. For NPC inverter, it has three kinds of topologies, including active inverter, diode clamped inverter and T-type inverter, shown in Fig. 1-4. A.Nabae proposed three-level diode clamped inverter in 1980 [7]. The two diodes can be replaced by two active switching tubes and then called active inverter shown in Fig. 1-4(b). The neutral point and output also can be connected by two switching tubes shown in Fig. 1-4(c) and named T-type inverter [8-10]. This topology has fewer switching devices and is easily controlled.

FC inverter has some similar characteristics with diode clamped inverter, such as: topology,

control strategy and so on. And it can output voltages with three level through the parallel capacitor, shown in Fig. 1-4(d).

Even though T-type inverter reduces its switching devices, it increases its voltage stress twice as much as that of active inverter. When T-type inverter and diode clamped inverter work, the unbalanced capacitor voltages can increase harmonic distortion of the output currents. Even though FC inverter doesn't have such problem, it also needs additional strategies to make the voltage of the flying capacitor half of that on the DC side.

Fig. 1-5 shows that two-level active inverter is developed into five-level active inverter. The law of this kind of inverter is generally that $2(k-1)$ switching tubes and $(k-1)(k-2)$ diodes are needed to generate k levels. It is obvious that the more the levels, the more switching devices needed and the more complicated the system. Thus, the problem of unbalanced loss is more serious.



(a) (b) (c) (d)

Fig. 1- 4 Inverter topologies: (a) diode clamped inverter; (b) active neutral-point clamped inverter; (c) T-type inverter; (d) flying-capacitor inverter

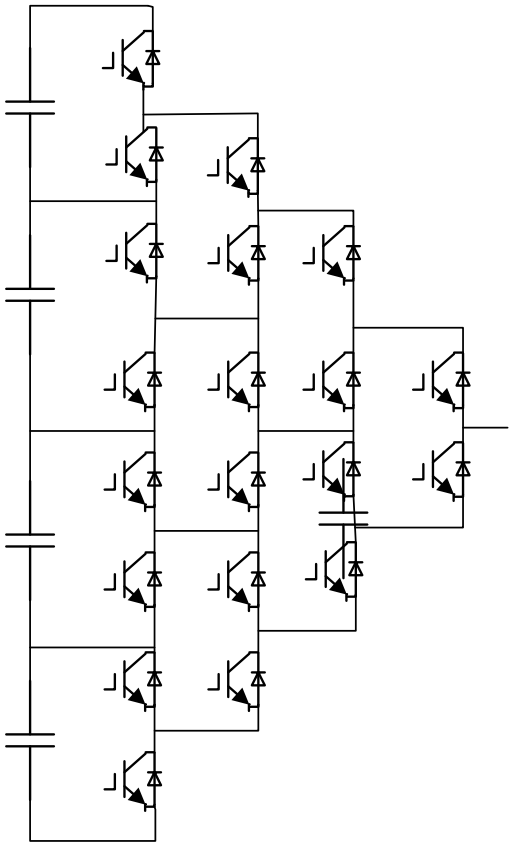
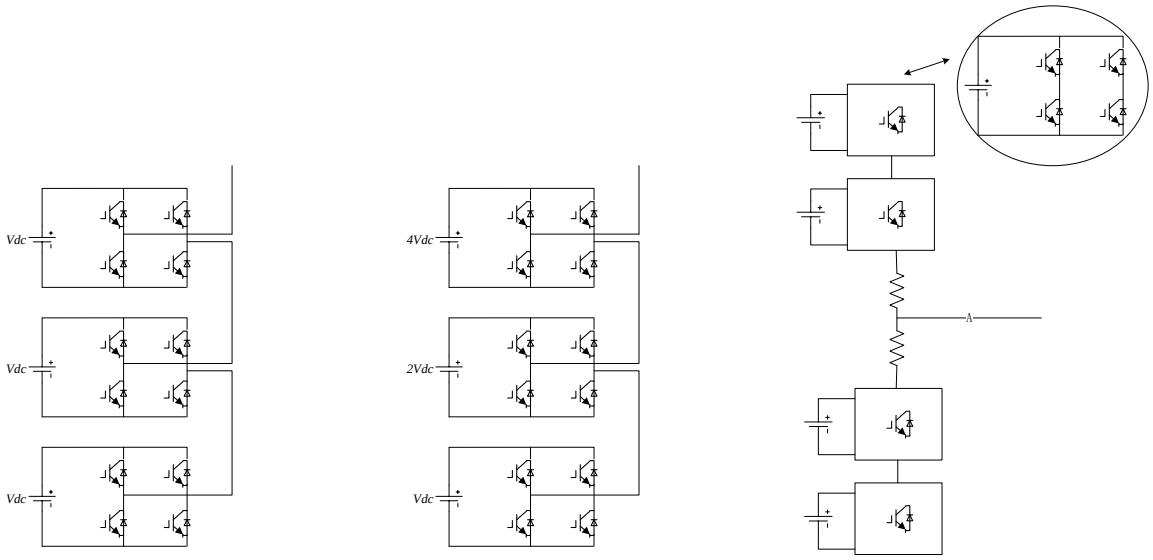


Fig. 1- 5 Phase leg of five-level active neutral-point clamped inverter

1.2.2 Cascade Multilevel Inverter

Cascade Multilevel Inverter is also widely used. The basic unit of single-phase cascaded multilevel inverter is a two-level inverter. And with number of basic units increasing, the number of output levels also increases. So cascaded multilevel inverter is very suitable for high voltage and high power applications [11].

Fig. 1-6 shows the Cascaded H-Bridge (CHB) multi-level inverter. Each phase has *N* units and can generate *2N+1* levels [12]. Fig. 1-6(b) shows asymmetric cascaded inverter whose legs have different DC voltages. If it has *N* units, it can generate $2^{N+1}-1$ levels. But because of these different parallel voltages, different switching devices have different voltage stress. Fig. 1-6(c) shows the modular multilevel with two legs on each phase and it can generate $2N-1$ levels.



(a) (b) (c)

Fig. 1- 6 Cascaded multilevel inverter: (a) cascaded H-Bridge inverter; (b) asymmetric cascaded inverter; (c) Modular multilevel inverter

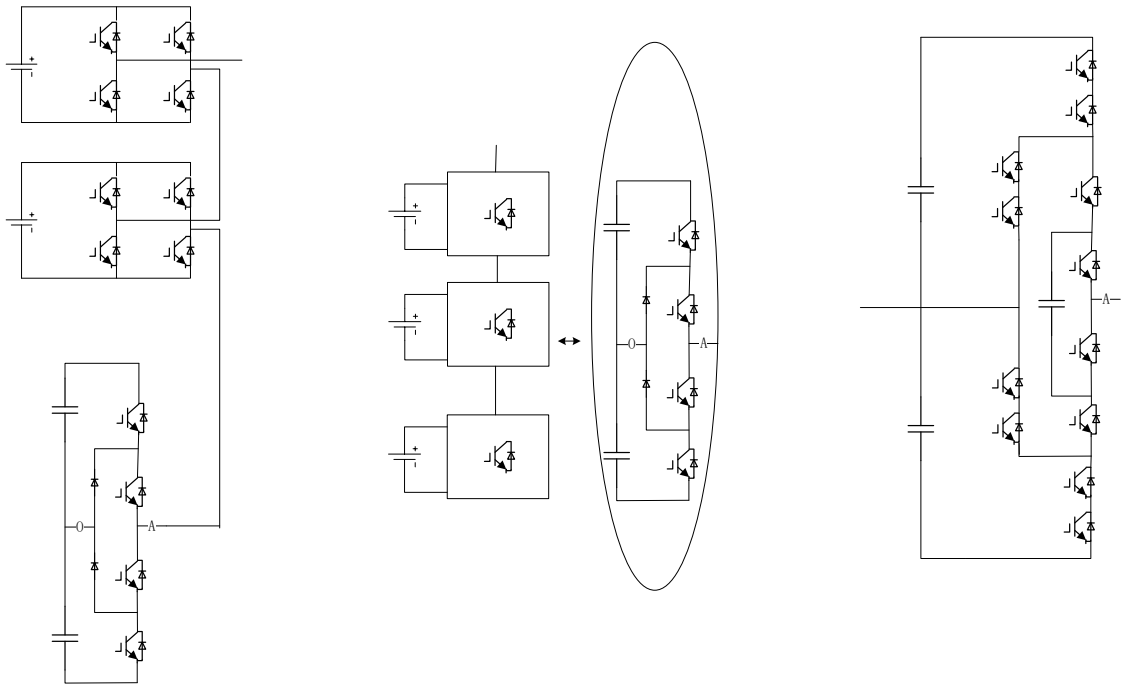
1.2.3 Hybrid Inverter

Hybrid inverter is designed by combining inverter topologies mentioned above. Fig. 1-7(a) shows the topology combined by NPC topology and CHB topology. The power for NPC part is supplied by DC source and the power for CHB part is supplied by the capacitor. The more CHB units, the more levels generated. Because of the NPC units, the problem of unbalanced neutral-point potential also exists.

Fig. 1-7(b) shows cascaded NPC-H bridge inverter. Each NPC unit in the topology can generate five levels. The inverter can generate much more levels with very small amounts of basic units [13-14]. But it also has the problem of unbalanced neutral-point potential because it has NPC units.

Fig. 1-7(c) shows the hybrid topology combined by ANPC topology and FC topology [15]. This inverter has the advantages of less complicated topology structure and amounts of switching devices. It can generate 5 levels with 12 switching tubes and 3 capacitors needed.

However, for this topology, the loss and voltage stress are extremely unbalanced.



(a) (b) (c)

Fig. 1- 7 Hybrid inverter: (a) NPC+CHB; (b) cascaded NPC; (c) ANPC+FC

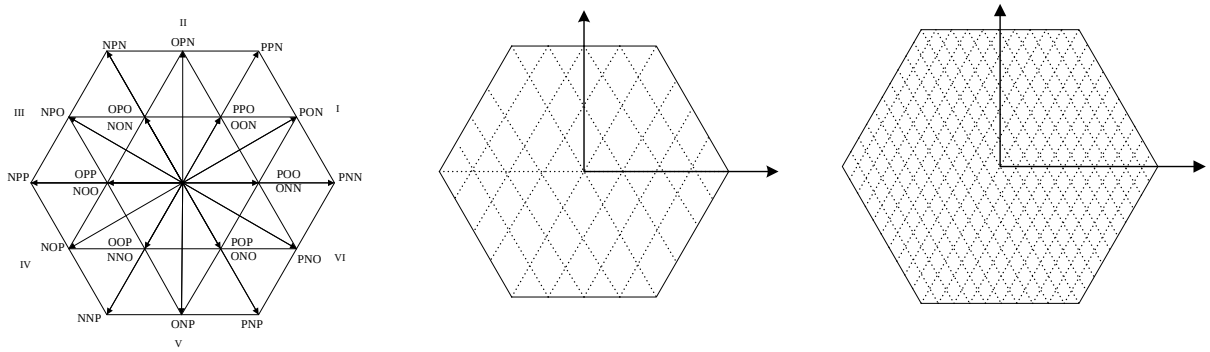
1.3 Control Strategy

The control strategies play an important role in determining the performance of inverters. Here show the main control strategies, including space vector pulse width modulation, fault tolerant control strategy and model prediction control strategy.

1.3.1 Space Vector Pulse Width Modulation (SVPWM)

SVPWM is widely used among multilevel inverters as it can decrease its total harmonic distortion [16-27]. For three-level inverter, it has 27 voltage space vectors shown in Fig. 1-8(a). Fig. (c) and (b) show the voltage space vector distribution of five-level inverter and eleven-level inverter respectively. The switching states are three times of the voltage levels. The higher levels cause the difficulty in calculating the action times of those voltage space vectors. But the space vector control strategy is very suitable to three-level inverter because of its simple

topology structure and small amounts of vectors.



(a) (b) (c)

Fig. 1- 8 Space vector hexagon for multilevel: (a) three-level; (b) five-level; (c) eleven-level

1.3.2 Fault Diagnosis

The open-circuit fault can cause serious damage to inverters as it can not only reduce performance of inverters, but also lead to distortion of the output currents and unbalanced neutral-point potential. So, it is important to study the fault diagnosis strategy.

A lot of scholars have proposed some fault diagnosis method, some of which detect whether fault occurs by analyzing the output currents [28-32]. Because of the output current with distortion when open-circuit fault occurs. These current methods include Park's transformation, average current and so on.

[33] applies current vector to do the fault detection and fault diagnosis. But for NPC inverter which has two switching tubes and one diode on upper and lower leg respectively, it can just identify faulty part, but can't identify to which device the fault occurs.

[34] uses slope method to identify the faulty switch because different faulty switches have different characteristics. But this method is only suitable to inverters in the power generation side and cannot detect faults in the grid side.

In [35], current sensors are needed to detect the faulty switch, which is achieved by measuring the currents and comparing them with normal currents.

1.3.3 Fault Tolerance

In [36], replacing switching states with others is applied to solve faulty states. When open-circuit fault occurs, one switching state and some voltage space vectors can't be generated. But when modulation ratio is small enough, some impossible small voltage space vectors can be replaced by the others which can generate the same output voltages. But when modulation ratio become larger and medium vectors are involved into vector composition, this method can't work because each sector has only one medium vector which generates certain voltage and can't be replaced by others.

In [37] [38] [39] [40], more switching devices are needed to replace the faulty device. If open-circuit fault occurs, the system can detect the faulty leg and make it isolated and replaced by other leg. But all these methods need more switching devices.

1.4 Research Objective and Thesis Layout

This thesis clarifies research on three-level neutral-point clamped (NPC) inverter because of its widely application and high cost-effective. Some methods are proposed to solve the problems of three-level NPC inverter, which includes unbalanced neutral point potential, fault diagnosis and fault tolerance control strategy. The chapters in this thesis are organized as follows:

Chapter 1: Research background and objective are introduced. It is necessary to do research on inverters because more and more renewable energy needs inverters to convert power. Some multilevel inverter topologies and control strategies are also introduced.

Chapter 2: The basic principle of NPC inverter is introduced, which can be the fundamental of following chapters.

Chapter 3: The characteristics of output currents are detailedly analyzed, when each fault occurs to the switch on phase A leg. Based on these characteristics, a method for detecting faulty leg and diagnosing to which switching device the fault occurs is proposed. And it is simulated for verification.

Chapter 4: A fault-tolerant control strategy is proposed and simulation is carried out to prove the proposed method.

Chapter 5: A Model Prediction Control strategy is proposed to reduce the difference of neutral-point potential. One more simulation proves that this method has better capability even though the NPC inverter is in worse case.

Chapter 2 Principle of Three-Level Inverter

2.1 Basic Principle

This chapter introduces the common control strategy, SVPWM which is widely used among multilevel inverters. The topology of three-level inverter is shown in Fig. 2-1.

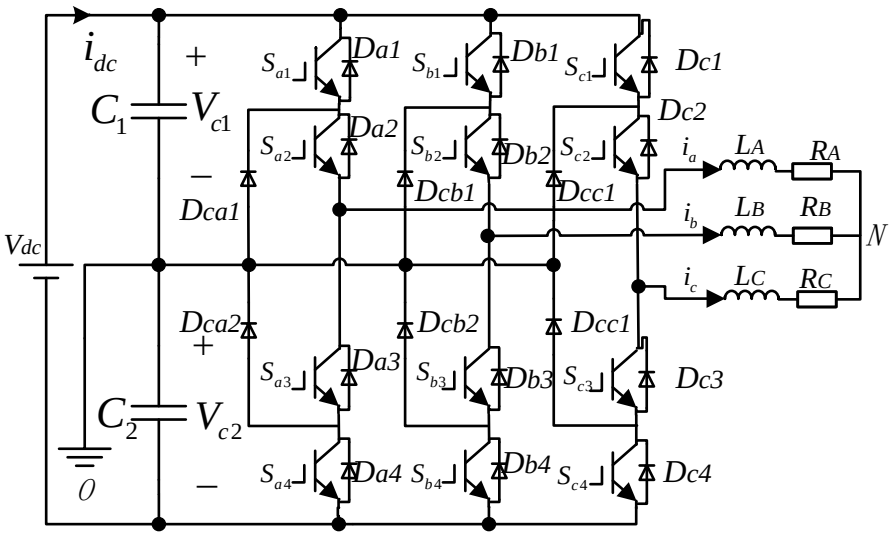


Fig. 2- 1 topology of three-level neutral-point clamped inverter

Table 2-1 shows the three working models of three-level NPC inverter.

Table 2- 1 Working models

Model	S_{k1}	S_{k2}	S_{k3}	S_{k4}	Output voltage	Switching state
1	1	1	0	0	$V_{dc}/2$	P
2	0	1	1	0	0	O
3	0	0	1	1	$-V_{dc}/2$	N

Where, k can replace a, b and c; S_{k1}, S_{k2}, S_{k3} and S_{k4} mean switching states of each switching tubes; 1 means turn-on, 0 means turn-off.

Each phase voltage can be expressed by S_a, S_b and S_c, shown as follows

$$\begin{cases} V_a = \frac{V_{dc}}{2} S_a \\ V_b = \frac{V_{dc}}{2} S_b \\ V_c = \frac{V_{dc}}{2} S_c \end{cases} \quad (2\text{-}1)$$

Where $S_k = \begin{cases} 1 \\ 0 \\ -1 \end{cases}$, k=a, b or c.

Voltage space vector can be defined as:

$$\mathrm{V} = \frac{2}{3}(V_a + wV_b + w^2 V_c) \quad (2\text{-}2)$$

Where $\mathrm{w} = e^{\frac{j2\pi}{3}} = -\frac{1}{2} + j\sqrt{\frac{3}{2}}$, which means that the phase is delayed by 180°.

Because S_a has three states, there are 27 states totally for S_a, S_b and S_c. The distribution of space vectors is shown in Fig. 2-2. Table2-2 only shows 6 switching states.

Table 2- 2 Switching states

S_a	S_b	S_c	V
-1	-1	-1	0
-1	-1	0	$\frac{1}{3}V_{dc}e^{-j120°}$
-1	-1	1	$\frac{2}{3}V_{dc}e^{-j120°}$
-1	0	-1	$\frac{1}{3}V_{dc}e^{-j120°}$
-1	0	0	$\frac{1}{3}V_{dc}e^{-j180°}$
-1	0	1	$\frac{\sqrt{3}}{3}V_{dc}e^{-j150°}$

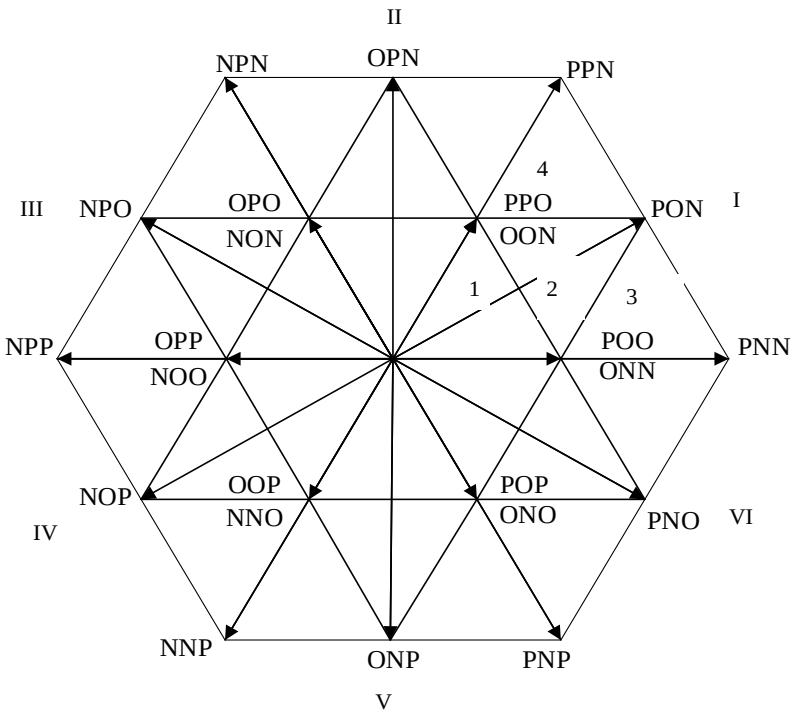


Fig. 2- 2 Distribution of space vectors

2.2 Switching Sequence

Switching order of the three-level NPC inverter often maintains two steps:

1) In order to avoid the straight-through (four switches connected in series are turned on or off at the same time), the switching state of the same bridge arm does not allow the P state to directly switch to the N state.

2) In order to reduce the switching frequency and switching losses of the NPC inverter, the three-phase bridge arm only allows the state of one phase bridge arm to be converted when the switching state is switched. For example, the state [PON] cannot be directly converted to the state [PPO], but can be switched to the state [POP].

Table 2-3 shows the switching sequence in sector 1.

Table 2- 3 Switching sequence of sector 1

Interval	Switching sequence
1	POO, OOO, OON, ONN, OON, OOO, POO
2	POO, PON, OON, ONN, OON, PON, POO
3	POO, PON, PNN, ONN, PNN, PON, POO
4	PPO, PPN, PON, OON, PON, PPN, PPO

2.3 Simulation

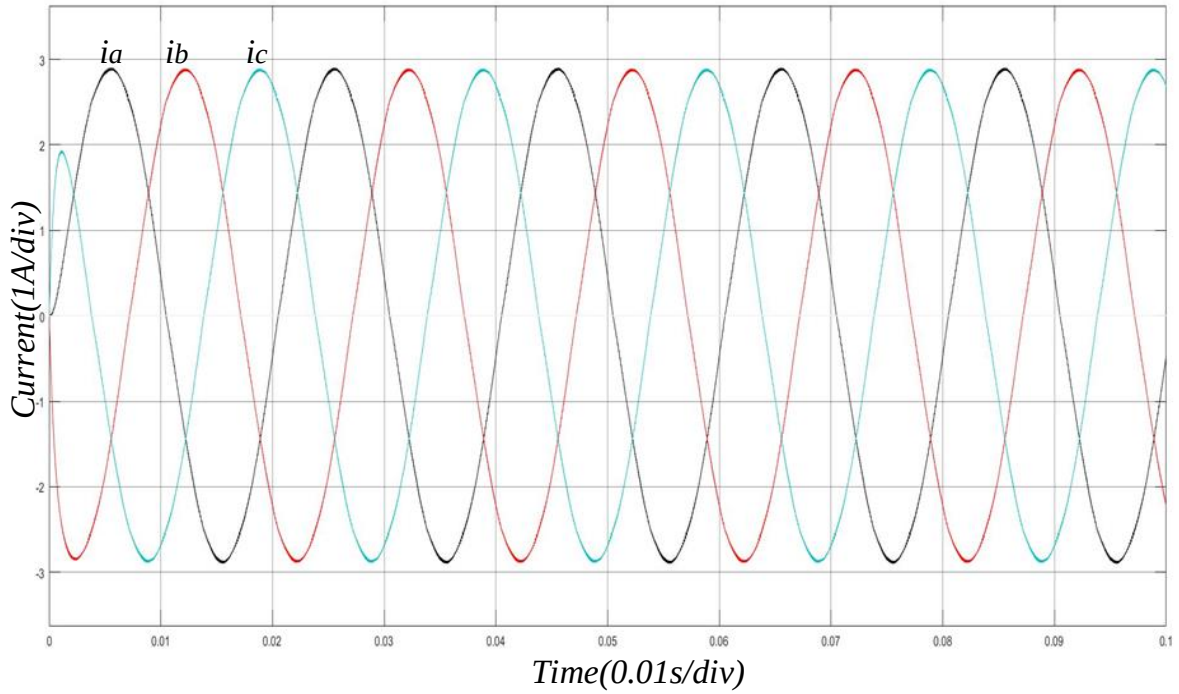
In order to verify the correctness and effectiveness of SVPWM, the simulation model of the NPC three-level inverter with a RL load is carried out on Matlab/Simulink. The simulation specifications are shown in Table 2-4.

Table 2- 4 Simulation specifications

V_{dc}	*80V*
Capacitor C_1, C_2	*2000μF*
Inductors L_A, L_B, L_C	*4mH*
Resistor R_A, R_B, R_C	*10Ω*
Sampling frequency	*10kHz*

Fig. 2-2(a) and (b) shows the simulation results of phase voltages and currents. There are three levels in the phase voltage waveforms and no distortion in currents waveforms.

Fig (c) shows the total harmonic distortion is 0.84%.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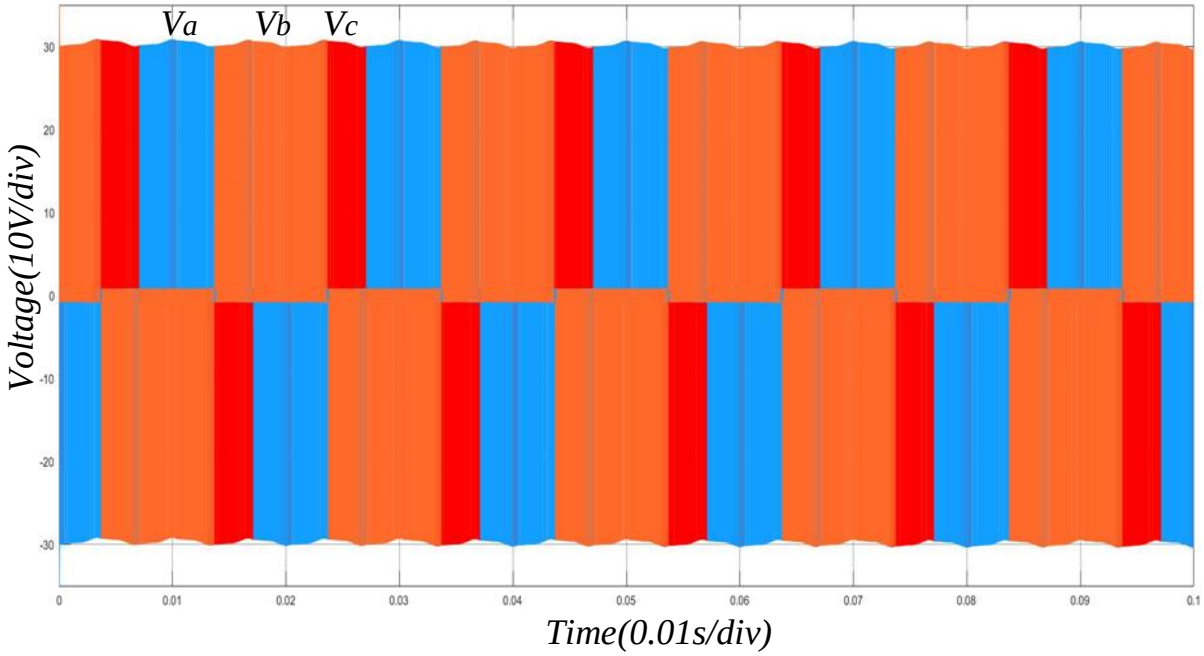
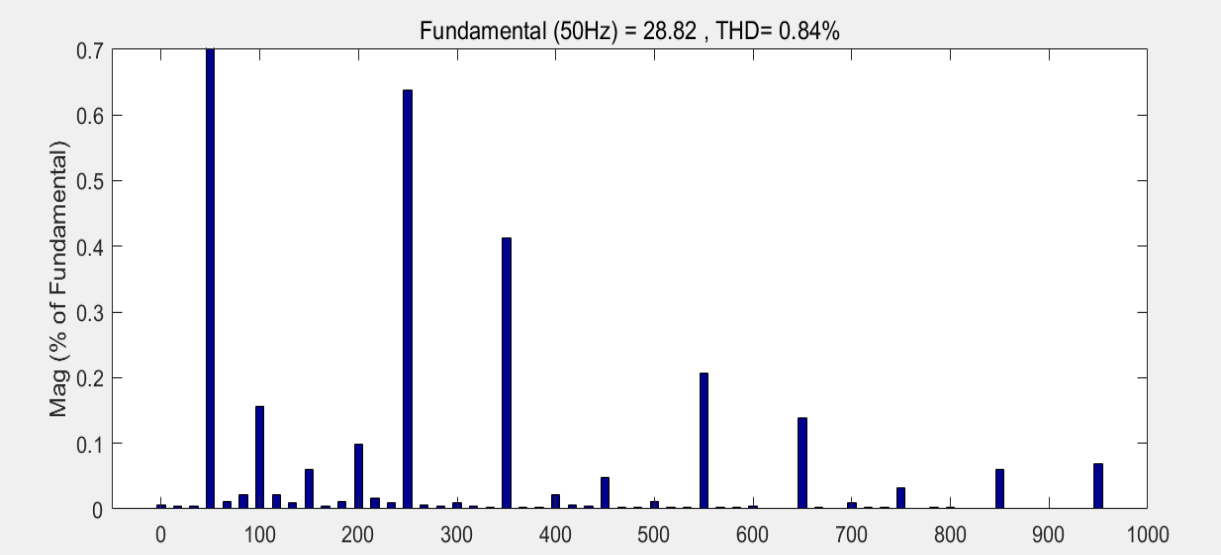
ic
Current(1A/div)
Time(0.01s/div)

(a)


Va
Vb
Vc
Voltage(10V/div)
Time(0.01s/div)

(b)



(c)

Fig. 2- 3 Simulation for three-level NPC inverter: (a) phase currents; (b) phase voltages; (c) total harmonic distortion

2.4 Conclusion

In this chapter, the basic principle of three-level NPC inverter is introduced. The following chapter will clarify some algorithms which are based on the principle.

Chapter 3 Fault Diagnosis

3.1 Introduction

When open-circuit faults occur to three-level NPC inverter, the output current waveform becomes distorted and the performance of inverter is considerably reduced. Thus, it needs to detect and identify these faults for further process. This chapter introduces a method to diagnose these faults.

3.2 Diagnosis Principle

In this section, the characteristics of two different kinds of open-circuit faults in phase A are analyzed. One is that fault occurs to one of the switching tubes (type 1) and another is that fault occurs to one of clamping diodes (type 2).

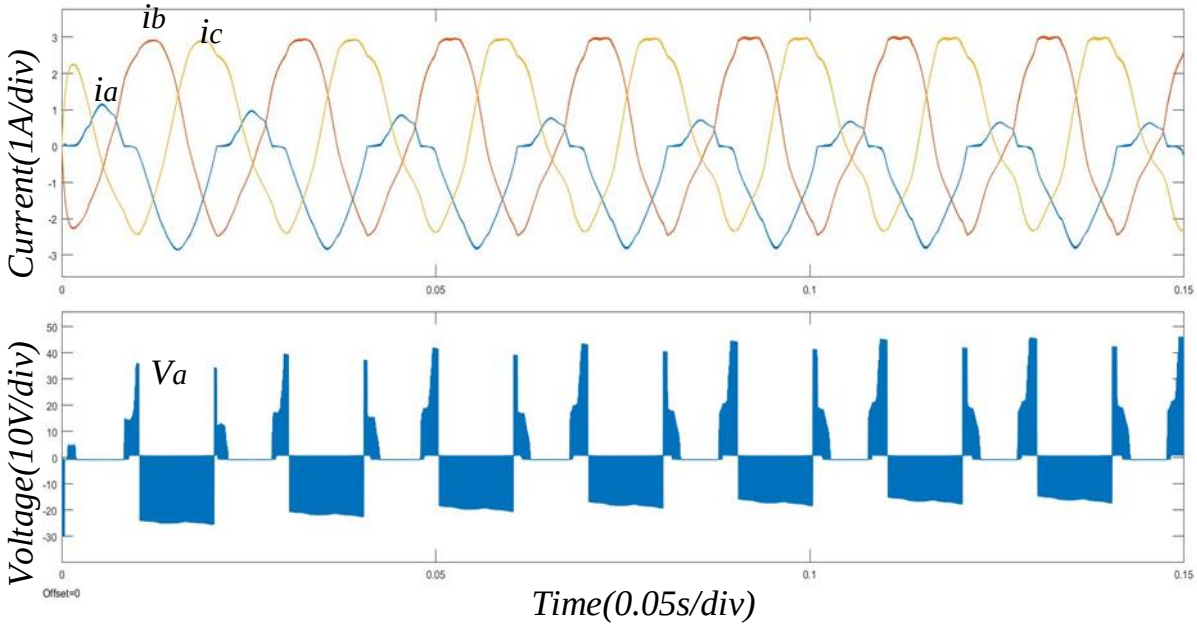
3.2.1 Type 1 Fault

1) Open-Circuit Fault in S_{a1}: To generate switching state [P], S_{a1} and S_{a2} should be turned on. And positive currents will pass through these switching devices. While, when S_{a1} fault occurs, another current path is formed, from D_{ca1} and $S_{a2.}$ As the output current decreases to 0, these switches are reversed-biased, shown in Fig. 3-1(a). When the current decreases to 0, When S_{al} fault occurs, the switching state [P] can't work as normal.

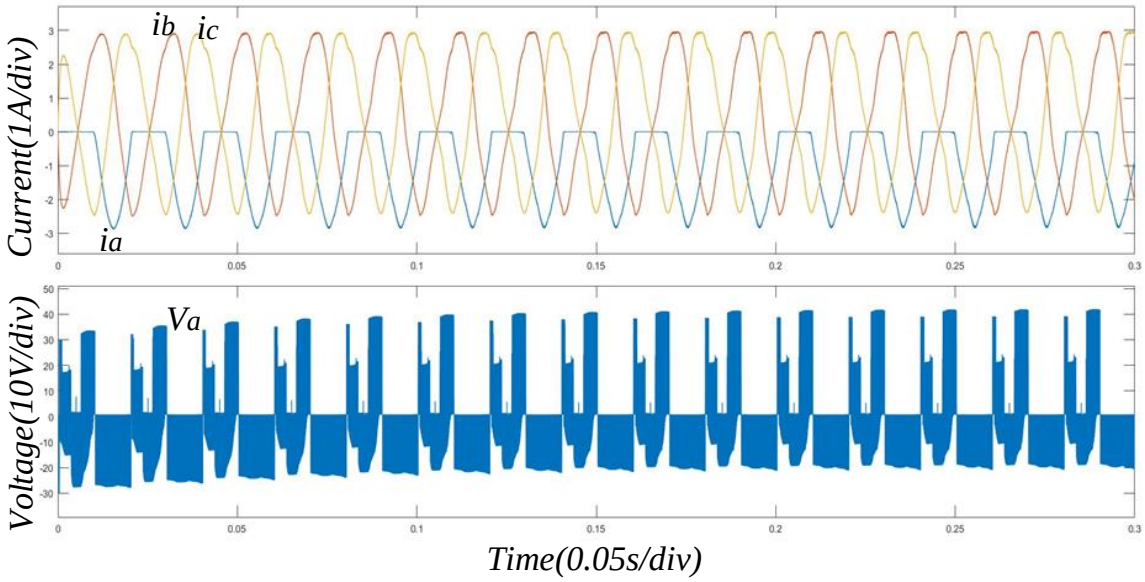
2) Open-Circuit Fault in S_{a2}: To generate switching state [O], S_{a2} and D_{ca2} should be turned on. And positive currents will pass through these switching devices. In case of switching state [P], S_{a1} and S_{a2} should be turned on. And positive currents will pass through these switching devices. While, when S_{a2} fault occurs, another current path is formed, from D_{a3} and D_{a4}. As the output current decreases to 0, these switches are reversed-biased due to the positive voltage, shown in Fig. 3-1(b).

3) Open-Circuit Fault in S_{a3}: To generate switching state [O], S_{a3} and D_{ca2} will be turned on. And the current path is formed. To generate switching state [N], S_{a3} and S_{a4} will be turned on. And the current path is formed. While, when S_{a3} fault occurs, another current path is formed, from D_{a1} to D_{a2}. As the output current decreases to zero, the two switches are reverse-biased, shown in Fig. 3-1(c).

4) Open-Circuit Fault in S_{a4}: To generate switching state [N], S_{a3} and S_{a4} should be turned on. And the current path is formed. While, when S_{a4} fault occurs, another current path is formed, from D_{ca2} to S_{a3}. As the output current decreases to zero, D_{ca2} is reverse-biased, shown in Fig. 3-1(d).



(a)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Current(1A/div)
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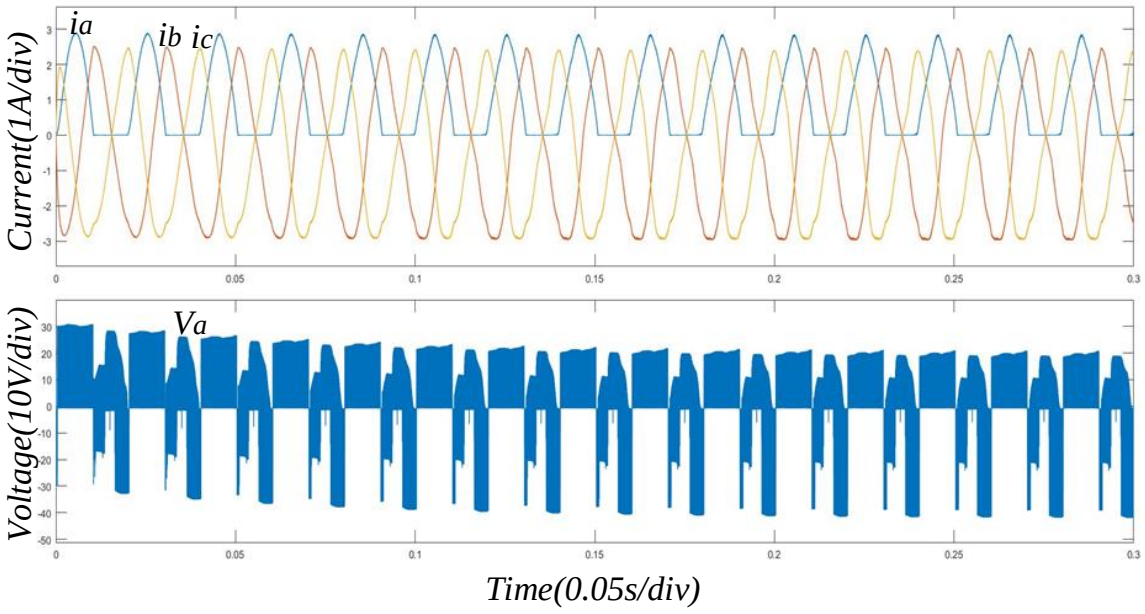
(b)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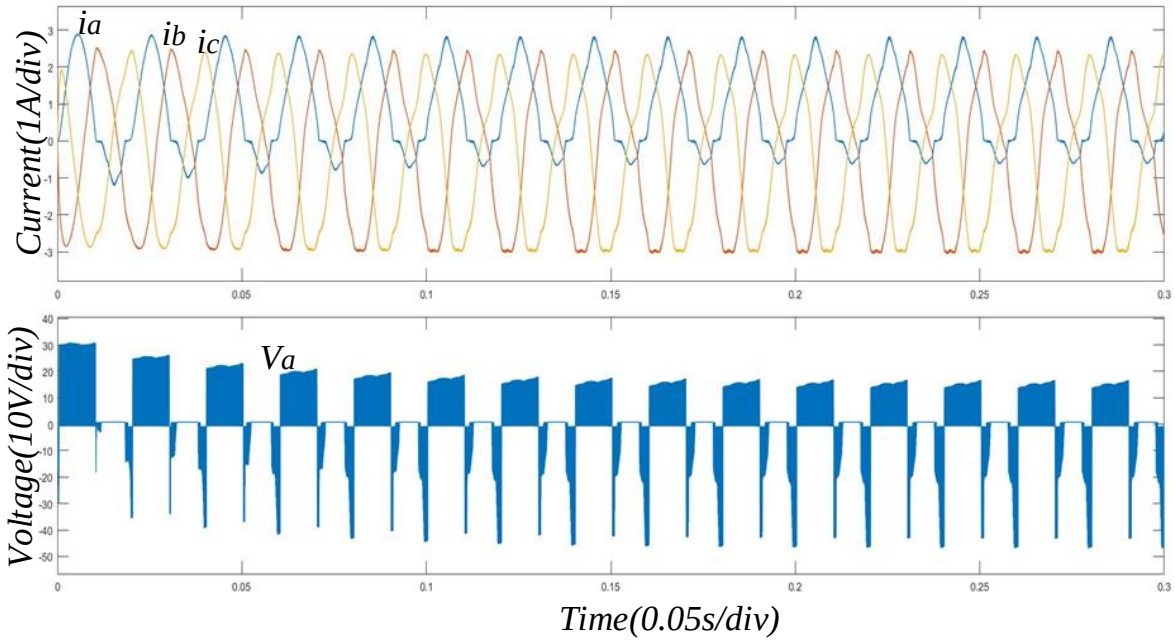
Current(1A/div)
Va
Voltage(10V/div)
Time(0.05s/div)

(c)



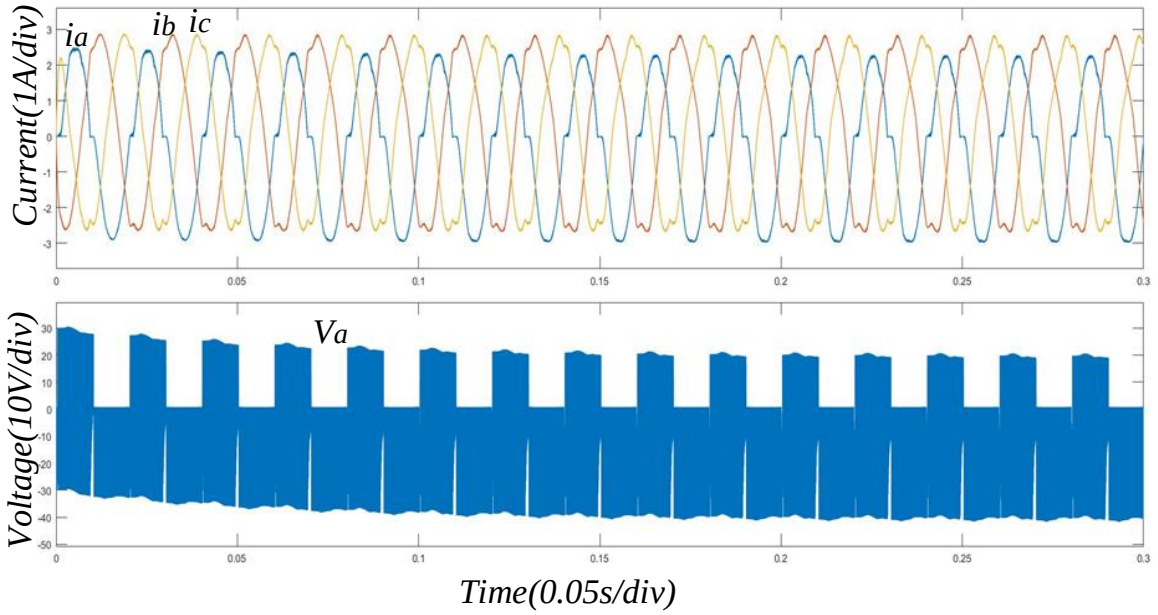
(d)

Fig. 3- 1 Output phase currents and voltage for faults (a) S_{a1} fault; (b) S_{a2} fault; (c) S_{a3} fault; (4) S_{a4} fault

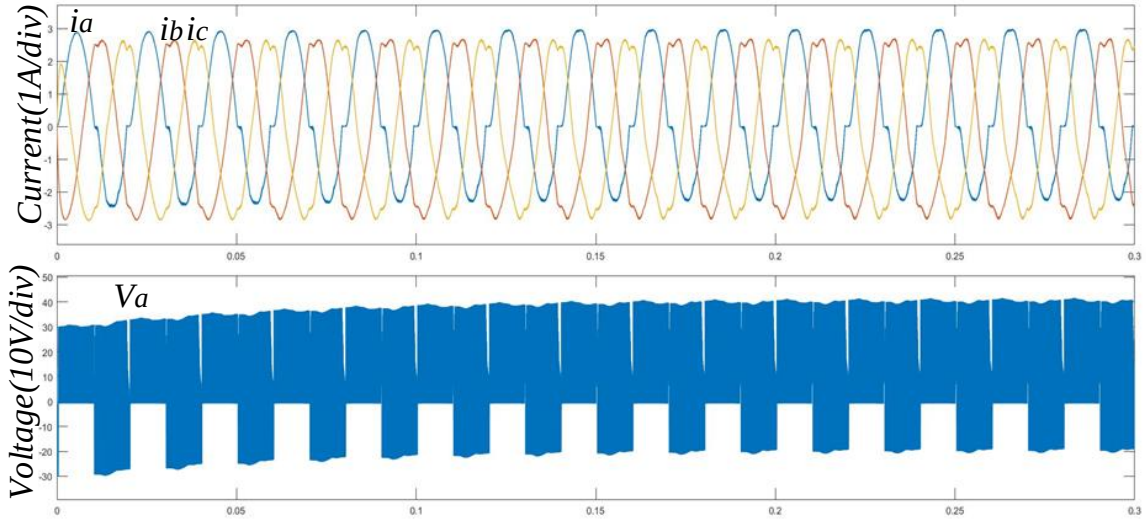
3.2.2 Type 2 Fault

1) Open-Circuit Fault in D_{ca1}: When the inverter is in normal case, to generate the switching state [O], the current path is formed, from D_{ca1} to S_{a2}. When the fault occurs, another current is formed, from D_{a3} to D_{a4}. The overall analysis is almost the same with type-A fault. The output currents and voltage waveforms are shown in Fig. 3-2(a).

2) Open-Circuit Fault in D_{ca2}: When the inverter is in normal case, to generate the switching state [O], the current path is formed, from D_{ca2} to S_{a3}. When the fault occurs, another path is formed, from D_{a1} to D_{a2}. The output currents and voltage waveforms are shown in Fig. 3-2(b).



(a)



(b)

Fig. 3- 2 Output phase currents and voltage for faults: (a) D_{ca1} fault; (b) D_{ca2} fault

3.3 Open-circuit Fault Detection Method

3.3.1 Identification of Faulty Leg

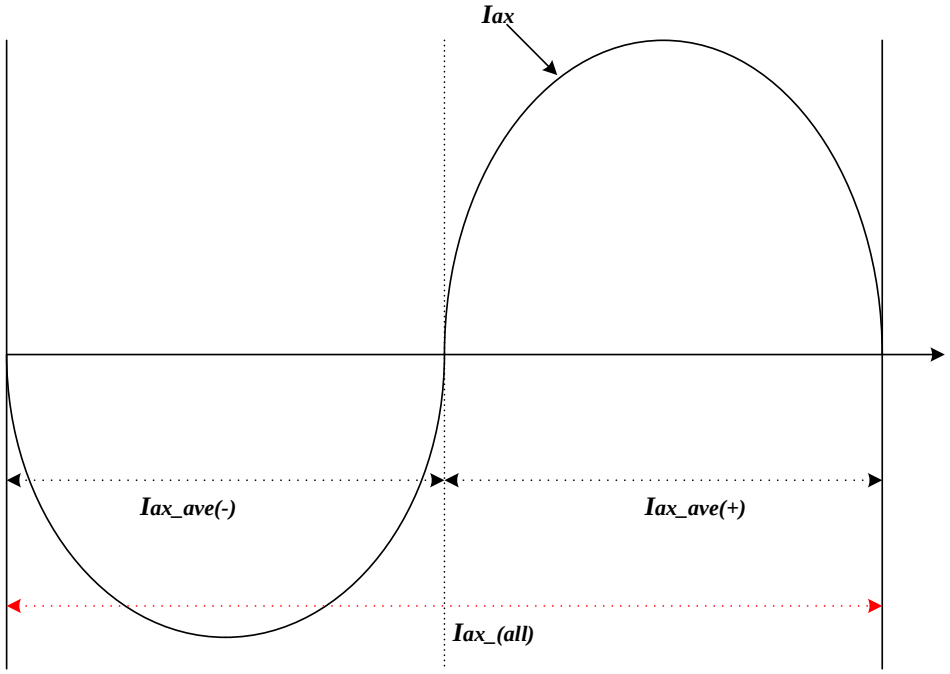


Fig. 3- 3 Definition of variables for the fault detection

The average value of positive current of each phase is defined by *Ix_ave(+)*. Similarly, the average value of negative current is defined by *Ix_ave(-)*. Thus, each phase has two current values. In this thesis, the two variables are used to judge the faulty leg.

Phase A is taken as an example. In normal case, because no faults occur and the current waveforms are not distorted, *Iax_ave(+)=Iax_ave(-)* or *Iax_ave(+)-Iax_ave(-)=0*. When fault occurs to S_{a1}, *Iax_ave(all)=Iax_ave(+)+Iax_ave(-)* has a negative value, shown in Fig. 3-1(a). And $I_{ax_{ave}}(all) = -(I_{bx_{ave}}(all) + I_{cx_{ave}}(all)) < 0$. Thus, it can be used to judge the faulty leg by calculating average values of these currents. When open-circuit fault occurs in other phases, it can be judged by the similar way.

3.3.2 Classification of the Fault Type

Phase A is taken as an example. A method to identify faulty switch is proposed according to

the characteristics of currents in the thesis.

As the magnitude of currents change when the load changes. It is necessary to normalize the current for classification. The phase currents can be normalized as follows:

$$Imax=max\{Ia[1], Ia[2], \ldots Ia[n], Ib[1],\ldots Ib[n],\ldots Ic[1], Ic[2],\ldots Ic[n]\} \quad (3\text{-}1)$$

Where, *Ia[n]* is the sampling current of phase A in the *Nth* sampling cycle, *Ib[n]* is the sampling current of phase B in *Nth* sampling cycle, *Ic[n]* is the sampling current of phase C in *Nth* sampling cycle; *Imax* is the maximum sample value.

Once *Imax* is identified, $Ia'[1]=Ia[1]/Imax$, $Ia'[2]=Ia[2]/Imax$,….

In normal case, no faults occur, $Ia'[1]+\ldots+Ia'[n]=0$, $Ib'[1]+\ldots+Ib'[n]=0$, $Ic'[1]+\ldots+Ic'[n]=0$. But, when faults occurs in phase A, $Ia'[1]+\ldots+Ia'[n]\neq 0$ because of the distorted waveforms. Especially, when fault occurs to S_{a1}, $Ia'[1]+Ia'[2]+\ldots+Ia'[k]<\left|Ia'[k+1]+\ldots+Ia'[n]\right|$.

Where, $1\ldots k$, mean sample value of upper part of current; $k+1,\ldots,n$, mean sample value of lower part of current.

$$Iax\_ave(+)=(Ia'[1]+\ldots Ia'[k])/k \quad (3\text{-}2)$$

$$Iax\_ave(-)=(Ia'[k+1]+\ldots+Ia'[n])/k \quad (3\text{-}3)$$

As is shown in Fig. 3-1 and 3-2, when the fault occurs to S_{a1}, S_{a2} or D_{ca1}, the magnitude of *Iax_ave(+)* is smaller than that of *Iax_ave(-)*. When the fault occurs to S_{a3}, S_{a4} or D_{ca2}, the magnitude of *Iax_ave(-)* is smaller. Therefore, comparing the magnitude of *Iax_ave(+)* and *Iax_ave(-)* can identify if the fault is in the upper part(S_{a1}, S_{a2} or D_{ca1}) or lower part(S_{a3}, S_{a4} or

D_{ca2}).

Because the fault occurring in upper part has similar characteristics with that in lower part. Faults in upper part are mainly analyzed. According to the characteristic of distortion,

$$Iax\_ave3(+)>Iax\_ave1(+)>Iax\_ave2(+) \tag{3-4}$$

Where $Iax\_ave1(+)$, $Iax\_ave2(+)$ and $Iax\_ave3(+)$ represent average value of upper distorted current for S_{a1} fault, S_{a2} fault and D_{ca1} fault respectively.

To judge these three faults, two thresholds are applied as follows:

$$Iax\_ave3(+)>I_{threshold1}>Iax\_ave1(+)>I_{threshold2}>Iax\_ave2(+) \tag{3-5}$$

If the fault is in lower part, it can be identified by similar way. To better illustrate the algorithm, the flow chart is shown in Fig. 3-4.

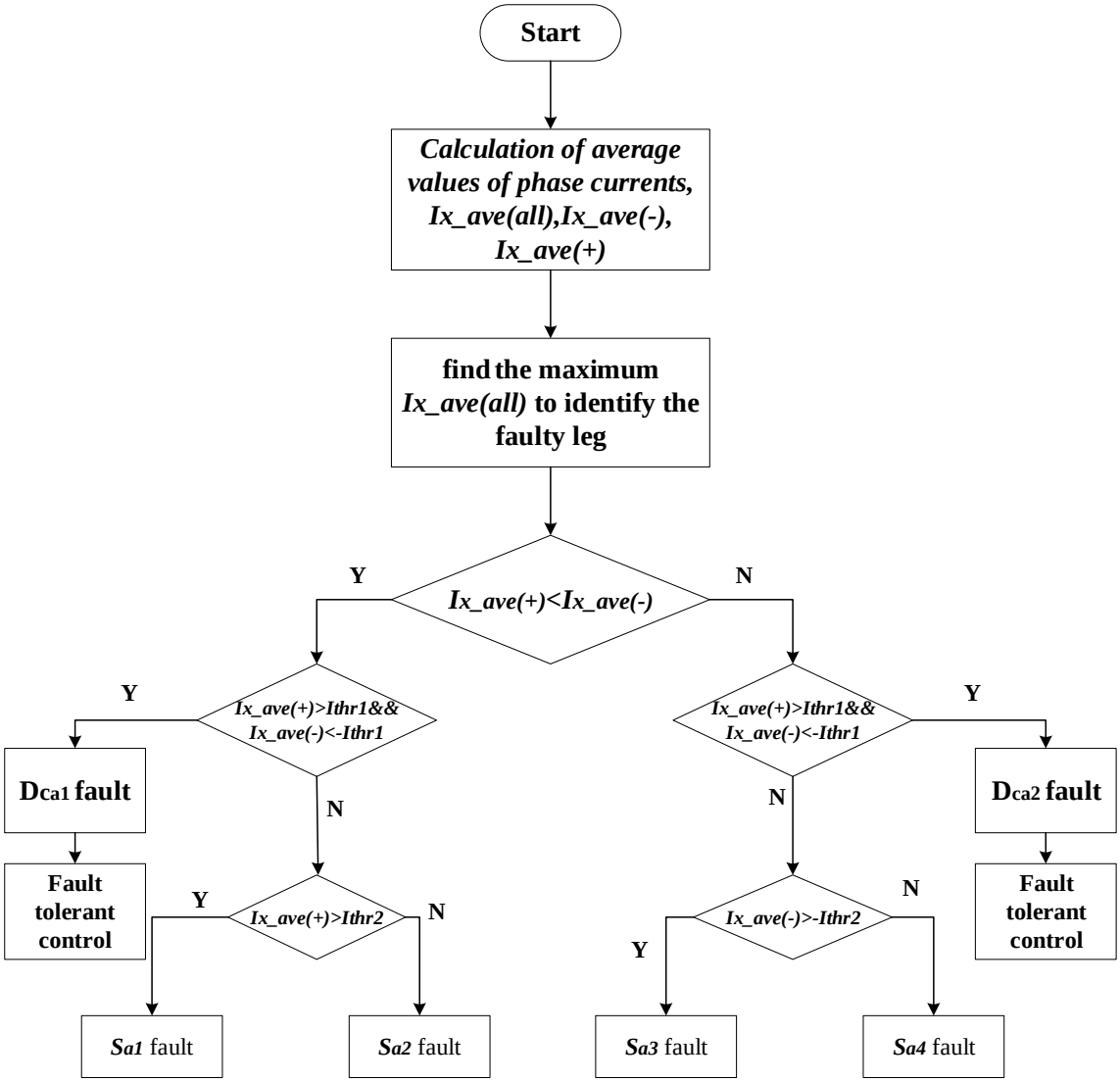


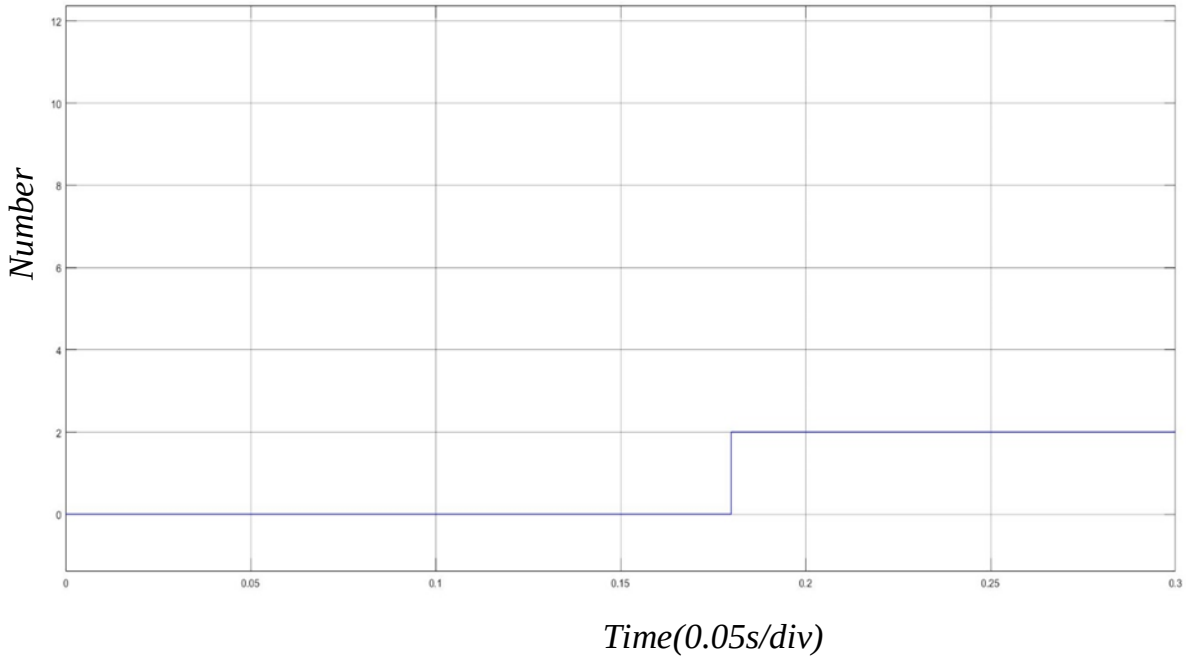
Fig. 3- 4 Flow chart of proposed fault detection

3.4 Simulation

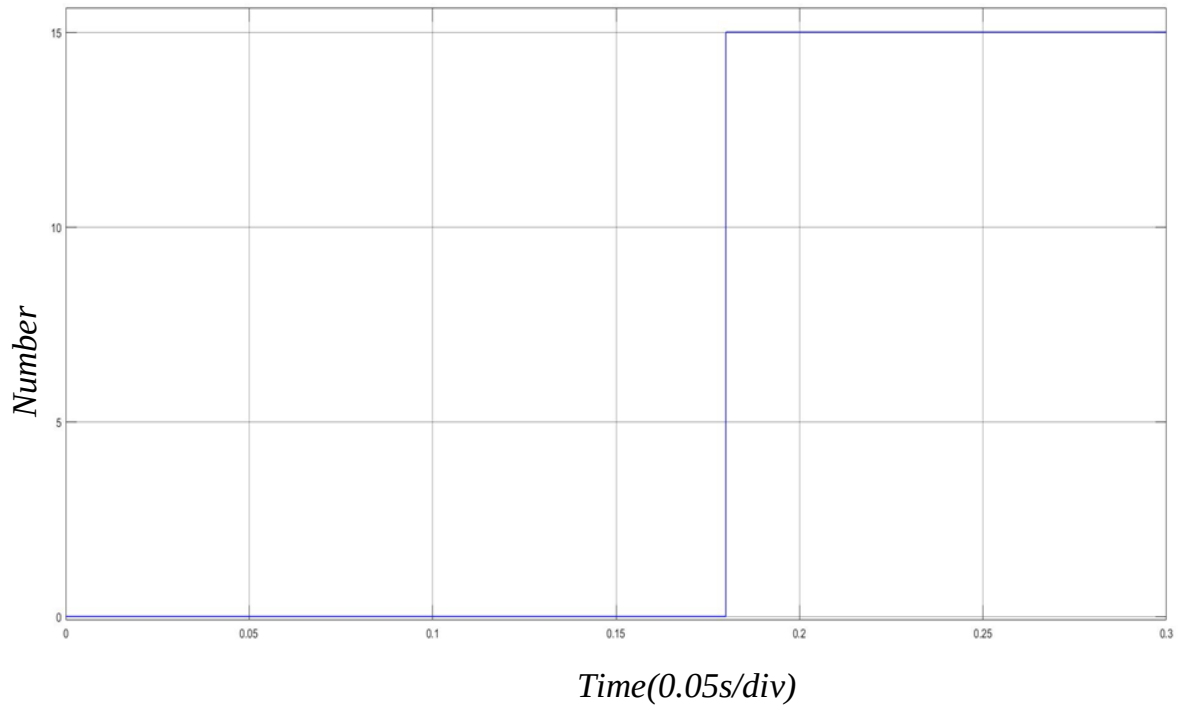
Since there are four switching tubes and two clamping diodes on each phase leg, it has 18 faults totally. This thesis uses numbers from 1 to 18 to represent these faults and #0 to represent normal case as shown in table 3-1.

Table 3- 1 Fault numbers

Fault #	Switch #	Fault #	Switch #
1	S_{a1}	10	D_{cb2}
2	S_{a2}	11	S_{b3}
3	D_{ca1}	12	S_{b4}
4	D_{ca2}	13	S_{c1}
5	S_{a3}	14	S_{c2}
6	S_{a4}	15	D_{cc1}
7	S_{b1}	16	D_{cc2}
8	S_{b2}	17	S_{c3}
9	D_{cb1}	18	S_{a4}



(a)



(b)

Fig. 3- 5 Simulation for fault diagno: (a) Sa2 fault; (b) Dcc1fault

Fig 3-5(a) shows simulation when the fault occurs to S_{a2} and its value is 2. Fig. 3-5(b) shows simulation when the fault occurs to D_{cc1}. The two simulations can show that the algorithm proposed in this thesis is capable of detecting the open-circuit faults and identifying to which switching device the open-circuit fault occurs.

3.5 Conclusion

A fault diagnosis algorithm is proposed in this chapter. And simulation can verify the effectiveness of this method. Even if this method can accurately identify the faulty switching device, it may need more methods to handle this open-circuit fault and output normal currents.

Chapter 4 Fault-Tolerant Control Strategy

4.1 Introduction

In engineering cases, even though the faulty switches can be identified, it still needs some time to handle these cases. Thus, it is necessary for fault tolerant control strategy to work before faulty switches are replaced.

4.2 Analysis of Open-Circuit Fault

1）Open-circuit fault S_{a1}: If the open-circuit fault occurs to switch S_{a1}, space vectors containing switching state [P] can't be generated, such as: [PPO], [PON] and so on. But other switching states [O] and [N] in leg A can be generated normally.

2) Open-circuit fault S_{a2}: If the open-circuit fault occurs to switch S_{a2}, space vectors containing switching state [P] and [O] can't be generated, such as: [PPO], [OPN] and so on.While other switching state [N] in leg A can work normally.

3) Open-circuit fault D_{ca1}: If the open-circuit fault occurs to switch D_{ca1}, space vectors containing switching state [O] can't be generated, such as: [ONN], [OPN] and so on. While other switching state [P] and [N] in leg A can be generated normally.

when the fault occurs to other switching devices, the impossible space vectors can be analyzed by the same way.

4.3 Control Strategy

4.3.1 Fault Occurs to switching tubes

If the open-circuit fault occurs to switching tubes (S_{a1}, S_{a2}, S_{a3} or S_{a4}), the output phase currents are distorted and neutral-point potential is unbalanced as mentioned in Chapter 3. This is because the switching states [P] or [N] is impossibly generated. Thus, it is necessary to reduce modulation ratio to generate currents without distortion.

S_{a1} for example, the switching state [P] cannot be generated. But some voltage vectors containing [P] can be replaced by others, which is that [PPO] can be replaced by [OON]. To replace the switching state [P] with [N], the modulation ratio must be small enough from 0 to 0.5 shown in the shaded area in Fig. 4-1.

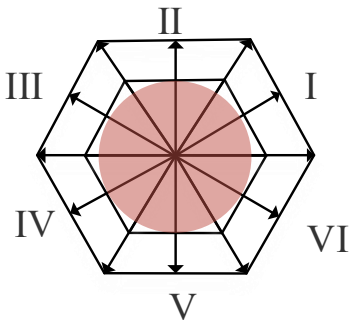


Fig. 4- 1 Simplified distribution of space vectors

Fig. 4-2(a) shows switching sequence when the reference vector is in sector II of shaded area. Since S_{a1} fault occurs and the switching state [P] can't work, it should be replaced by the switching state [N] which has the same magnitude as the switching state [P]. It can be easily achieved by adding or subtracting a certain time to the action time of other voltage space vectors， which is shown in Fig. 4-2(b). After T_a, T_b *and* T_c are changed, [PPO] is replaced by [OON] because they have the same line-to-line output voltage.

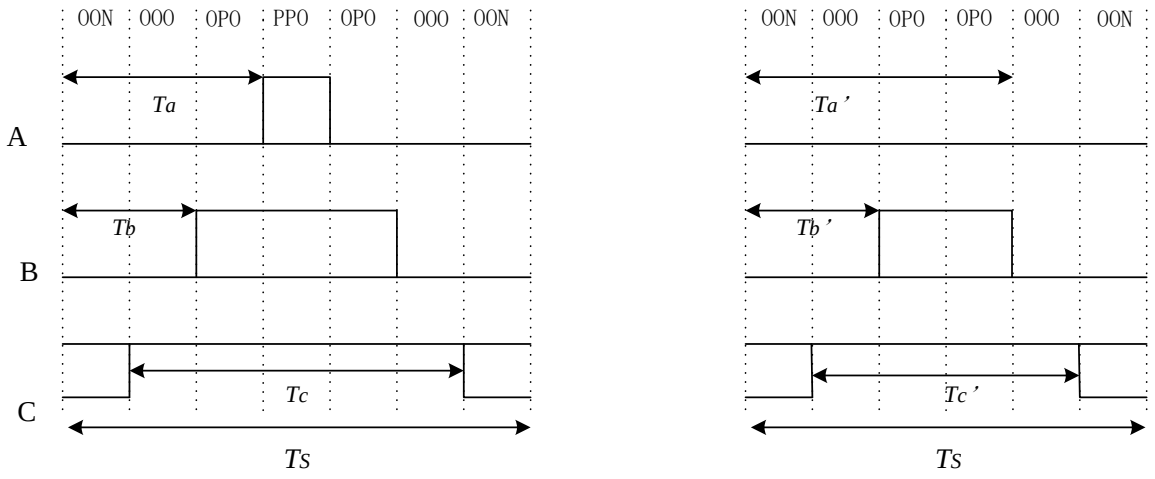


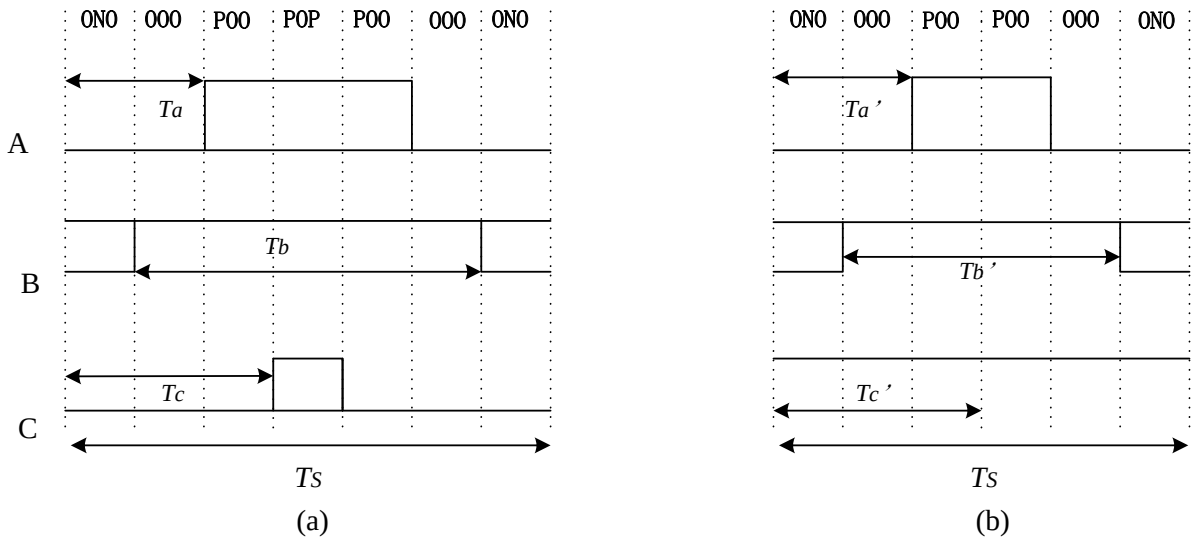
Fig. 4- 2 Switching sequence for fault-tolerant control in Sector II: (a) before rearrangement; (b) after rearrangement.

$$T_{low}=T_s/2-T_a \tag{4-1}$$

$$T_a'=T_{low}+T_a \tag{4-2}$$

$$T_b'=T_b+T_{low} \tag{4-3}$$

$$T_c'=T_c-T_{low} \tag{4-4}$$



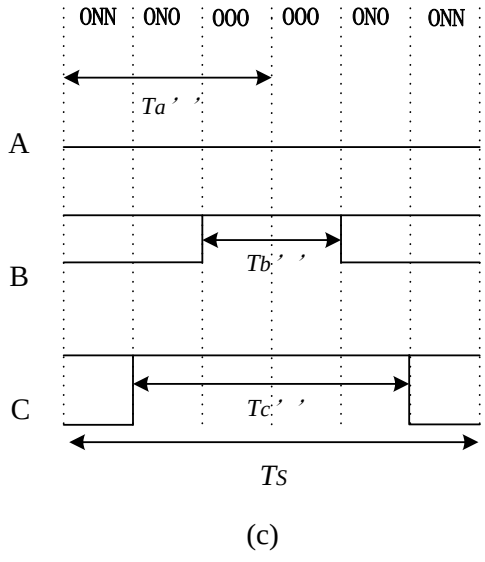


Fig. 4- 3 Switching sequence for proposed method in sector VI: (a) under normal condition; (b) after rearrangement; (c) final rearrangement.

When the reference voltage vector is in sector VI of shaded area, [PPO] should be replaced by [OON] because of S_{a1} fault, after T_{low} is taken to the action time of these voltage vectors as shown in Fig. 4-3(b). Besides, [POO] also needs to be replaced by [ONN]. The final rearranged switching sequence is shown in Fig. 4-3(c).

$$T_{low}=T_s/2-T_c \quad (4\text{-}5)$$

$$T_a'=T_a+T_{low} \quad (4\text{-}6)$$

$$T_b'=T_b-2T_{low} \quad (4\text{-}7)$$

$$T_c'=T_c+T_{low} \quad (4\text{-}8)$$

$$T_{low}'=T_s/2-T_a' \quad (4\text{-}9)$$

$$T_a''=T_a'+T_{low} \quad (4\text{-}10)$$

$$T_b''=T_b'-2T_{low} \quad (4\text{-}11)$$

$$T_c''=Tc'+T_{low} \quad (4\text{-}12)$$

The switching state [P] is replaced by [N], which can cause unbalanced neutral-point potential. To avoid unbalanced neutral-point potential, the switching state [N] should be replaced by [P] when the refence vector is in the opposite sector. In case of S_{a1} fault, the switching state [P] in the sectors 1, 2 and 6, is replaced by [N]. Therefore, the switching state [N] in the opposite sector 3, 4 and 5 should be replaced by [P].

The final rearranged switching sequence is [OPP]-[OOP]-[OOO]-[OOP]-[OPP] in the sectors 4.

4.3.2 Fault Occurs to Clamping Diodes

If the open-circuit fault occurs to clamping diodes (D_{ca1}, D_{ca2}), the switching state [O] can't be generated.

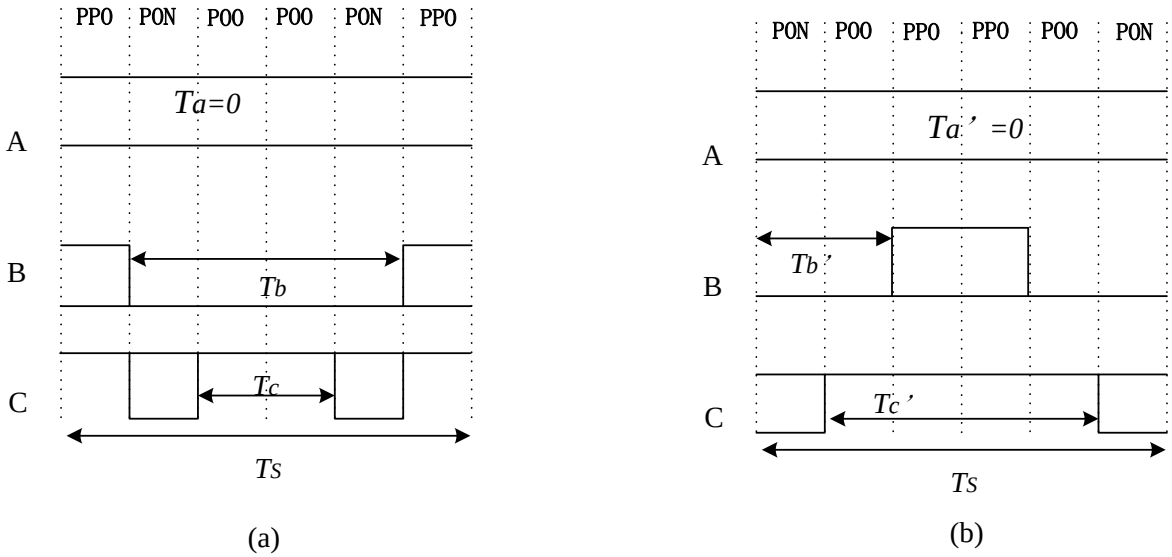


Fig. 4- 4 Switching sequence for proposed method in sector I (shaded area): (a)rearrangement; (b) final rearrangement.

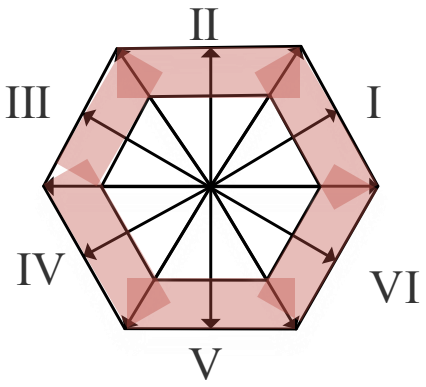


Fig. 4- 5 Simplified distribution of space vectors

1）High modulation ratio：If the reference voltage vector is in the shaded area shown in Fig. 4-5, it is impossible to generate the switching state [O] because of D_{ca1} fault. For example, the switching sequence should be rearranged as shown in Fig. 4-4(b), after [OON] and [ONN] are replaced by [PPO] and [POO] respectively as shown in Fig. 4-4(a).

$$T_a'=0 \tag{4-13}$$

$$T_b'= T_b/2 \tag{4-14}$$

$$T_c'=T_S-T_b+T_c \tag{4-15}$$

b) Low modulation ratio: D_{ca1} fault for example, it is impossible to generate voltage vectors

containing the switching state [O]. To avoid distortion of output voltage and current, when [OOO] is replaced by [PPP]. In the opposite area, [OOO] should be replaced by [NNN].

Fig. 4-6(a) shows the switching sequence under normal case. When D_{ca1} fault occurs, [OOO], [ONN]and [OON] should be replaced by [PPP], [POO] and [PPO] separately. The rearranged switching sequence is shown in Fig. 4-6(b). The turn-on times are redefined as follows

$$T_a''=T_S/2 \tag{4-16}$$

$$T_b'= (T_S -T_b)/2 \tag{4-17}$$

$$T_c''=(T_S -T_c)/2 \tag{4-18}$$

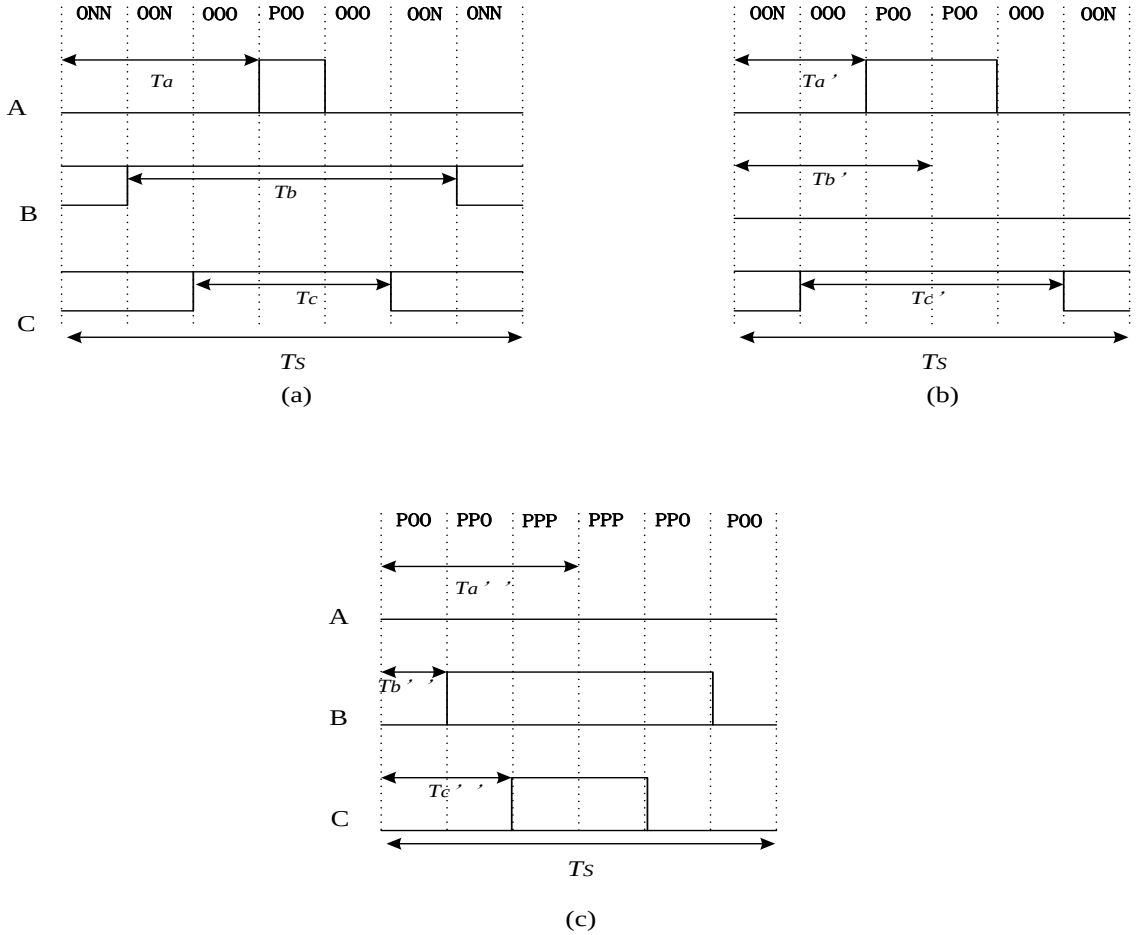


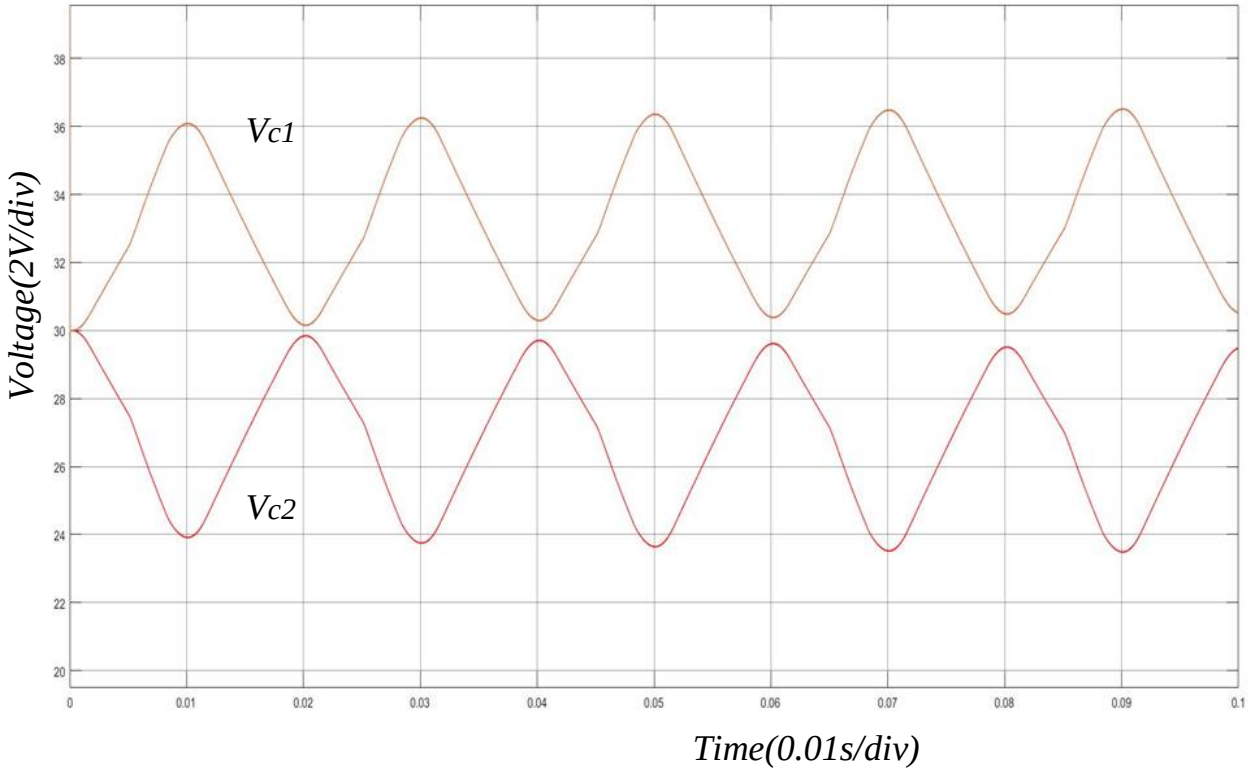
Fig. 4- 6 Switching sequence for proposed method (low modulation ratio) in sector I: (a) under normal condition; (b) after rearrangement; (c) final rearrangement.

4.4 Simulation

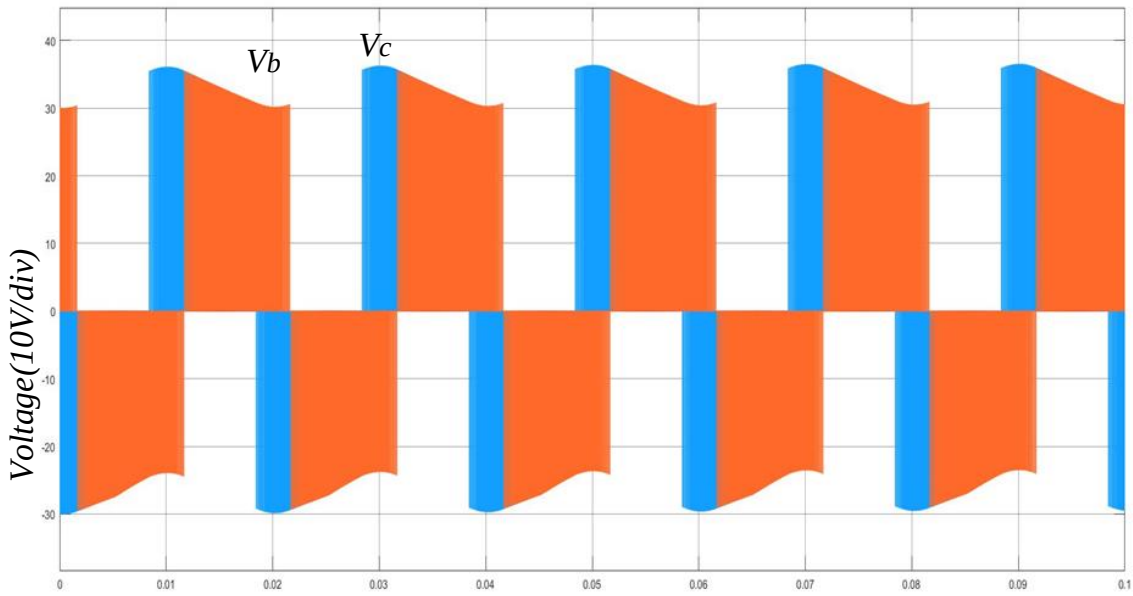
Simulation has been carried out to verify the effectiveness of the proposed fault tolerance control strategy. The specifications used for the simulation are shown in Table 4-1:

Table 4- 1 Simulation specifications

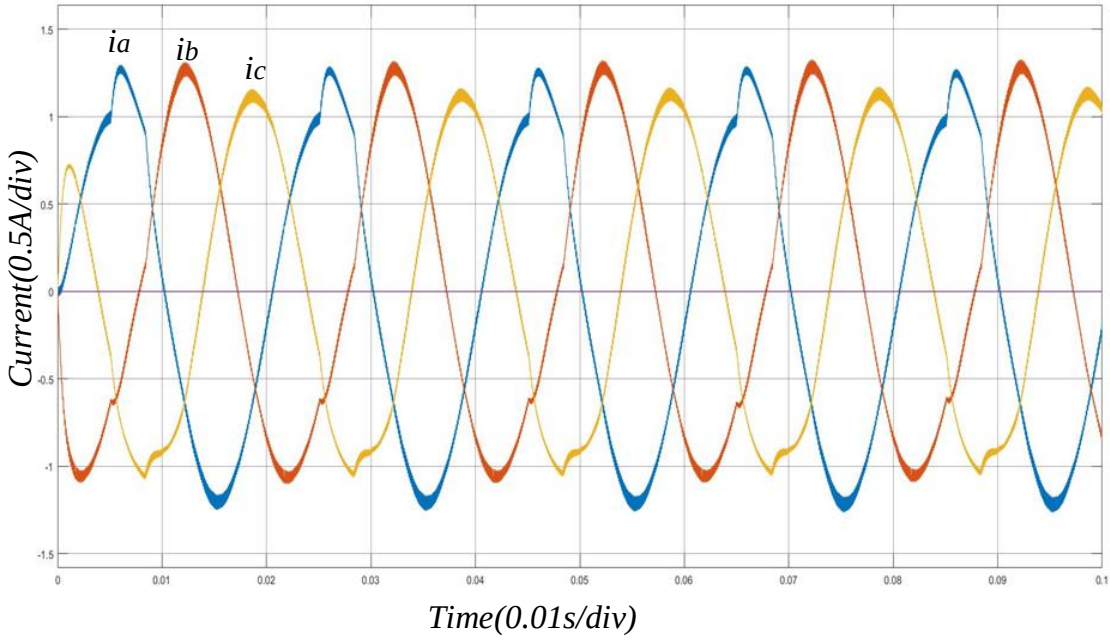
V_{dc}	*60V*
Capacitor C_1, C_2	*470μF*
Inductors L_A, L_B, L_C	*6mH*
Resistor R_A, R_B, R_C	*10Ω*
Sampling frequency	*10kHz*



(a)

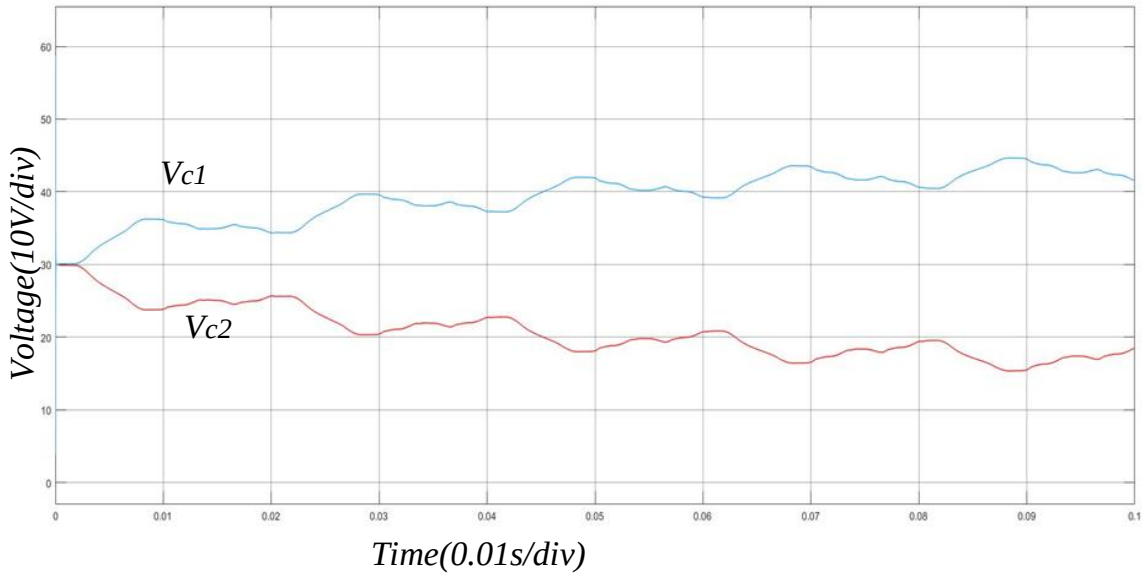


(b)

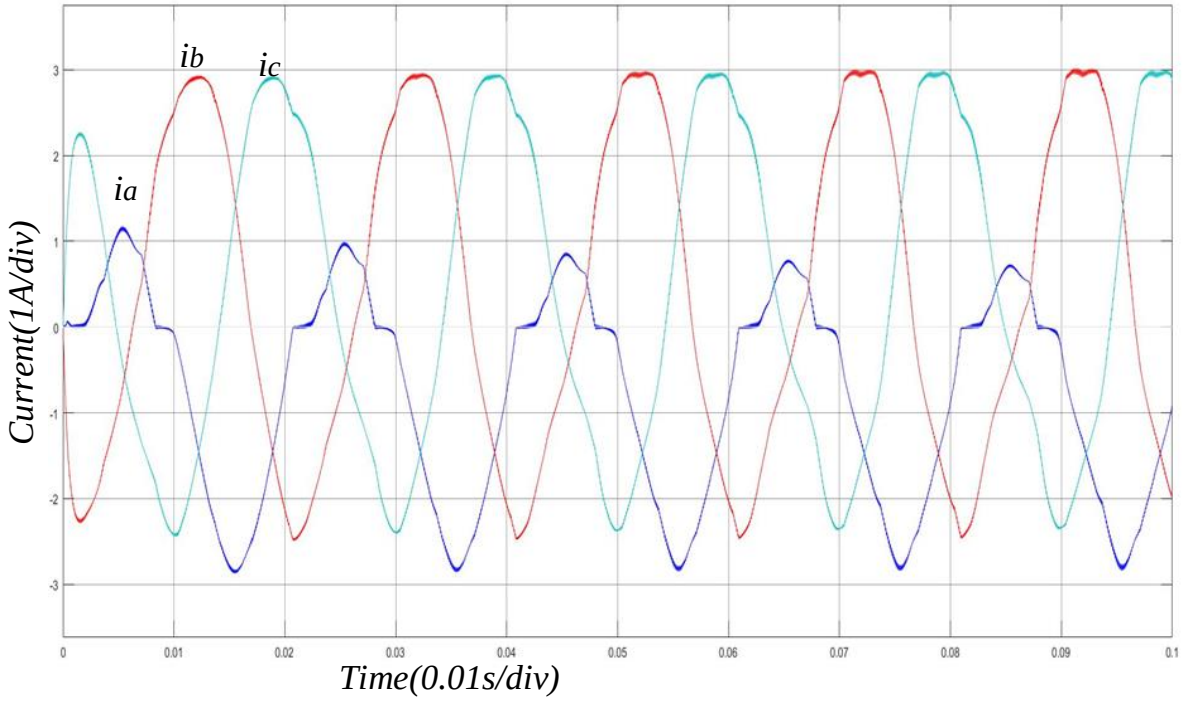


(c)

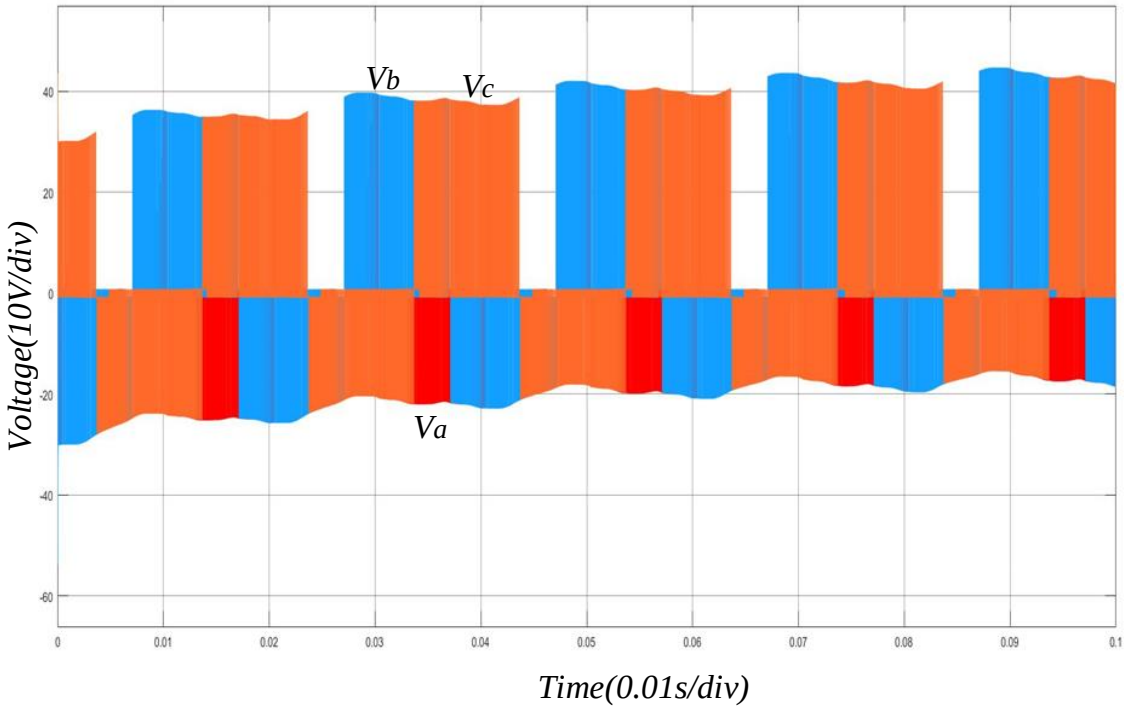
Fig. 4- 7 Simulation for proposed fault tolerant control: (a) neutral-point potential; (b) phase voltages; (c) phase currents.


Vc1
Vc2
Voltage(10V/div)
Time(0.01s/div)

(a)


ia
ib
ic
Current(1A/div)
Time(0.01s/div)

(b)



(c)

Fig. 4- 8 Simulation for no fault tolerant control strategy: (a) neutral-point potential; (b) phase currents; (c) phase voltages

It can be seen from the Fig. 4-7(c) and 4-8(b) that the output currents of tolerance control strategy have better performance and less distortion, compared with that of no control strategy. From Fig. 4-8(a), it can be seen that the differences between two capacitor voltages become larger even though they keep balanced state at the beginning. The neutral-point potential in Fig. 4-7(a) has better performance and its fluctuation keeps between *24V* and *36 V*. And it also can be seen that the output phase voltages are smoother compared with that of no fault tolerance strategy shown in Fig. 4-7(b) and 4-8(c). It is caused by the large difference of the neutral-point potential. In other words, if the neutral-point potential keeps balanced state, the output phase voltages are smooth and output currents are less distorted.

It can be concluded that with the fault tolerance control strategy, the three-level NPC inverter has better performance when open-circuit fault occurs.

4.5 Conclusion

This chapter introduces the principle of the proposed fault tolerance control strategy and simulation is used to verify the effectiveness of this strategy. However, the simulation also shows that though this strategy can improve the performance when the open-circuit fault occurs, the differences between the two capacitor voltages still exists. In other words, this strategy just reduces the effect of the open-circuit fault. Thus, it is necessary to propose more effective method to greatly reduce the difference of two capacitor voltages and further improve the performance of the inverter.

Chapter 5 Model Prediction Control Strategy

5.1 Introduction

Though the difference of the two DC capacitor voltages in chapter 4 is very small, it still affects the output currents and phase voltages. Thus, this chapter introduce Model Prediction Control (MPC) strategy to solve this problem.

5.2 Principle

The topology of three-level inverter is shown in Fig. 2-1. To better express the unbalanced voltage between the two capacitors, two variables are defined as:

$$\begin{cases} S_{kh} = \frac{S_k(S_k+1)}{2} \\ S_{kl} = \frac{S_k(1-S_k)}{2} \end{cases} \tag{5-1}$$

Where, $S_k = \begin{cases} 1 \\ 0 \\ -1 \end{cases}$, k=a, b, or c.

According to Kirchhoff's current law,

$$\begin{cases} C_1 \frac{dV_{c1}}{dt} = i_{dc} - (S_{ah} i_a + S_{bh} i_b + S_{ch} i_c) \\ C_2 \frac{dV_{c2}}{dt} = i_{dc} - (S_{al} i_a + S_{bl} i_b + S_{cl} i_c) \end{cases} \tag{5-2}$$

Where, $C_1 = C_2 = C$; i_{dc}, i_a, i_b, i_c are shown in Fig. 2-1.

In discrete system, *dx/dt* can be expressed by:

$$\frac{dx}{dt} \approx \frac{x(k+1)-x(k)}{T_s} \tag{5-3}$$

Where *x(k+1)* is the *k+1*th sampling value, *x(k)* is *k*th sampling value.

Then, equation 5-2 can be expressed by:

$$\begin{cases} V_{c1}(k+1) - V_{c1}(k) = \frac{T_s}{C}(i_{dc} - j_h) \\ V_{c2}(k+1) - V_{c2}(k) = \frac{T_s}{C}(i_{dc} - j_l) \end{cases} \tag{5-3}$$

$$\begin{cases} j_h = S_{ah} i_a + S_{bh} i_b + S_{ch} i_c \\ j_h = S_{ah} i_a + S_{bh} i_b + S_{ch} i_c \end{cases} \tag{5-4}$$

Equation 5-3 can be simplified by

$$\Delta \mathrm{V}(\mathrm{k}+1) = \Delta \mathrm{V}(\mathrm{k}) - \frac{T_S}{C}(j_h - j_l) \tag{5-5}$$

Where $\Delta \mathrm{V} = V_{C1} - V_{C2}$.

When faults occur, only three space vectors work in one cycle. Thus, the difference of capacitor voltages can be expressed by:

$$\Delta \mathrm{V}(\mathrm{k}+1) = \Delta \mathrm{V}(\mathrm{k}) - \sum_{i=1}^{3} \frac{t_i}{C}(j_{h\_i} - j_{l\_i}) \tag{5-6}$$

Where j_{h_i} and j_{l_i} are the *i*th switching states of j_h and j_l separately.

In this thesis, a cost function is proposed to track the reference voltage and keep neutral-point potential balanced. The cost function is expressed by:

$$\mathrm{g} = \lambda_1 \left\{ \left[V_{\alpha_{ref}}(k+1)T_S - (V_{1_\alpha} t_1 + V_{2_\alpha} t_2 + V_{3_\alpha} t_3) \right]^2 + \left[V_{\beta_{ref}}(k+1)T_S - (V_{1_\beta} t_1 + V_{2_\beta} t_2 + V_{3_\beta} t_3) \right]^2 \right\} + \lambda_2 \left(\Delta V(k+1) \right)^2 \tag{5-7}$$

Where, $V_{\alpha_{ref}}$ and $V_{\beta_{ref}}$ are the horizontal axis components and the vertical axis components of V_α and V_β separately in the two-phase stationary coordinate system; $\lambda_1$and λ_2 are the weigh factor; $V_{1\alpha}$, $V_{1\beta}$, $V_{2\alpha}$, $V_{2\beta}$, $V_{3\alpha}$ and $V_{3\beta}$ are the horizontal axis components and the vertical axis components of V_1, $V_2$and V_3 separately which are selected according to nearest three vector principle. For example, when Sa1 fault occurs, and modulation is small, and the reference vector is in sector 1, V_1, $V_2$and V_3 are [OON], [OOO] and [ONN] respectively, based on the analysis of chapter 4,

5.3 Optimization of Cost Function

To solve the action times of space vectors, Lagrange equation is applied.

Because the cost function is related to t_1, t_2 and t_3, equation 5-7 can be simplified by

$$\begin{cases} \min g(t_1, t_2, t_3) \\ s.t.\ 2t_1 + 2t_2 + t_3 = T_S \end{cases} \tag{5-8}$$

Equation 5-8 can be further simplified by

$$\mathrm{L}(t_1, t_2, t_3, t_3) = g(t_1, t_2, t_3) + \lambda(2t_1 + 2t_2 + t_3 - T_S) \tag{5-9}$$

Where, λ is weigh factor, $0 < \lambda < 1$.

To solve t_1, t_2 and t_3, derivation can be applied to equation 5-9 and expressed by

$$\begin{cases} \frac{dL}{dt_1} = 0 \\ \frac{dL}{dt_2} = 0 \\ \frac{dL}{dt_3} = 0 \end{cases} \tag{5-10}$$

Besides, t_1, t_2, t_3 and t_4 all should meet the requirement that

$$\begin{cases} 0 \le t_1 \le T_S \\ 0 \le t_2 \le T_S \\ 0 \le t_3 \le T_S \end{cases} \tag{5-11}$$

Cases where $t_1 < 0$ may happen according to equation 5-10. Thus, it is necessary to optimize these action times. If $t_1 < 0$ occurs, action times can be optimized by

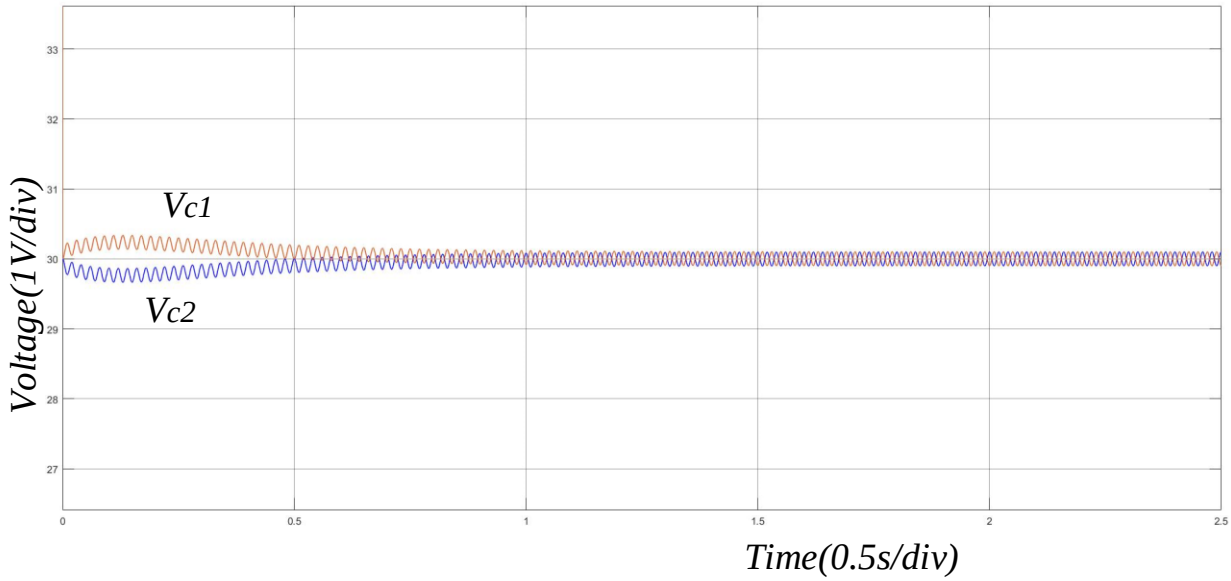
$$\begin{cases} t_1^* = 0 \\ t_2^* = \frac{t_2}{t_2+t_3+t_1} \\ t_3^* = \frac{t_3}{t_2+t_3+t_1} \end{cases} \tag{5-12}$$

5.4 Simulation

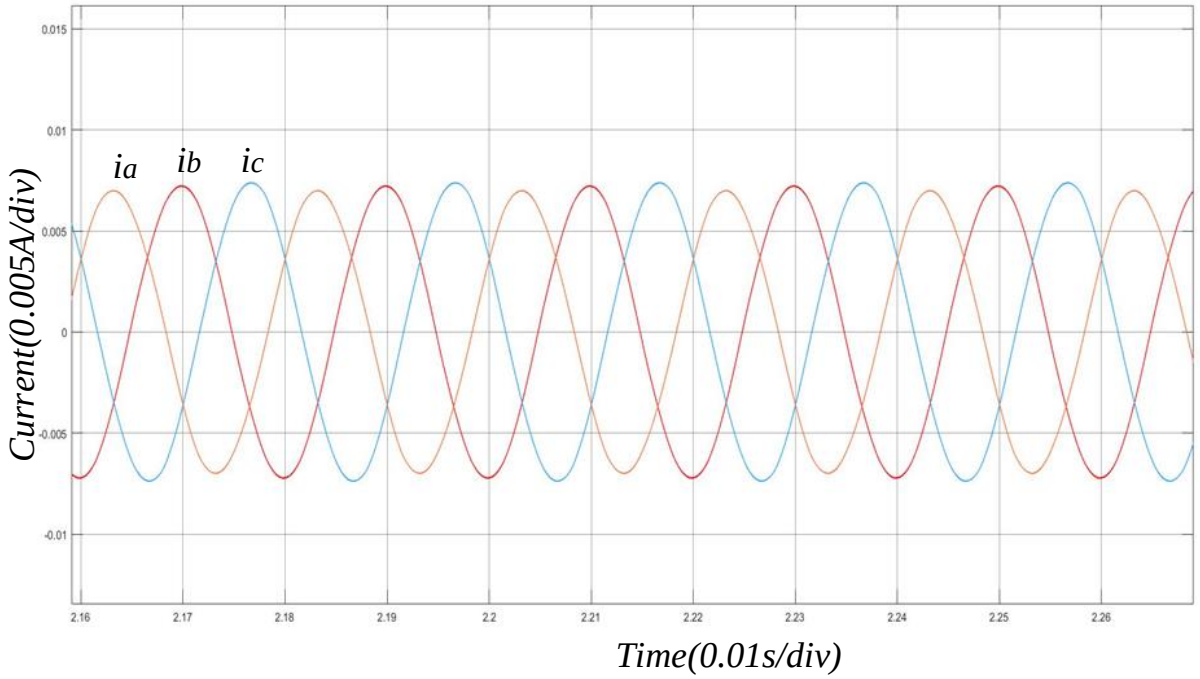
To verify the effectiveness of the proposed method, simulation on Matlab/Simulink is carried out. The specifications and parameters used for simulation are shown in table 5-1.

Table 5- 1 Simulation specifications

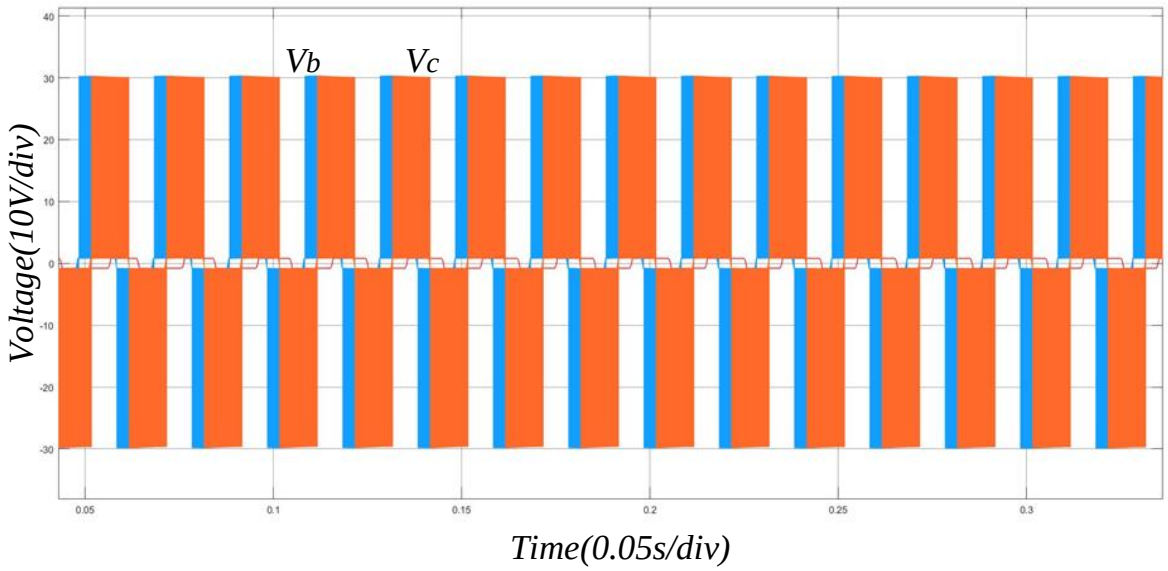
V_{dc}	*80V*
Capacitor C_1, C_2	*470μF*
Inductors L_A, L_B, L_C	*4mH*
Resistor R_A, R_B, R_C	*12Ω*
Sampling frequency	*10kHz*


Vc1
Vc2
Voltage(1V/div)
Time(0.5s/div)

(a)


ia
ib
ic
Current(0.005A/div)
Time(0.01s/div)

(b)



(c)

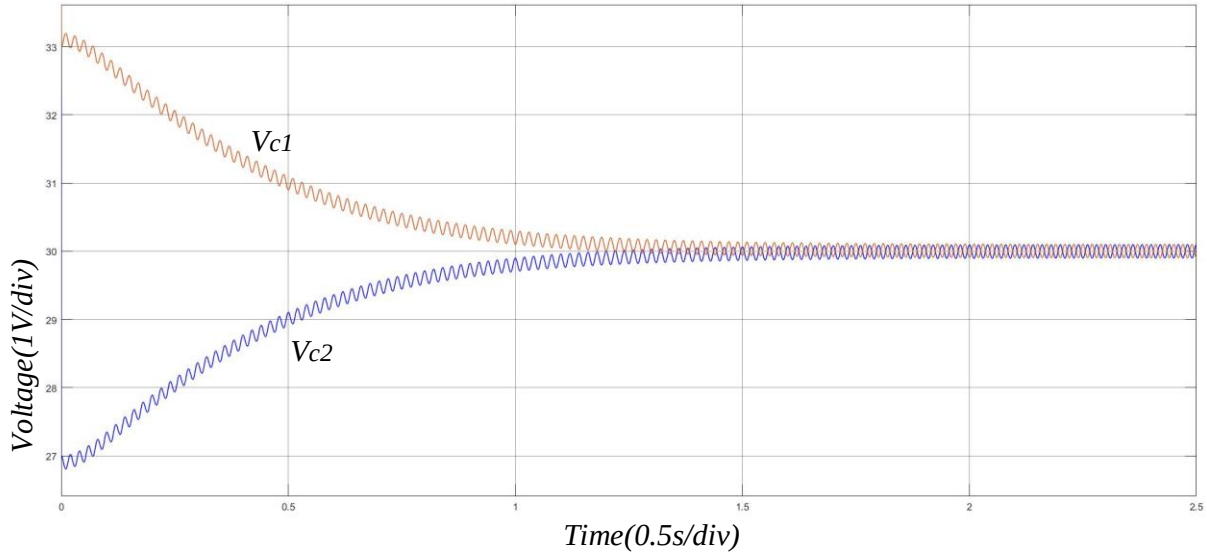
Fig. 5- 1 Simulation for MPC strategy with balanced neutral-point potential and Sa1 fault: (a) neutral-point potential; (b) phase currents; (c) phase voltages

It can be seen that the neutral-point potential has smaller fluctuation between *30.1V* and *29.9V*, when Sa1 fault occurs. Compared with the result shown in Fig. 4-5 in chapter 4, the proposed MPC strategy has better performance. The current waveforms in Fig. 5-1(b) show no distortion, and phase voltages in Fig. 5-1(c) is smooth and has three levels, *0V*, *30V* and *-30V*.

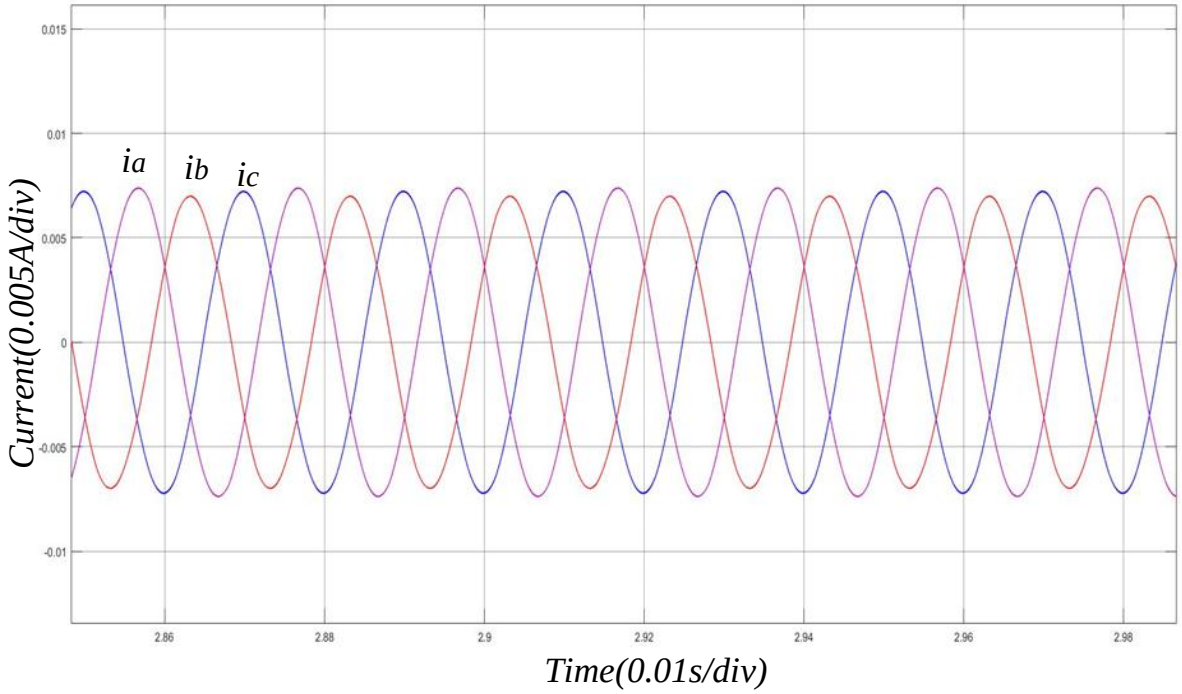
In actual engineering environment, the unbalanced load or the different parameters of the switching devices can cause the unbalanced state of the neutral-point potential. When these cases occur, they will also considerably reduce the performance of the inverter. To further verify the effectiveness of the proposed method, another simulation that both unbalanced neutral-point potential and Sa1 fault occur is carried out. Table 5-2 shows the specifications and parameters.

Table 5- 2 Simulation specifications

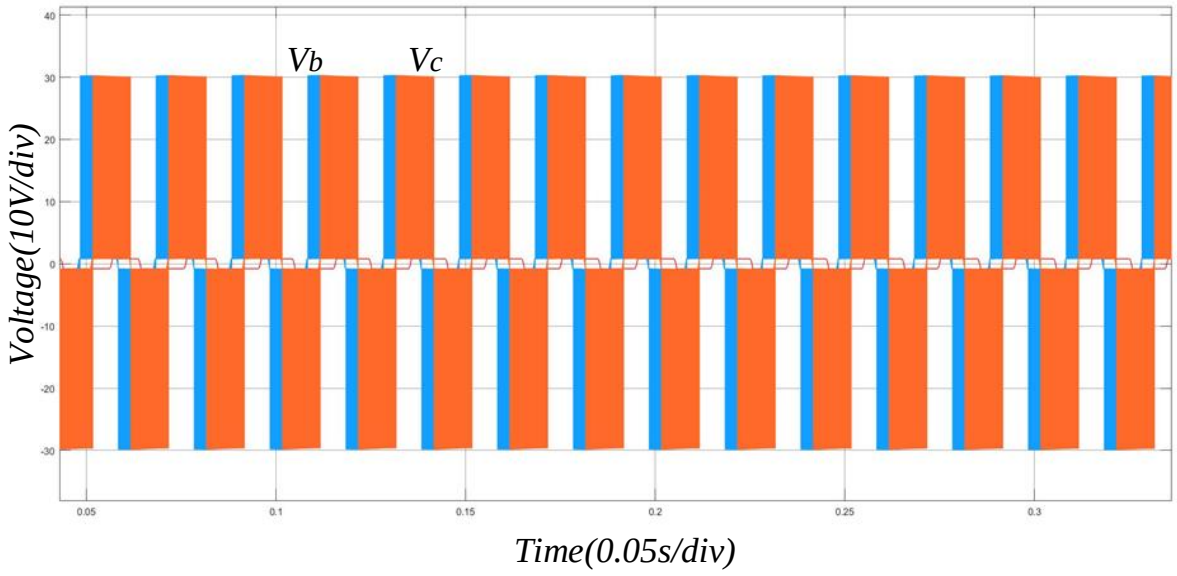
V_{dc}	*80V*
V_{c1}	*33V*
V_{c2}	*27V*
Capacitor C_1, C_2	*470μF*
Inductors L_A, L_B, L_C	*4mH*
Resistor R_A, R_B, R_C	*10Ω*
Sampling frequency	*10kHz*



(a)



(b)



(c)

Fig. 5- 2 Simulation for MPC strategy with unbalanced neutral-point potential and Sa1 fault: (a) neutral-point potential; (b) phase currents; (c) phase voltages

It can be seen in Fig. 5-2(a) that the difference of the neutral-point potential is *6V* at the

beginning. When the proposed method is added to the system, it takes about *1.2s* to make the neutral-point potential balanced and fluctuate between *30.1V* and *29.9V*. The current waveforms and phase voltages also show no distortion even though both S_{a1} fault and unbalanced neutral-point potential occur at the same time.

5.5 Conclusion

This chapter introduces the basic principle of MPC strategy. Simulation for S_{a1} fault and unbalanced neutral-point potential are carried out to verify that the proposed method can improve the performance of NPC three-level inverter even though inverter is in worse case. And the simulation also proves that the proposed method can reduce the fluctuation of neutral-point potential.

Chapter 6 Conclusion

This thesis is mainly to introduce the control strategy for NPC three-level inverter to improve its performance. The main work of this thesis can be concluded as follows:

Firstly, the common principle for NPC three-level inverter is introduced and simulation for the inverter is carried out to show its performance under normal situation. However, in actual engineering environment, there are more cases, like open-circuit fault and unbalanced neutral-point potential.

Secondly, this thesis proposes one method to detect whether faults occurs and identify to which switching device faults occur. The first step of the proposed method is to detect the faulty leg based on the characteristic that when one fault occurs, the magnitude of the average value for the upper part of the output currents is unequal to that of the lower part. According to this, the faulty leg can be identified. Then, fault occurring to different switching devices will cause distortion of the output currents and the average value of the distortion is smaller compared with other parts of the currents. According to this fact, the faulty switching device can be identified. The simulation verifies that the proposed method can diagnose faults. However, it is far from enough because in actual engineering environment, before faulty device is replaced, more measurements should be taken do reduce the loss.

Thirdly, this thesis proposed a fault tolerance control strategy for faulty cases. The faulty switching device can cause that some voltage space vectors can’t work as usual. While, small voltage space vectors can be replaced by other small vectors with the same effectiveness. The replacement of the certain vectors is applied to suppress the negative effect of the faulty switching device. The simulation also carried out to verify this method.

Finally, though the proposed fault tolerance control strategy can suppress the distortion of output currents, the fluctuation of neutral-point potential is too large. Thus, a Model Prediction Control strategy is introduced to overcome this drawback. This proposed algorithm is to take the difference of the neutral-point potential into calculation and accurate action times of space vectors are used to suppress the too large fluctuation. Besides that, unbalanced neutral-point potential is added to the faulty case to verify the capacity of this method.

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