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Exploring Methods for Studying Recoverability of Shipboard Electrical Power Distribution Systems

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EXPLORING METHODS FOR STUDYING RECOVERABILITY OF SHIPBOARD ELECTRICAL POWER DISTRIBUTION SYSTEMS

by

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ABSTRACT

EXPLORING METHODS FOR STUDYING RECOVERABILITY OF SHIPBOARD ELECTRICAL POWER DISTRIBUTION SYSTEMS

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Advancement of the technology included on ships, is changing the nature of loads installed on ships. Not only are there more loads than installed power generation, but advanced electrically powered weapons and sensors are changing the profile of the installed loads. These are challenges for future shipboard power systems design. Challenges which must be solved with careful distribution system planning, energy storage integration, and selection of individual power electronic converters within the ship. Different topologies and distribution systems have differing fault isolation and recovery (FIR) capability sets, which affects ship survivability. Furthermore, different FIR capability sets, operate at different speeds. The speed of a system's survivability functionality dictates the amount of energy storage needed. A goal of this work is to enable such topological comparisons.A challenge of making such topological comparisons is simulating shipboard power distribution systems. For the purposes of FIR the simulation must have accurate grounding and realistic cabling to enable study of line to line and line to ground faults in a floating system. This means the simulation must not only have differential mode behavior but accurate common mode behavior. As well as the challenge presented by the length of time required to simulate large systems by conventional offline simulation methods. By finding means to reduce simulation run times, via the use of real time simulations methods. While keeping in mind that each module has an effect on FIR efforts, which implies that the controls of each sub-system must be capable of enabling FIR topological comparisons. In this work a set of simulations of a realistic ship auxil-

iary power system with full switch models, including medium voltage and low voltage distribution, were developed and tested. This lays the ground work for future topological comparisons enabled by the simulation methodology and state machine based controls.

DEDICATION

Firstly, I would like to thank my professor Robert Cuzner for giving me opportunity to work under his guidance, keeping me on track, and influencing me to continue my education. I also need to thank my family for encouraging my curiosity from a young age. I would like to thank the United States Marine Corps for teaching me things about myself, I would have otherwise never known. As well as introducing me to the most supportive and loyal friends you could wish to have.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY OF ACRONYMS AND SYMBOLS

CHiL = Control Hardware in the Loop

cRIO = Compact RIO

dcZEDS = dc Zonal Electrical Distribution System

eHS = Electric Hardware Solver

FIR = Fault Isolation and Recovery

HiL = Hardware in the Loop

IPES = Integrated Power and Energy System

IPNC = Integrated Power Node Centers

IPS = Integrated Power System

LG = Line-to-Ground Fault

LL = Line-to-Line Fault

LLG = Line-to-Line-Ground Fault

LVac = Low Voltage Alternating Current

LVdc = Low Voltage Direct Current

MLG = Multiple Line-Ground Fault

MMC = Modular Multi-level Converter

MVac = Medium Voltage Alternating Current

MVdc = Medium Voltage Direct Current

NI = National Instruments

NLG = Negative Line-to-Ground Fault

NLSw = No-Load Switch

NPC1 = Neutral Point Clamp

PCM-1A = Power Conversion Module

PDM = Power Distribution Module

PEC = Power Electronic Converter

PGM = Power Generation Module

PHiL = Power Hardware in the Loop

PLG = Positive Line-to-Ground Fault

PMM = Propulsion Motor Module

SiL = Software in the Loop

SPS = Sim Power Systems

SSCB = Solid State Circuit Breaker

SSCL = Solid State Current Limiter

SSN = Sate Space Nodal

VSI = Voltage Source Inverter

VSR = Voltage Source Rectifier

CHAPTER 1
INTRODUCTION AND BACKGROUND

The Department of Energy defines a microgrid as "A microgrid is an integrated energy system consisting of interconnected loads and distributed energy resources, which as an integrated system, can operate in parallel with the grid or in an intentional island mode" [1]. By this definition, the electrical distribution system of a ship is a microgrid, and it follows that the development for land based microgrids and ship based microgrids are synergistic. Given the changing nature of future shipboard loads (from passive and motor loads to pulsed power loads associated with future electrified weapons and sensors), a transition from Low Voltage ac (LVac) and Medium Voltage ac (MVac) to Medium Voltage dc (MVdc) shipboard distribution systems has a lot of advantages [2] [3]. What is needed is a highly survivable Integrated Power and Energy System (IPES) that can deliver the needed power/energy through multiple routes exactly when and where it is need. The exact method for achieving survivable and flexible MVdc IPES, has not been explicitly mapped out.

A principal characteristic of a shipboard power system is that there is limited installed generation capability and the installed load significantly exceeds this capability. Shipboard power systems must also be survivable [4]. Survivability breaks down into three behavioral classifications associated with the system response to a casualty event: susceptibility, vulnerability and recoverability. From electrical perspective, the manifestation of a casualty event is referred to as a fault. More specifically, a fault is a line-to-line (LL), line-to-ground (LG), multiple line-to-ground (MLG) or line-to-line-to-ground (LLG) short circuit or impedance that is outside of specifications. Susceptibility is a measurement of the ability to avoid faults. Vulnerability is a measure of the response to the fault and recoverabilty is a measurement of the ability of the system to recover from the fault. These considerations dictate the electrical power distribution architecture and the associated equipment.

The trend for advanced shipboard power distribution systems is delivering an increasing percentage of the generated power to the loads through power electronic converters (PECs), as opposed to simply routing fixed frequency LVac or MVac power through configurable switchgear, load centers, and power panels. PEC-based electrical systems have the potential of being more flexible and reduce the susceptibility and vulnerability of the electrical system over a wider range of operating scenarios. PEC-systems can also incorporate automated functions that potentially reduce ship manning and tend to be more efficient, which reduces fuel usage [5] [6]. Because of the challenge of a high ratio of installed load to generation, it is recognized that installed load usage is a function of the current operational scenario [7]. Therefore, only a percentage of the total installed load power is delivered at any time. This operational consideration is referred to as "load diversity". As a result, even advanced PEC-based based shipboard system will still require conventional circuit-breaker based load centers at common points of voltage usage to achieve load diversity, downstream of the PECs.

Future shipboard systems will require increasing amounts of energy storage [8]. System level architectural choices dictate where this energy storage should be included. In the past, this energy storage was built into each individual load. However, as the need for more energy storage increases, the decision of where to include energy storage should also serve to further our survivability goals. In a dc Zonal Electrical Distribution System (dcZEDS), generation sources and loads are divided into isolatable zones either electrically, or electrically and physically. The increased survivability of the dcZEDS relies on the ability to electrically isolate sections of the system in the event of a fault [9]. In the Integrated Power System (IPS), electrical propulsion methods are used, and those electrical systems are integrated into the rest of the ship electrical system [10]. Either as a propulsion system zone, or as an element within a zone, if the overall architecture is zonal. By combining these ideas, the concept of a shipboard IPES emerges. Integrating propulsion power with a zonal distribution system where energy storage is included within each zone, as part of some sub-system.

Modular equipment implementations are inherent to all shipboard dcZEDS, IPS and IPES

based implementations. These systems are made up of sub-systems that are referred to as Modules. The Module itself is not a replaceable unit, but it is a sub-system having a specific functionality. For example, the Power Generation Module (PGM) is responsible for power generation. In the IPES the PGM consist of turbine, generator, switchgear and ac to dc PECs. The Propulsion Motor Module (PMM) consist of switchgear, motor drive, and motor [4]. The specific IPES architecture is derived from the functionalities that are allocated to the Modules. For example, a system that distributes the survivability functions to all the Modules (including use of PEC current limiting capability) is a unit-based protective architecture.

Given the size and scope of these systems, it is not a realistic goal to attempt to simulate a full electric ship, or a microgrid larger than some critical mass. With present day simulation tools, despite the advances in computational power made in the past few decades. With a full switching model, in order to determine the precise behavior of that system, in any given scenario; by using conventional off-line modeling techniques in software such as PLECs or Sim Power Systems (SPS). Would result in simulations with run times on the order of days. However, an alternative does exist, and in this case, it isn't to sacrifice all the detail in the model simply to make the simulation run faster, it's to sacrifice some of the detail. However, instead of eliminating all the common mode behavior via the use of average models, careful selection of simulation time-step determines what detail remains. By leveraging the speed of hardware in the loop real time simulation methods, which by virtue of the to desire integrate real controllers into simulations are required to simulate in real time. It is possible to develop a framework with which a large ship system could be modeled with much more detail than a traditional averaged model simulation, but implemented in a way that would run real time or at least faster than other simulation methods. With a methodology like that in place, further work could take place on fault isolation and recovery (FIR) of a full system. With both common mode and differential mode behaviors as defined in [11] accurately modeled, allowing for the observation of system phenomenon which would not be observed in average modeling. It is the goal of this work to explore a solution to these modeling problems, as well as the system level controls strategy needed in the implementation of a solution.

To the authors knowledge no simulation of this scale, with this level of detail has been previously completed.

This thesis will cover the following topics:

Chapter 2 Discusses the various methods and architectural configurations for achieving MVdc IPES.

Chapter 3 Discusses the state of the art of Hardware in the Loop (HiL) solutions and platforms.

Chapter 4 Introduces the IPES framework for distributing control and protective functions among the various Modules within the IPES and how these were implemented into the HiL simulation model

Chapter 5 Describes the challenging aspects of the hardware simulation, including the level of detail of the Modules, the grounding structure, the partitioning of the model between CPU and FPGA-based platforms and fault application and recovery.

Chapter 6 Documents HiL simulation results.

Chapter 7 Provides conclusions and recommendations for future work.

CHAPTER 2
SHIP POWER SYSTEMS BACKGROUND AND STATE OF THE ART

There are many advantages to using a MVdc (IPES) architecture for the ships of the navy after next. Among them is the ease of paralleling multiple power generation and storage devices. Simple voltage level matching, as opposed to voltage and phase matching when using ac, is used to connect buses. The decoupling of mechanical operation speed of prime movers from the frequency of the power they generate, which also eliminates pole count restrictions and allowing for more optimized generation by allowing variable speed generation. The operation of PECs at higher frequencies allows for smaller magnetic components due to Faraday's law [2]. Moving to an IPES changes the power and energy distribution control of the ship, from a system where machine dynamics play the largest roll in the behavior of supplying power, to a system in which the controllers of individual PECs dominate the system behavior. This is especially true when considering the implications of adding distributed energy storage to the ship's architectural design.

2.1 dc Zonal Electrical Distribution System

With the advantages of the MVdc system in mind, a dcZEDS that divides generated dc power into zones is a possible distribution methodology, that provides increased survivability. In this system, a zone is considered to be an isolatable set of loads. The survivability of this system relies on the implied ability to isolate sections of the system in the event of a fault. The definition of dcZEDS implies the redundant delivery of power from both port and starboard main MVdc buses within an electrical zone [9]. In addition, cross connections between port and starboard could be added and normally left open, to provide for additional redundancy. With these considerations in mind, it is possible for a load connected to a faulted bus to be powered by these redundant connections [12].

2.2 Integrated Power System

IPS on the other hand, implies that electrical ship propulsion would also be integrated with the rest of the ship electrical system. IPS offers many advantages on its own, such as removing the need to have prime movers for propulsion oriented a specific way within the ship and allowing any prime mover to supply propulsion power, lowering the chance of a mobility kill [9]. Not every IPS needs to use a dcZEDS as its distribution layout, nor does a dcZEDS distribution layout imply IPS. When used together, it is simply implied that the electrical propulsion system and power systems supplying ship service loads are connected. The propulsion system could either be considered to be a separate zone or could be in a module within a zone.

2.3 Integrating Energy Storage

When a resource is needed ship-wide, it is worth considering whether that resource should exist discretely, at each location where it is needed, or whether that resource should be existing in some centralized location and be distributed as needed. Just as there is not a water desalination apparatus at every freshwater usage point on a ship, nor should there be a separate energy storage solution for every load. Thus, moving the energy storage up to the system level is a reasonable course of action. This is how we logically get to IPES, by taking the IPS concept and moving energy storage aspects up into the system level design arena.

2.4 Integrated Power and Energy System

With these background considerations in mind. The IPES ship functionality is divided into sub-systems, called modules. Each module is defined by the set of capabilities and features it is expected to bring to the system. A given IPES architecture is simply a collection of these modules arranged into zones, when zonal distribution is being used, in a manner which attempts to improve the overall survivablity of the ship. The ship designer must also balance sometimes conflicting design parameters when developing a particular architecture. As the most survivable IPES might

not meet required cost, volume, or power density constraints. Given this understanding of the system level concerns, description of the module system is now required.

The Power Generation Module (PGM) is responsible for power generation. In the IPES the PGM consist of turbine, generator, switchgear and ac to dc PECs. The Propulsion Motor Module (PMM) consist of switchgear, motor drive, and propulsion motor, and is responsible for the ships electric drive components. The Power Distribution Modules (PDM) could containing either MVdc circuit breakers or no-load switches (NLSw). The PDMs allow for the reconfiguration of the electrical network. Decisions around, which portions of vulnerability and recoverability fall into the capabilities required of the PDM help drive its lower level components. Power Conversion Modules (PCM-1A) would be responsible for converting power from MV to LV and would be a possible module in which to require energy storage capability. The contents of the PCM-1A would vary based the requirements of its MV and LV interfaces, as well as the interface to its energy storage. There are other possible modules with in this overall system, to include types of PCMs other than the 1A requirement variety, some of them can be found in the following [3] [4] [8].

The decision of which capabilities and features, associated with survivability, to assign to which module drives architectural and topological design choices. A system that distributes the survivability functions to all the Modules (including use of PEC current limiting capability) is a unit-based protective architecture. If only some modules are responsible for the survivability functionality then the system is non-unit-based.

2.5 Unit-Based Protection

In unit-based protection, the features required for system surviability are distributed to all the modules in the system. This includes the current limiting abilities of PECs within the system. In the case of a unit-based protection scheme with dc bus being fed power from one or more PGMs, while also containing a number of PDMs capable of sufficiently re-configuring the bus in the event of a fault. The system would conduct operations to mitigate a fault in the following manner.

1. A fault is detected.

2. PECs feeding power to the faulted bus would need to enter a state in which they would limit and/or cut off current to the faulted bus.
3. NLSw within the PDMs open around the fault isolating it.
4. PECs re-enter normal operating modes.

If a PEC is selected, which can fully control its output current, the process is as easy as listed above. Upon detection of the fault that PEC would immediately cease power conversion and limit its output current to zero. However, in the case of a topology such as a neutral point clamp (NPC1) once the dc link capacitor of the PEC has discharged below the AC voltage at the PEC's input, the converter will simply begin to conduct through its diodes. At that point, the bus voltage is too low to keep the diodes in their blocking state. In this case, the PGM containing the converter would need to contain either MVdc Solid State Circuit Breakers (SSCB) or MVac breakers, in order to halt the current through the PEC and into the fault. At this point PDMs within the system would isolate the fault. Thus, coordination between the PECs, and NLsws in the PDMs allows for the isolation of the fault. After the system has reconfigured to isolate the fault, the PGMs, would be instructed to resume normal operation [13] [14] [15].

2.6 Non-Unit-Based Protection

In the non-unit-based approach, the simplest solution would be to attribute much of the survivability capability to the PDMs. This would require the PDM to contain MVdc Breakers. Generally, this breaker contains a current limiting element and a NLSw for galvanic isolation. The MVdc breaker is an active area of research, and not covered in this thesis, though more information can be found in [16] [17] [18] [19]. In the event of a fault, isolation would take place, via the limiting of current through SSCBs. At which point NLSw would open to provide isolation.

2.7 Impacts of Topologies on Protection Strategies

Given the above background, if attempting a unit-based architecture, the PGM's PEC either needs to be able to fully control its output current or additional equipment must be added. If the PEC cannot fully control its output current then it must be accompanied by a MVdc SSCB. A full bridge Modular Multi-level Converter (MMC) would be an example of a converter that has the ability to limit its fault current quickly [20] and could be a good candidate for the rectifier portion of the PGM. However, the down side of the MMC is the size of the converter. In the shipboard environment power density is an important design consideration at the module level. However, in a land based micro-grid functioning using unit-based protection, other constraints such as cost and efficiency drive the selection of topology. MMC based unit-based protection is certainly a possible topology choice in those applications. Other topologies capable of limiting their output current are also possibilities such as thyristor based converters. However, that speed at which a thyristor based converter can limit its fault current is slower than the MMC [21]. Furthermore, some topologies would be able to limit fault current, but would discharge their dc link capacitors requiring the converter to recharge the bus after the fault is isolated.

On the other hand, converters that cannot limit their fault current like the NPC or flying capacitor topologies would need to be paired with a MVdc SSCB and a NLSw, in order to achive higher levels of survivability. Since the maximum fault current in the ship board system is limited only by the dc link capacitors and line inductance of the short runs of cable on the ship. A MVdc breaker of sufficient size would be required in order to provide that survivability. However, since MVdc breakers are still an area of active research, parameters associated with them such as power density and efficiency are not clearly defined. When comparing these different architectures it is important to compare the power density of the full module rather than the individual components, in order to make a valid comparison. This implies that component, thermal management systems, and other ancillary support equipment should be included in the comparison. One can not say that a NPC based topology has superior power density without factoring in the size of the MVdc SSCB

and NLSw, when comparing module topologies within IPES systems approaches.

Furthermore, different PGM rectifier topologies have different FIR capability sets. To include the speed at which the FIR schemes are capable of operating. The speed of the protection scheme from fault onset to a recovered system, determines the amount of energy storage needed to sustain critical loads during fault events. Faster systems require less energy storage for survivability concerns. A goal of this work is to enable such topological comparisons. By finding means to reduce simulation run times, while keeping in mind that each module has an effect on FIR efforts. Which implies that the controls of each module must be capable of enabling FIR topological comparisons.

CHAPTER 3
HARDWARE IN THE LOOP STATE OF THE ART

3.1 Hardware in the Loop Basic Concept

The general idea behind HiL simulations is to have a simulation of some system operating in real time. When the simulation is interfaced to some manner of device under test, that exists virtually, and the entire system exists in software, this is Software in the Loop (SiL). In the simplest HiL set up, a system is simulated real time, with the some hardware existing physically. The next level of complexity is Control Hardware in the Loop (CHiL), in this case the intended controller for the system in question is developed as it is intended to be in the final product, and then interfaced to the real time simulation. In the final level of complexity, Power Hardware in the Loop (PHiL), the real time simulation exchanges power with the real physical system under test. There are many different ways to build a real time simulation.

3.2 Solver Time Step vs Switching Frequency

In the early days of power electronic real time modeling, engineers were attempting to model behavior at the power transmission and distribution level, where the cable lengths may be in the hundreds of kilometers or with line commutated semiconductors [22]. Controls solutions for line commutated semiconductors have bandwidths on the order of cycles at line frequency. Thus, the timing constraints on the real time simulation required to model these system dynamics were slow enough that CPU based solvers were sufficient to model these dynamics. When building a discrete time offline simulation, the engineer must select the minimum time-step, to see the dynamics of interest with sufficient resolution. With the introduction of PECs, higher switching frequencies, and filter dynamics, the minimum time step required in order to see the dynamics of interest has decreased. There exists a ratio between the time-step of a real time solver and the frequency of the

dynamics that is desired. Thus there is a ratio between the switching frequency and the time-step of the simulation. This ratio determines the minimum duty cycle resolution within the simulation. To elaborate, if the switching period and the time step of the simulation are too close to each other in value, then in the authors experience, the simulation will become artificially noisy. Thus, there is a practical limit to how large a time-step can be to still have a useful simulation. On the other hand, as time-steps become smaller, there exists practical limits to how fast a real time simulation can execute. An engineer must carefully consider the dynamics one intends to simulate, when compared to the time-step they must use. All models are inaccurate, but some are useful.

Additionally, when operating a CPU based real time simulator with a controller under test, there is a possibility that the simulator will receive a gate signal for a particular device in simulation from the external controller in-between its time-step [23] [24].

3.3 CPU based Real Time Models

CPU based real time simulations have existed for decades [22]. Modern commercially available CPU based simulators use a variety of different methods to model power electronic systems. Many solutions are based on nodal admittance matrices, or time sampled bridge methods [24] in order to solve for system output each time step. Simulation speed in CPU based models is highly dependent on the size of the network being simulated, despite advances in both the CPUs themselves and the methods used in real time simulation. CPU based solutions have several disadvantages when compared to FPGA based methods. CPU methods are limited to a minimum time-step bounded by the speed of their Input/Output (I/O) latency. As well as the amount of calculations that can be performed within a time-step of a given size. For usability purposes, CPU based solver platforms require an operating system. In most cases a real time operating system is used, an example of a common real time operating system is RedHawk Linux. Operating systems are by there very nature non-deterministic as are CPUs and thus have an amount of jitter. This latency can vary even when performing the same task repetitively. Jitter is the latency a process experiences due to scheduling, interrupts, and operating system tasks. An example of jitter can be seen by making

a simple C program, that counts to a few billion. Then executing the program many times, and observing the about of time it takes to execute. Due to the scheduler in the operating system, and other factors, the amount of time it takes to execute will vary from execution to execution. Jitter can limit the minimum time-step achievable.

3.4 State Space Nodal Solver

Within the set of CPU based real time simulation methods is the State Space Nodal (SSN) Method, which is used by OPAL-RT. The basic theory of operation behind the SSN method is to subdivide an electrical network into groups of smaller RLC networks. Then, an integration method is used to find the discrete equations of each group. At this point, a series of nodes connecting groups exists, the voltage and current of a given node is unknown, and must be solved for simultaneously. From the set of groups in the over all network, the discrete admittance is found, and combined to form an overall network discrete admittance, at which point the nodes can be solved for simultaneously. After this result is complete each group can have its state solved for the time-step [25] [26].

When this is applied to real time simulation methods, provided the number of nodes is small and the groups are large, the SSN method is computationally more efficient that solving the entire system in one state space matrix [25]. This is due to the larger size of matrices in a normal state space system, and the computational difficulty of inverting large matrices. With the addition of switching elements to the circuit in a real time simulation, a separate set of matrices must be pre-calculated for each switching state [25]. The number of matrices that must be pre-computed is 2^n where *n* is the number of switches. For example, a NPC1 containing 18 switches would require 2^{18} or 262,144 matrices. With the placement of nodes within the NPC1, each leg of the NPC1 can be separated from the others resulting in three groups of 6 switches per group. This results in 2^6 or 64 matrices per leg, leading to 192 matrices that must be pre-computed, significantly reducing the computational burden. If fact, OPAL-RT's Artemis solver will not permit having more than 15 switches per SSN group, due to the large number of matrices required and memory constraints.

3.5 FPGA based Real Time Models

FPGA based real time simulators for power systems are a newer development [27] when compared to the decades old CPU based real time simulation methods. Although FPGA based real time simulations for other fields have existed longer [28]. The primary advantages of using FPGA based methods is of course the low I/O latency of the FPGA platforms. Resulting in smaller achievable time steps for real time simulation compared to CPU based approaches. Additionally FPGAs have the ability to execute many computations in parallel. These factors coupled with the possibility of higher sampling rates, depending on the minimum time-step, and the ancillary hardware's ability to save data from these smaller time-steps [24]. Help make the resolution of data obtained from FPGA solvers significantly better than CPU based real time solvers. Custom made FPGA based solvers can have minimum time steps as small as 40ns [29]. Although standard commercial off the shelf systems have larger minimum time-steps Several possible methods exist for FPGA based solvers, but most use either a set of pre-calculated nodal admittance matrices or a constant nodal admittance method [29] [30] [24].

3.6 OPAL-RT's electrical Hardware Solver Intricacies

In order to avoid the problem of having multiple pre-calculated nodal admittance matrices, the electrical Hardware Solver (eHS) solver uses a fixed admittance nodal method. Switches within the simulation are modeled as a capacitor when open, and as an inductor while closed. This is done by ensuring that the discrete admittance of capacitor and inductor are constant with respect to the simulation step size. This method can have accuracy issues at high switching frequencies. The discrete time step is variable depending on the size of the circuit time-steps ranging from 100ns in a custom built single converter set-up to 1μs for a generic system, are common [31] [24].

CHAPTER 4
INTEGRATED POWER AND ENERGY SYSTEMS

4.1 Integrated Power and Energy Systems Sub-Classifications

The proceeding information broadly classifies architectures within the IPES framework. For purposes of this work, different varieties of IPESes will be defined as follows: IPES0 will represent unit-based MV protection strategies, while IPES1 will represent non-unit-based MV protection strategies. In the non-unit-based protection strategies, SSCBs are placed in series with NLSw throughout the MVdc bus, allowing the SSCBs to limit current low enough for the NLSw to open providing isolation. The ”A” or ”B” in IPES0X or IPES1X will be used to indicate whether the low voltage system is assumed to be 450 Vac at 60 Hz or 1 kVdc respectively. IPES0X-# or IPES1X-#, where # is 1 or 2 will indicate the interface between loads on the LV bus. 1 will be used to indicate the usage of Bulk low voltage buses and load centers. This implies that there are point of load converters for loads requiring different voltages than the main LV bus. Whereas 2 will indicate the usage of Integrated Power Node Centers (IPNC). The IPNC is described in detail in MIL-PRF-32272. The IPNC standard dictates that it have energy storage, in order to provide power to critical loads down stream from it, in the event of a problem up stream from it. This implies that in the IPNC containing architectures, there is energy storage at the PCM-1As as well as at the IPNC. All 8 possible combinations are shown in Table 4.1. As an example, IPES0B-1 indicates a unit-based protection plan at the MVdc level, with a 1 kV LVdc bulk bus feeding loads. Figures of each IPES system can be seen in Figs 4.1 - 4.8. This work will only simulate one architecture, but future work is planned comparing these architectures.

Table 4.1: IPES Nomenclature

Name	Unit or Non-unit	LVac or LVdc	Bulk Bus or IPNC	Figure
IPES0A-1	Unit-based	LVac	Bulk Bus	4.5
IPES0A-2	Unit-based	LVac	IPNC	4.1
IPES0B-1	Unit-based	LVdc	Bulk Bus	4.2
IPES0B-2	Unit-based	LVdc	IPNC	4.7
IPES1A-1	Non-unit-based	LVac	Bulk Bus	4.6
IPES1A-2	Non-unit-based	LVac	IPNC	4.3
IPES1B-1	Non-unit-based	LVdc	Bulk Bus	4.4
IPES1B-2	Non-unit-based	LVdc	IPNC	4.8

4.2 IPES0A-2

IPES0A-2 seen in Fig 4.1, is a unit-based architecture on the MVdc portion. The LV portion of the architecture is LVac, and uses IPNCs. In this architecture, all modules are responsible for providing survivability features to the system. The PCM-1A has the additional requirement to contain an dc to ac PEC. The LV PDMs also gain an additional requirement as they must contain automated bus transfer switches for inter-zonal connections.

4.3 IPES0B-1

IPES0B-1 seen in Fig 4.2, is a unit-based architecture in which survivability functionally is required of all modules. In this case, the system has a LVdc distribution featuring, LV bulk buses to carry power and energy to load centers. These load centers distribute this power to individual loads, which may contain their own converters depending on the load's individual requirements.

4.4 IPES1A-2

IPES1A-2 seen in Fig 4.3, is the non-unit-based twin, of the IPES0A-2. It still features energy storage at two levels within the architecture. The main change is the addition of unidirectional and bidirectional SSCB with series NLSw on the MV bus.

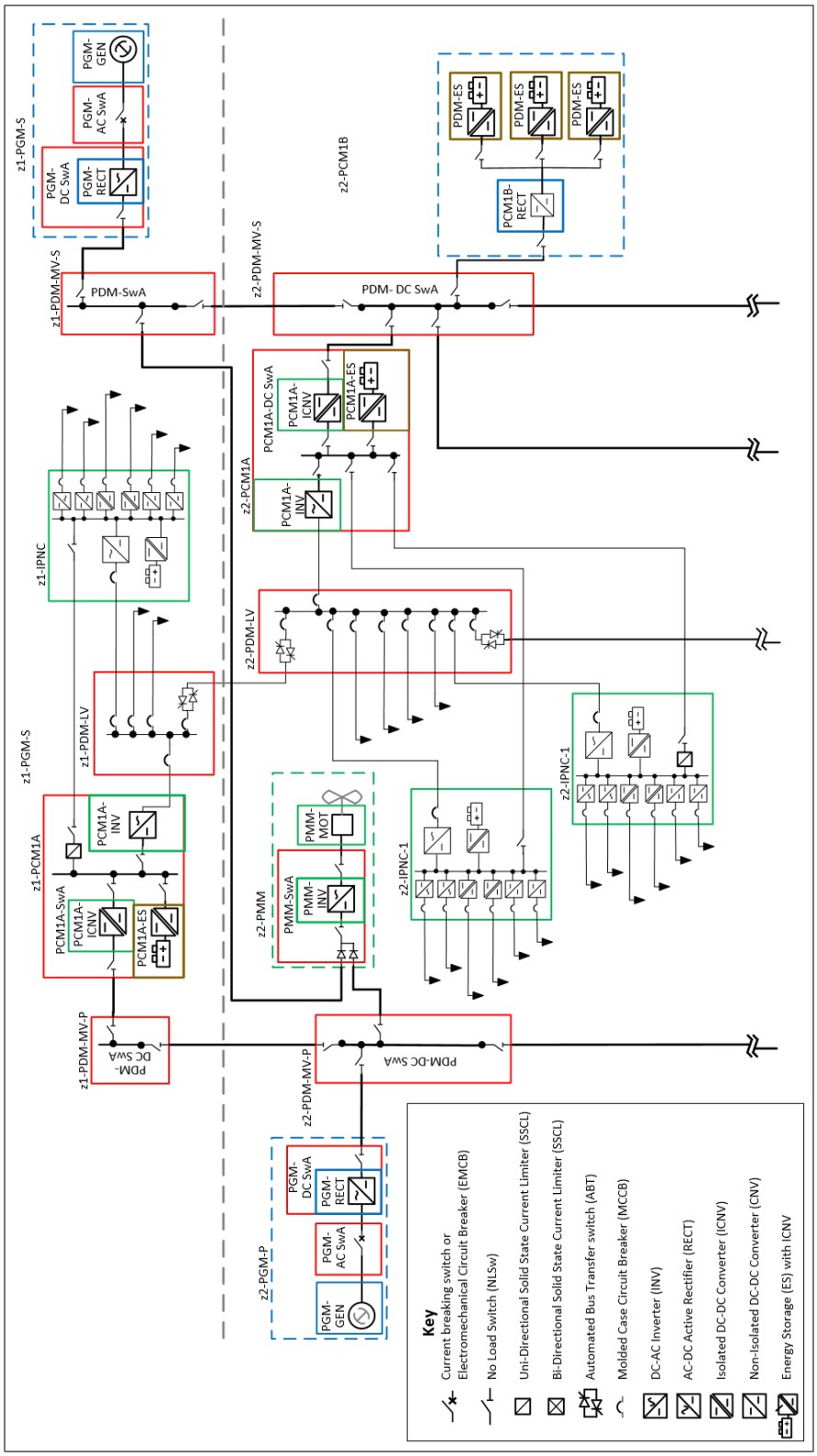

Figure 4.1: IPES0A-2

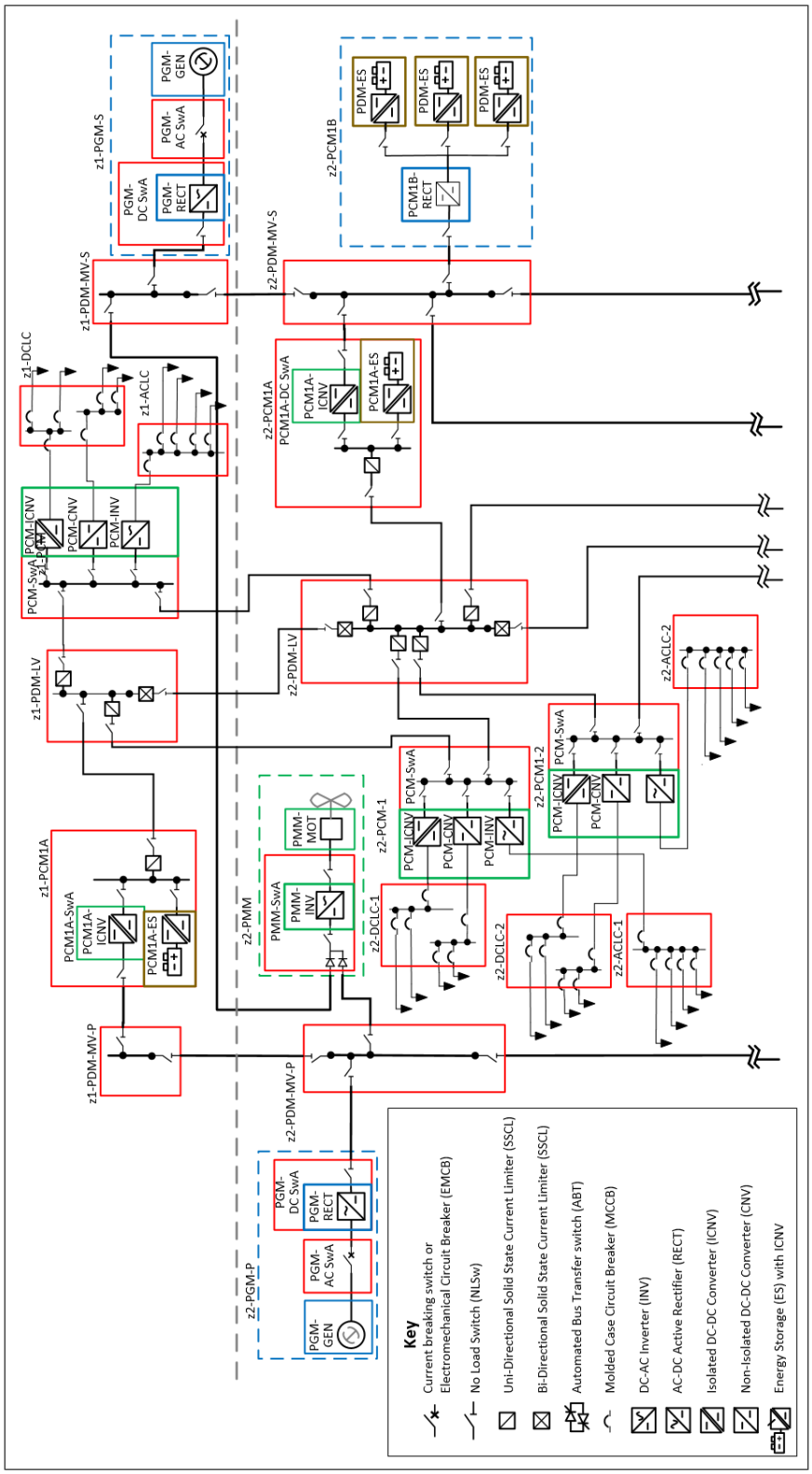

Figure 4.2: IPES0B-1

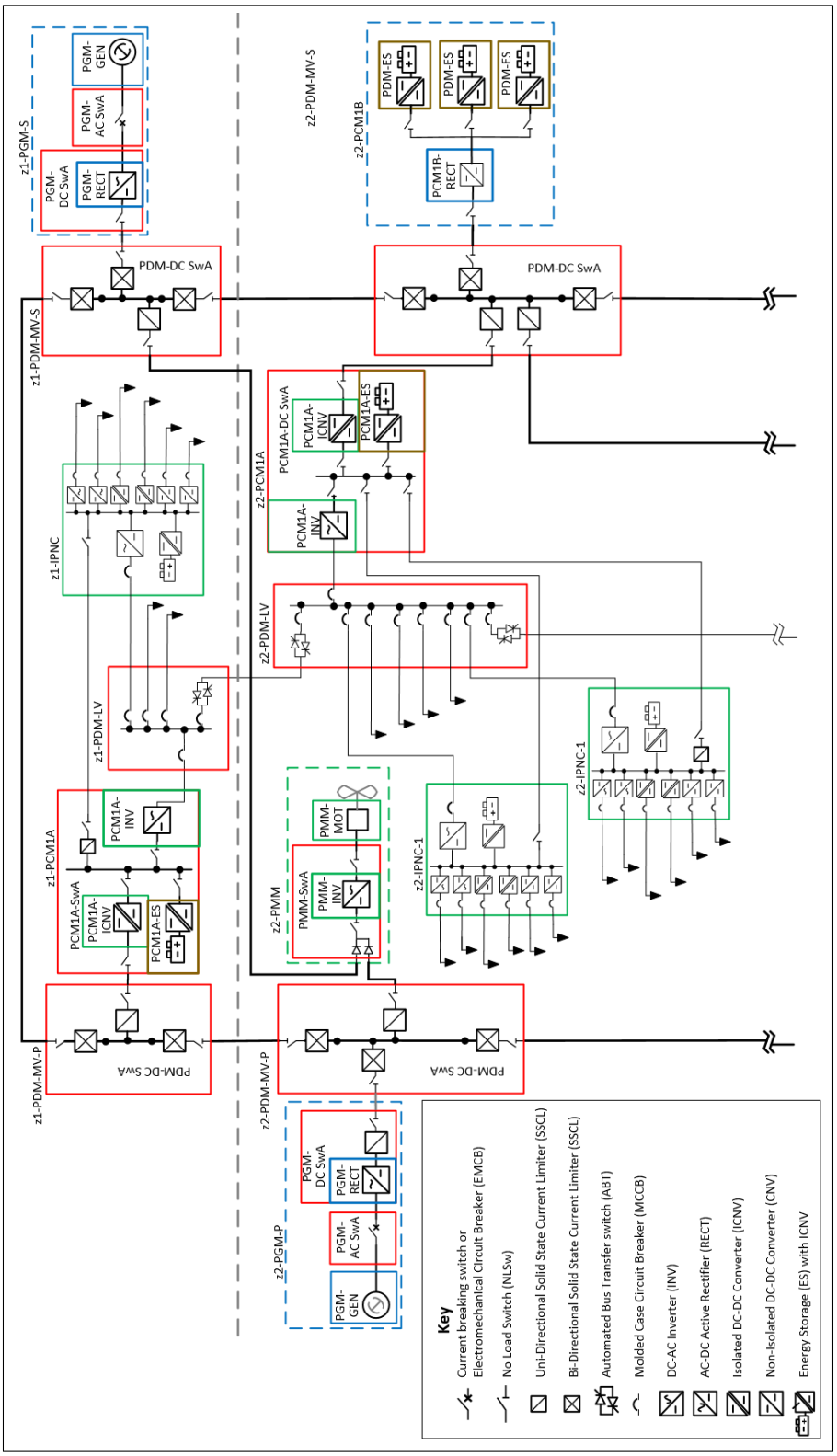

Figure 4.3: IPES1A-2

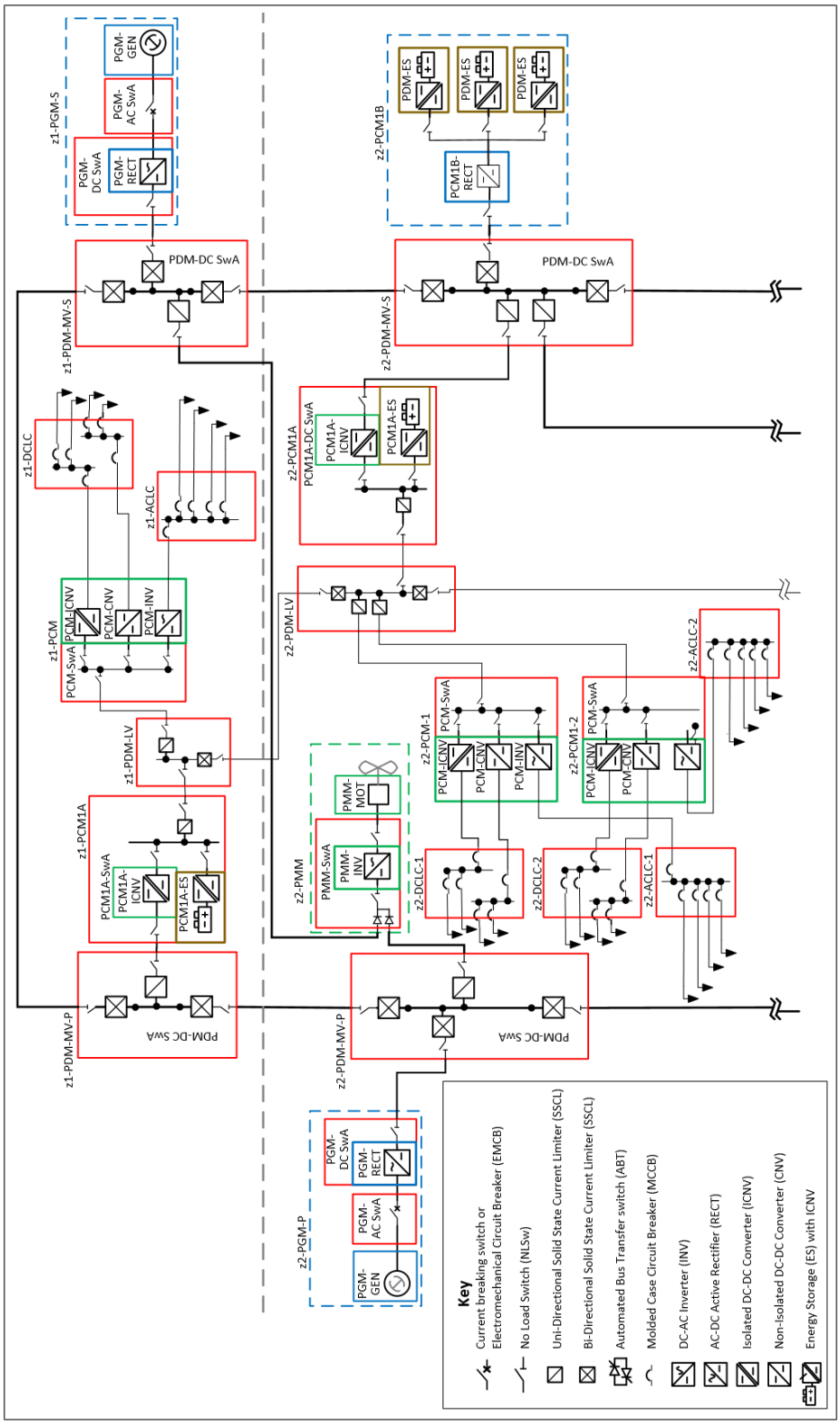

Figure 4.4: IPES1B-1

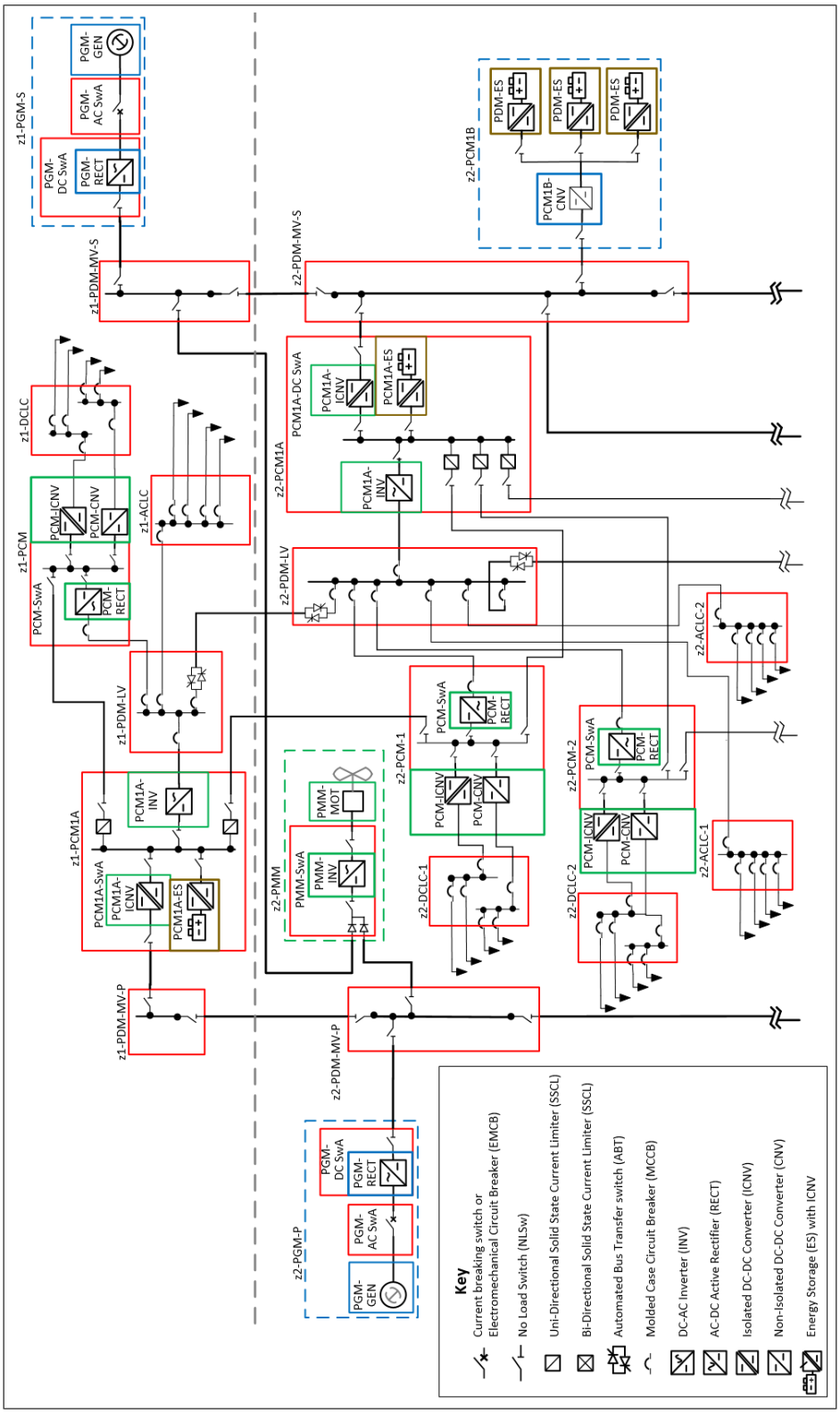

Figure 4.5: IPES0A-1

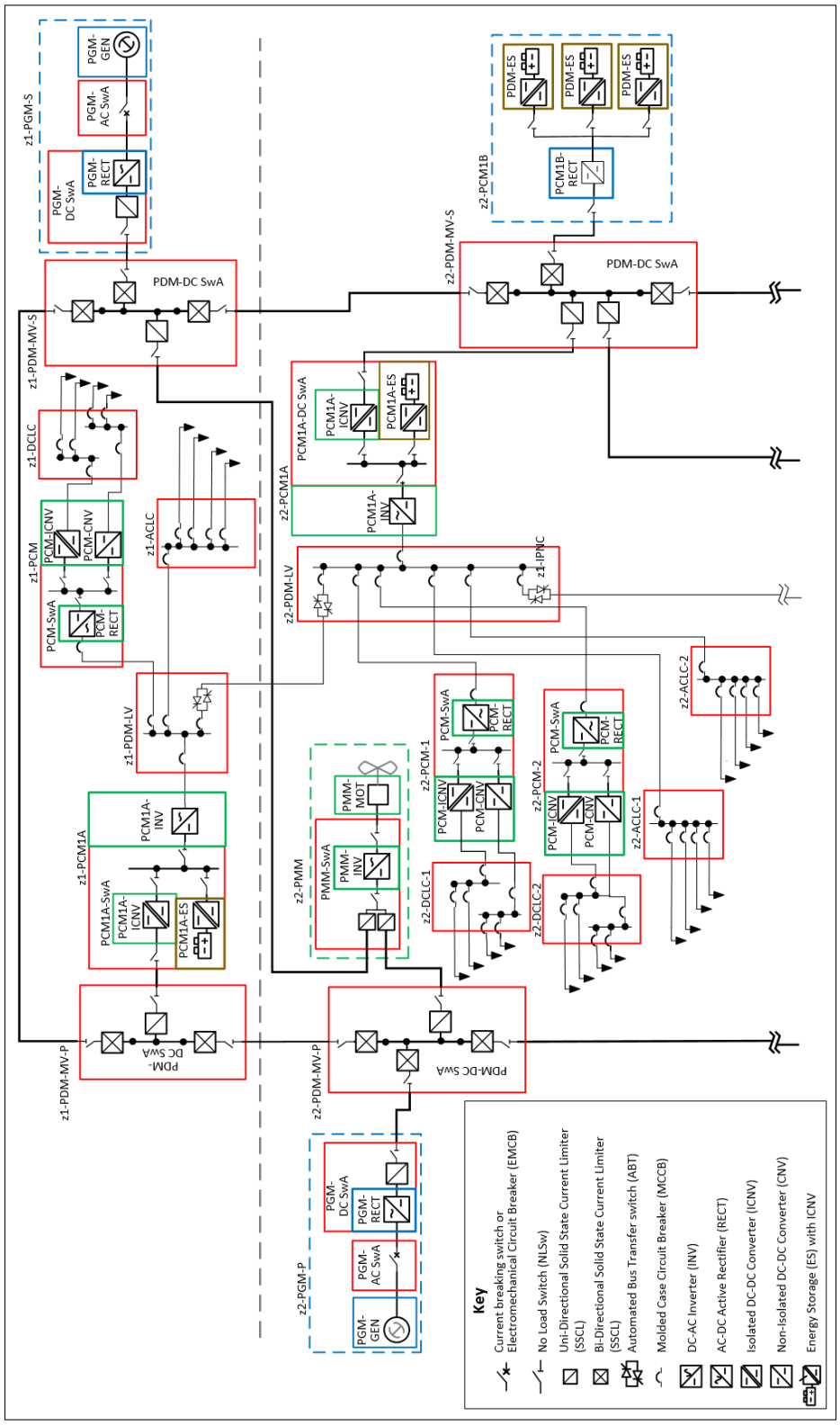

Figure 4.6: IPES1A-1

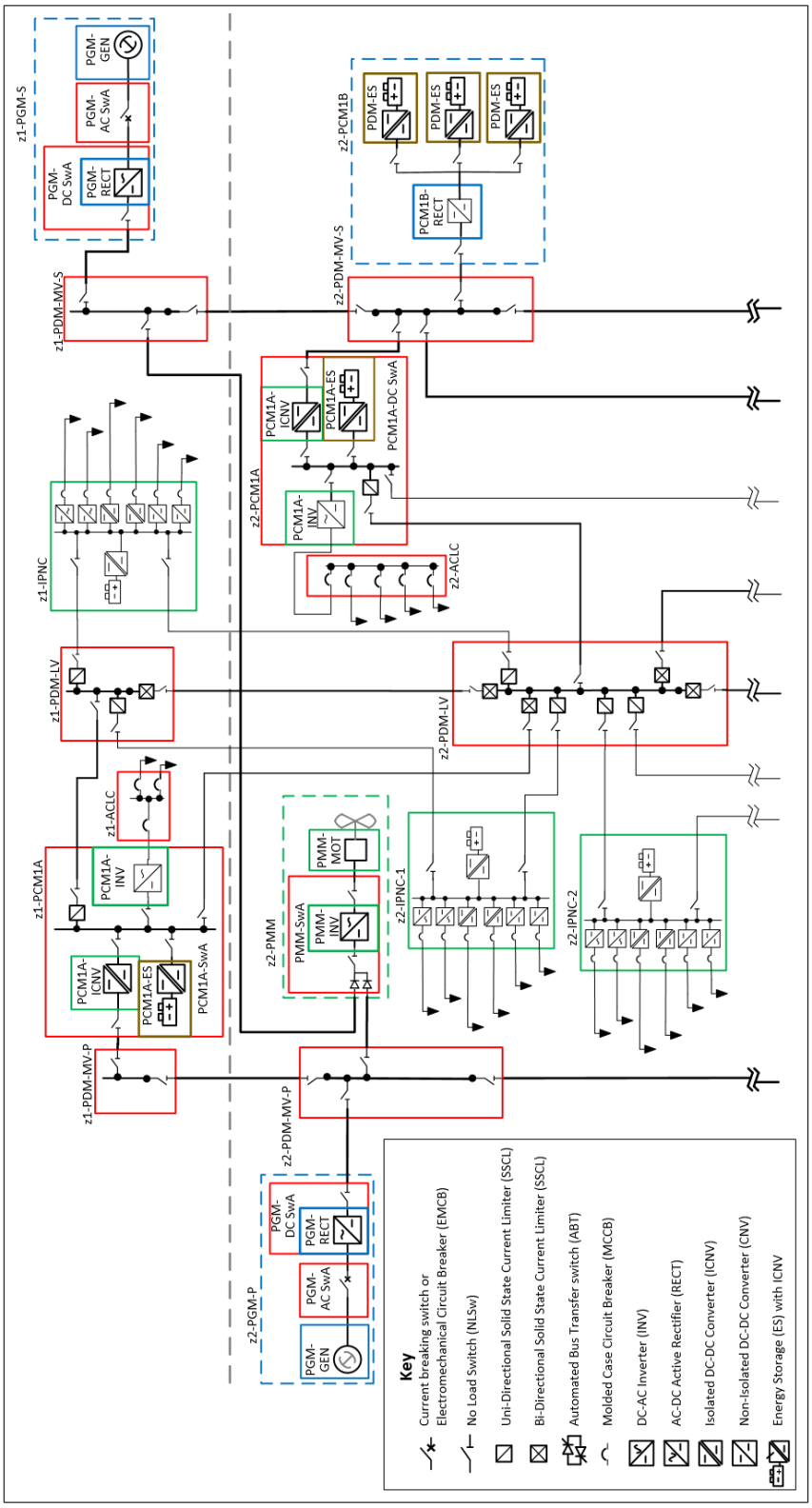

Figure 4.7: IPES0B-2

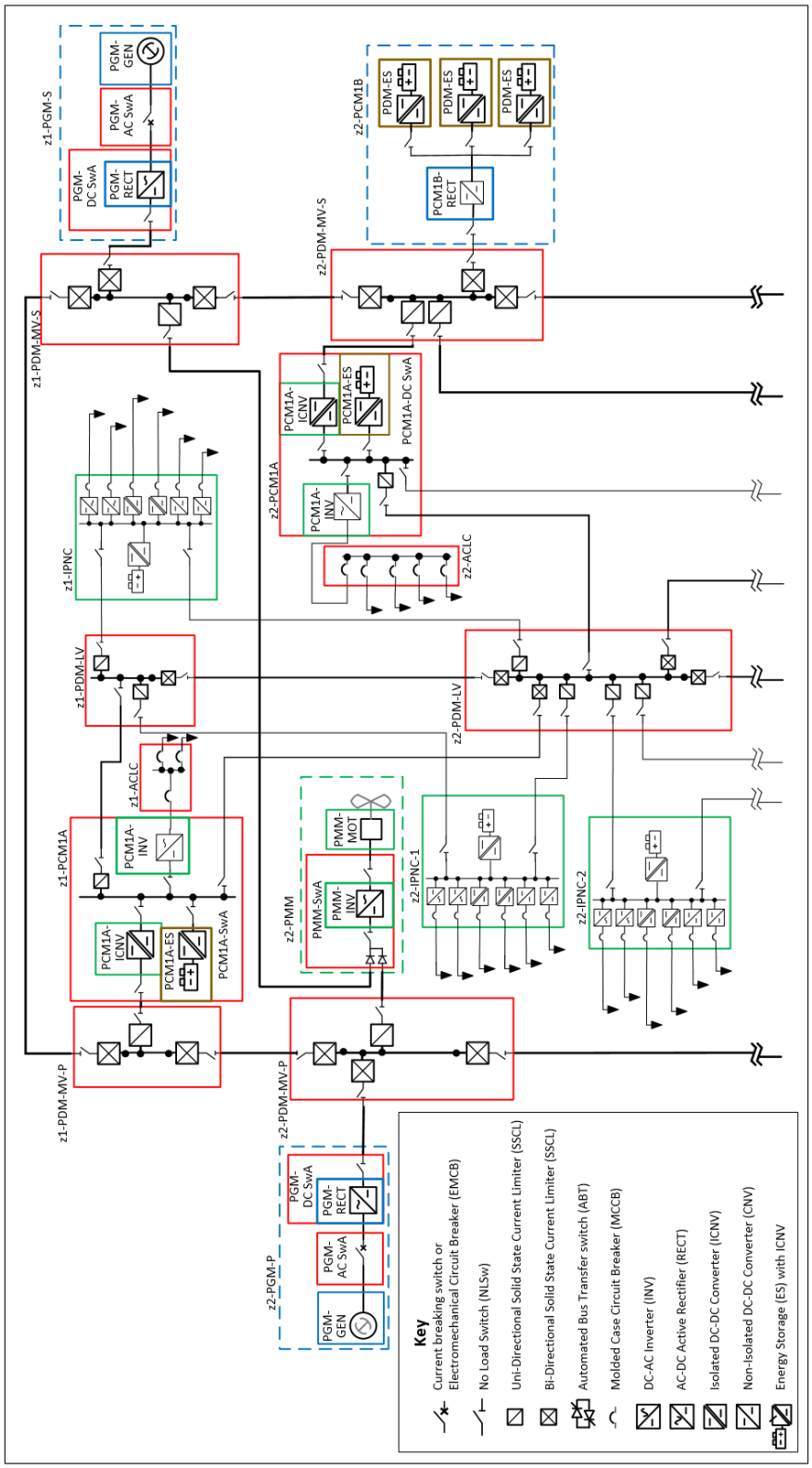

Figure 4.8: IPES1B-2

4.5 IPES1B-1

IPES1B-1 seen in Fig 4.4, is a non-unit-based architecture in which the majority of the survia-bility functionality is allocated to the PDMs. Fault isolation in this system would be handled by SSCB with NLSw in series with them. Allowing for isolation of faulted sections of the system. This system architecture also features LVdc bluk buses.

4.6 Other Possible Integrated Power and Energy Systems

Given Table 4.1 there are 4 more possible IPES configurations. They are IPES0A-1 Fig 4.5, IPES1A-1 Fig 4.6, IPES0B-2 Fig 4.7, and IPES1B-2 Fig 4.8.

4.7 Integrated Power and Energy Systems Implementation

Since the control and protective functionality are distributed across the various member mod-ules within any given IPES, it is necessary to define a control system which interacts with the other various control systems within different modules of the overall system, while also being able to independently operate if communications with other portions of the system are not avail-able, whether by design or by casualty. In order to implement this system level distributed control strategy, a series of state machines were used.

4.8 System Level State Machine

It is necessary to implement state machines for the successful control of the overall IPES. Within each major sub-system in a module, there should be a system level state machine. Seen in Fig 4.9, this state machine has states, such as Offline, Faulted, Precharge, Standby, and Online. This system level faulted state would be a state from which the converter would only exit upon receiving an external fault reset signal.

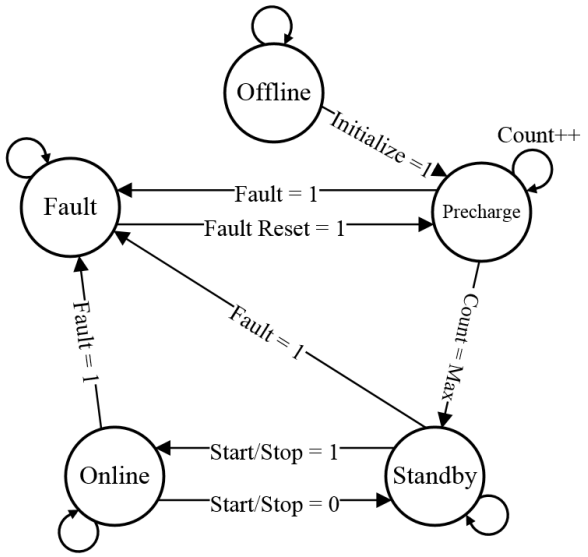

Figure 4.9: System State Machine

4.9 Ramping State Machine

Once in the online state, the converter would have a ramping state machine to control the various aspects of the converter's normal operation. Seen in Fig 4.10, whether the converter is ramping up, ramping down, or maintaining its output at any given point in time. Within this ramping state machine, an additional state should be added for short term fault 'ride-through'.

The author would like to note the distinction between ride-through in power systems standards such as IEEE 1547 [32], which governs utility grid connected power electronics systems. For 100% power electronic based distribution system like IPES, to the best of the author's knowledge, no the standard exists for ride-through, even for MVdc shipboard application [33]. One of the goals of the this research to help inform such a standard for IPES shipboard, and similar systems.

Since, there is no standard for ride-though in full power electronic based distribution systems. The precise action of this 'ride-through' state should be dependent on the position relative to the fault, the topology of the PEC in question, and its designed functionality. In most cases, the converter in question would simply be instructed to stop gating temporarily, as well as the integrators,

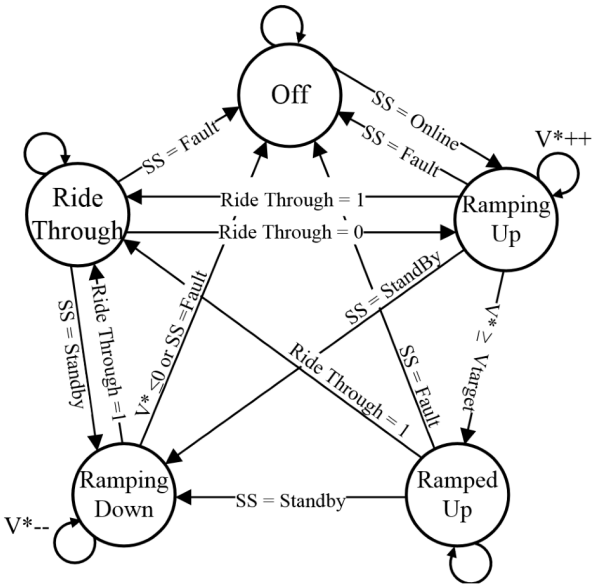

Figure 4.10: Ramping State Machine

within the modules feedback controller, should be disabled to prevent spooling. If the voltage is restored the controller will then exit the ride-through state. If voltage is not restored the converter will wait, while the fault scenario is handled external to the PEC.

4.10 State Machine Functionality

In the case of an active rectifier within the PGM, the chain of events would occur as follows. The converter is in its 'ramped' state outputting $\approx$1 per unit voltage to the bus. If an under-voltage is detected, the active rectifier supporting the bus would attempt to support the bus, for an amount of time. While controllers within the system determine if the cause of the under voltage is a fault. When a fault is detected, the converter immediately enters its 'ride-through' state. The converter's dc link capacitor discharge into the fault. In the unit-based protection topologies, the bus voltage is allowed to crash until such point as NLSw around the fault are able to isolate the fault, or the PEC limits its output current to zero. It should be noted that this assumes the converter is capable of fully controlling its output current. In the event that the PEC can not fully control its output current, a third option is required as it must have a MVdc SSCB at its output. Once the fault is

isolated, the converter leaves the 'ride-through' state, and enters a state depending on the voltage. The system level state machine may need to enter precharge, if not, then the ramping state machine could simply move to the ramping-up state, in order to resume normal operation. In a non-unit-based scenario, the converter enters 'ride-through', and waits for SSCBs and NLSws to operate in order to isolate the fault. At which point it re-enters its 'ramping up' state and resumes normal operation. In the above scenario, this signal to enter the 'ride-through' state could come either from fault detection logic internal to the PEC controls, from an external centralized fault controller, or from a distributed fault controller.

The case of an active rectifier or a dc to dc converter supplying the bus is different than a point of load converter. In the case of a point of load converter, 'ride-through' becomes a simple matter. Leaving all other states the same, when a point of load PEC on the MV bus, detects an under-voltage, the 'ride-through' state is entered and the PEC stops gating until the bus recovers, at which point it can re-enter its ramping state or precharge state depending on the conditions at the time. In the case of something like a motor drive, one could define the ramping state machines by the outermost control loops. For example, speed or torque command ramp up or ramp down.

In the case of unit-based protection with a PGM-rectifier topology that is not able to limit its output current, special considerations must be made when entering ride-through. As an example, a NPC1 active rectifier, which has stopped gating during a fault, will begin to diode rectify its input once its dc link capacitor has discharged to a low enough voltage. This implies that the current through the NLSws around the fault, would not reach zero. In this case, some other sub-system within the PGM would have to act in order to perform the current limiting function. This could mean opening the ac input breakers to the NPC1, ensuring that a SSCB is at the output of the NPC1, or some other method. Some methods are likely better than others, but some exploration is needed to determine the benefits and draw backs of each possible method. The downside of opening the ac side breaker is that now the active rectifier needs to go through its pre-charge state before beginning to 'ramp up' the dc bus again. This in turn increases the amount of energy storage needed elsewhere on the ship, to allow critical loads to continue operation while the MVdc bus is

inoperable. Adding a SSCB at the output will allow the PGM-rect to have DC link bus voltage after fault isolation, this enables a faster recovery of the bus, and therefore less required energy storage throughout the ship. The downside is that the MVdc SSCB will add size, weight, and losses to the PGM-rect. At the time of writing, MVdc SSCB is an active area of research so exact/optimal values are unknown.

4.11 No-Load Switch State Machine

To continue down the path of defining system state machines, we can apply this same approach to the NLSws within the system. For simulation purposes, this is important for correctly simulating timing delays while a mechanical switch actuates. In the case of the NLSw we can define the states as ‘opened’, ‘closing’, ’closed’, ’waiting for zero’, ‘opening’, and ‘fault’ as shown in Fig 4.11. In this case, the faulted state indicates that the NLSw has entered the waiting for zero state, and while in the process of waiting, has determined that the current is not approaching zero. After some time in waiting for zero, with the current not driving towards zero, the NLSw transitions to the faulted state. In this state machine, any signal to open the no-load switch (a fault signal or manual input from an operator, for example) places it into the ‘waiting for zero’ state, at which point the switch will wait for the current to reach zero before opening at no load. In simulation a current threshold was added as, current through switches is never actually zero, but some arbitrarily small current. Due to SPS switches being modeled as current sources, and thus the requirement for a high impedance in parallel.

The signal to open could come from another state machine internal to the modules controls or external fault controller during a fault handling sequence. The system could be designed to use nearest neighbor communication at the NLSw to perform fault locating functionality, at which point the no-load switch would send a fault signal to the energy sources on its bus, informing them of the fault, at the same time as it enters the ‘waiting for zero’ state. In simulation implementing a counter in the ‘closing’ and ‘opening’ states of the no-load switch, allows for the usage of realistic timings for mechanical switch operation based on real hardware.

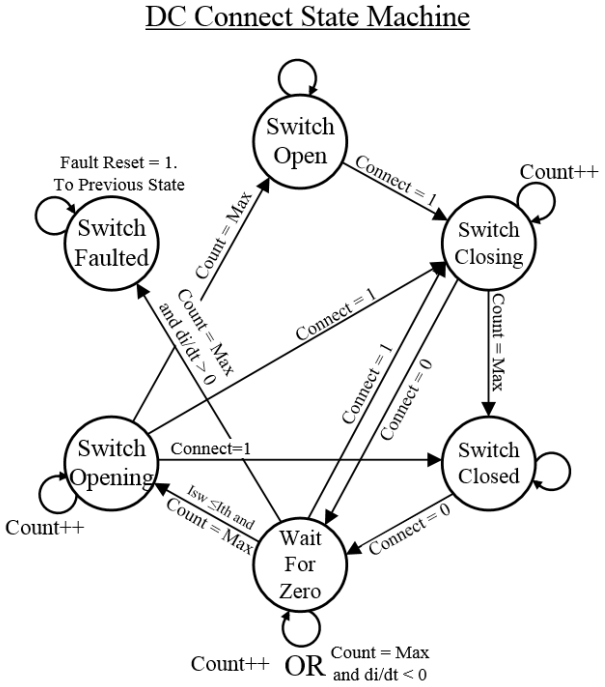

Figure 4.11: NLSw State Machine

This same no-load switch state machine can be applied to the various sub-components of a given solid state circuit breaker topology allowing for realistic timing of the opening of SSCBs in simulations. To include the insertion of delays for signal propagation and signal conditioning based on real hardware.

CHAPTER 5
HIL IMPLEMENTATION

5.1 Selection of Hardware in the Loop Tools

In an attempt to find the best way to run a simulation of the scope and size desired. Several approaches were considered, each with their own set of drawbacks and advantages. Early simulation attempts were done in Typhoon HIL. This was done by converting pre-existing Simulink block diagrams into Typhoon's block set. Typhoon's learning curve is very short compared to other real-time simulators the author has used.A power electronic component, converter or machine, takes up a fixed amount of computation resources on the hardware. Everything has a weighted score, so it is easy for the user to determine the size of the system which will run in real time.

The Typhoon can be configured to allow for more machine solvers or more power electronics solvers easily. Typhoon's strength comes from ease of integration with external controllers. The on-board processor, which runs controls, can easily handle multiple PI loops for feedback control of a converter. However, once the user begins adding multiple converters and attempting to run all of their controls on Typhoon's on-board processor, the user will quickly reach a point where over-runs are encountered. At this point, the user will be unable to have all controls operate within a single time step of their execution rate. The ease of doing core to core splits and Typhoon to Typhoon splits with Typhoon makes up for these downfalls. If external controls are interfaced to Typhoon-HiL for each converter, and enough Typhoon-HiL systems of connected in parallel to simulate all the components in the network, then this COTS platform would allow for fast implementation of RT CHiL system of IPES. During the development of this work, controllers were not developed on development boards, and available short time of development controller prototyping systems were not available in sufficient quantity to attempt to develop the system this way.

Having attempted a few models with Typhoon and having access to an OPAL-RT system, but lacking external controllers. MATLAB Simulink block diagrams were arranged in a manner that would allow them to be run real time on OPAL. With the selection of Opal-RT as a possible platform for real time simulation, there is something to be said about the possible simulation options within Opal-RT simulations. There are a few different synchronization methods that can be selected; hardware synchronized, software synchronized, and simulation synchronized. Simulation synchronized will be referred to as accelerated mode from this point forward. In both hardware and software synchronized modes the simulation runs in real time. Either on CPU or a combination of CPU and FPGA. In accelerated mode, the time to compute one timestep is non-real time.

5.2 Initial Hardware in the Loop Implementations

Early attempts at real time simulation were limited to a simple two module system with a PGM and PMM, shown in Fig 5.1, these were done initially as CPU only models with mixed CPU and eHS attempted later. The model thus appeared as described, a synchronous machine feeding an active rectifier creating an MVdc bus with a voltage source inverter (VSI) functioning with constant volts per hertz control feeding an induction machine load. A constant power load was also added to the dc bus. Both the VSR and VSI were the NPC1 topology. Time was expended on these models determining the correct way to set up the floating ground system to be tested in eventual larger model implementations. Capacitance to ground at various points in the model were estimated. Eventually line to ground faults were tested with the intention of seeing the differential bus voltage remain roughly constant while observing the common mode voltage shift with respect to ground (more information on common mode is in section 5.5). Moving a section of the model to eHS allows for higher resolution data from that section.

5.3 Logical Separations within Models

Upon getting several models working in this format, the VSR and VSI were moved into OPAL-RT's eHS FPGA based solver. The machines were not moved to the FPGA, because the additional

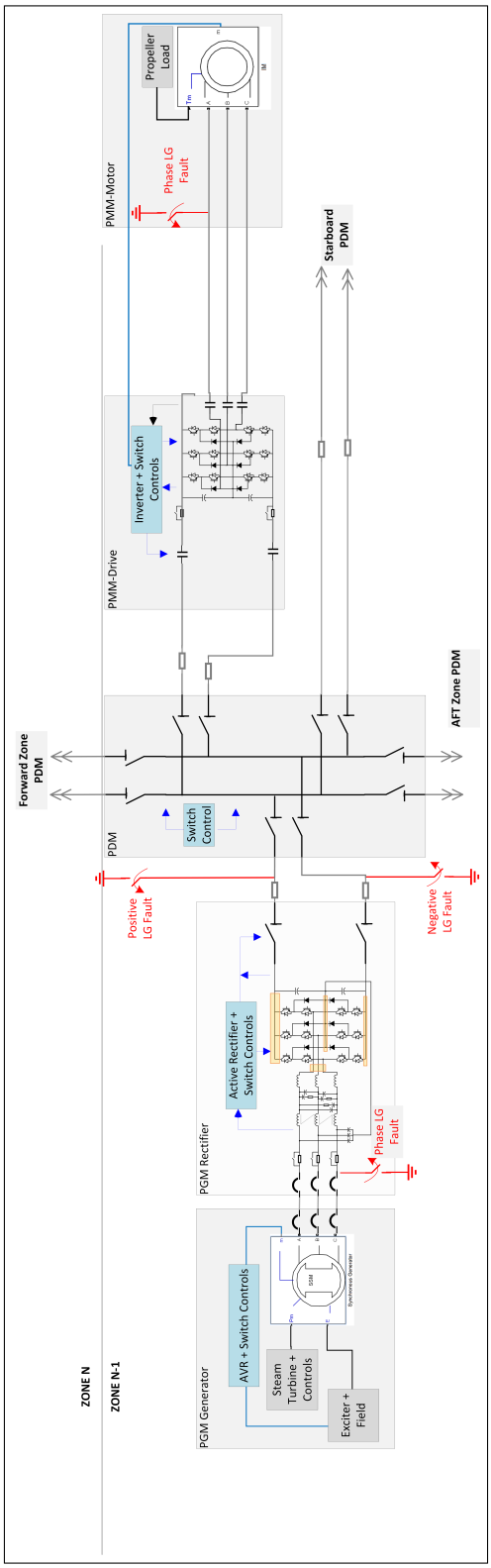

Figure 5.1: Diagram of Early Simulation Layout

machine resolution was not needed, to see the desired system behavior. In order to pass information from CPU to eHS a simple set of controlled voltage sources and controlled current sources were used. This logical separation of the model will be referred to as a 'cut' Fig 5.2. Measuring voltage on one side of the cut in the model and passing it to a controlled voltage source, while measuring the current and passing it back to the other side of the cut.

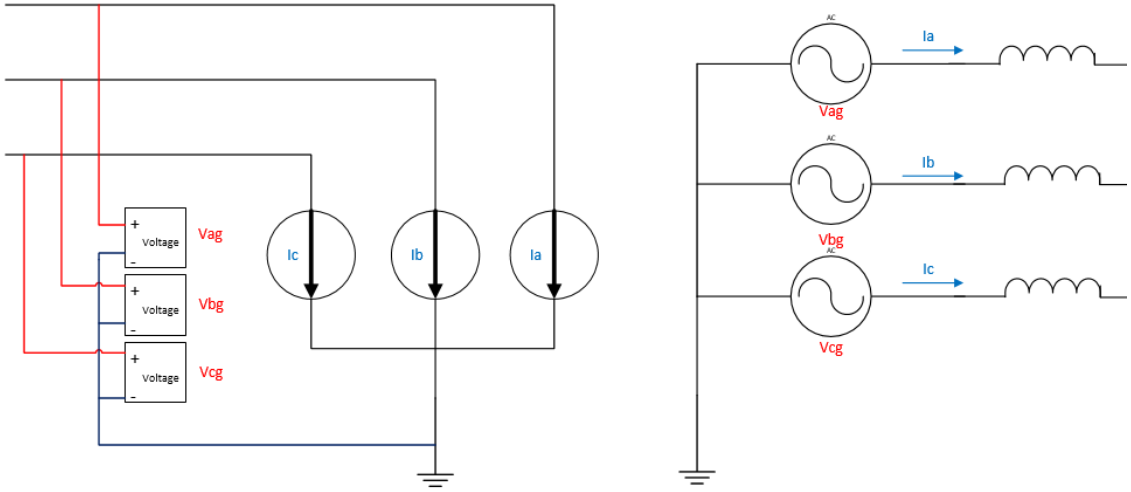

Figure 5.2: A Cut in the Model

Care was taken to make this 'cut' near an inductance that would effectively make the change in current from one time-step to the next small enough to ensure that the delay inserted by passing the information would not have a large effect on the result. An alternative to this would be to ensure that the capacitance near the cut was large enough to ensure the voltage change would be small. The thought behind this methodology is that, because the current in the inductor can't instantaneously change, nor can the voltage of the capacitor instantaneously change, the change in current or voltage from one time-step to the next should be negligible. Occasionally, the current source or voltage source at one side of the cut will require a small snubber to alleviate stability issues. OPAL-RT provides documentation on the time constant of this snubber relative to the simulation time step. With these considerations in mind, an issue to consider with this split, is that the line inductance from zone to zone on the ship is on the order of tens of μH due to the

short cable length [18]. This means that care must be taken when splitting a larger model between zones due to the small time constant of the cable relative to the time step of the simulation. It should also be noted that the differential mode time constant for dc systems is a function of the dc link capacitance and line inductance, but the common mode time constant is a function of line inductance and parasitic capacitance to ground, or in the case of some of the simulations capacitance added to approximate the distributed capacitance of the system.

5.4 Multi-Core Hardware in the Loop Simulations

The next step was to increase the model size, using the eHS x128 solver, two PGM supplied one PMM. With a switch count of seventy-nine, and seventy states inside of eHS with further states outside of eHS this model was large but well within the capabilities of the on hand OPAL-RT system. However, this increase in size pushed the controls burden on a single core of OPAL past the limit for completing all calculations within one time-step of 20 μs. To work past this problem, the model was further subdivided to allow for multi-core simulation. To avoid the problem of making many changes in a model involving complex features, and then discovering it does not work, this was first attempted without the eHS solver. Then the eHS solver was added back in later. It should be noted that when using multi-core a one time-step delay is added in-between each core. For this reason, all gate signals being sent to eHS were calculated on the same core responsible for the eHS interface. However, since the PI controllers would be able to compensate for this small delay, the rest of the controls were moved to a separate core. Given that the machines have large inductance, it was deemed safe to simply move them to a third core. In this implementation, the CPU portion of the model was running at a time step of 20 μs and the eHS solver was running close to 2 μs. However, the data being saved for the plots was reduced to a resolution of one sample every 20 μs.

Following successful line to ground fault testing in this model, attempts were made at adding realistic module base-plate to ground capacitance. These were discovered via the following method [34] and values given in [35]. Simple parallel simplifications were made where possible, in order to reduce diagram complexity. The equivalent circuit is shown in Fig 5.3. However, it was found

that the time constant of these small capacitances to ground were, in fact still significantly smaller than the time step of the eHS solver.

5.5 Challenges within Simulation Grounding

Since the system in question is intended to have no intentional grounding. A means of grounding the model for simulation purposes while preserving the floating system behavior was required. Electrical systems for marine applications use floating ground systems due to the increased survivability. A floating ground system is able to indefinitely tolerate a single line to ground fault. In order to ensure this behavior was kept while adding a minimum of simulation artifacts. The following grounding scheme was followed. The three phase lines coming from each machine, where connected to a Y of capacitors with a value of 100nF and the center point of that Y was subsequently grounded. The VSR's differential mode filter caps were placed in a Y with the center point tied to the neutral point of the NPC1, and the NPC1s neutral point was tied to ground via a 100nF capacitor. The center points of dc links were tied to ground via 100nF capacitors. Resistors in parallel were added to some of these capacitors, to enable recovery of the model from faults, the size of the resistance changes the rate at which the bus voltage recovers. Without this resistor the bus voltages would not recover from voltage level shifts associated with LG faults.

This was done in order to ensure proper common mode and differential mode behavior. Mathematically extracting common mode and differential mode from mixed mode is described in [11]. In this case, common mode behavior is defined as the instantaneous changes in voltage with respect to hull ground, and the associated currents flowing to hull ground (hull current). These common mode voltages and currents are a result of the switching behavior of the power electronic converters within the system, and the floating ground. For purposes of this work, an isolated converter is one which does not pass common mode from one side of the converter to the other. An example would be the PCM-1A, which includes a dual active bridge based solid state transformer, that provides this isolation. Although it should be noted that the switching behavior of the dual active bridge within the PCM-1A will generate its own common mode. The dual active bridge of the PCM-1A

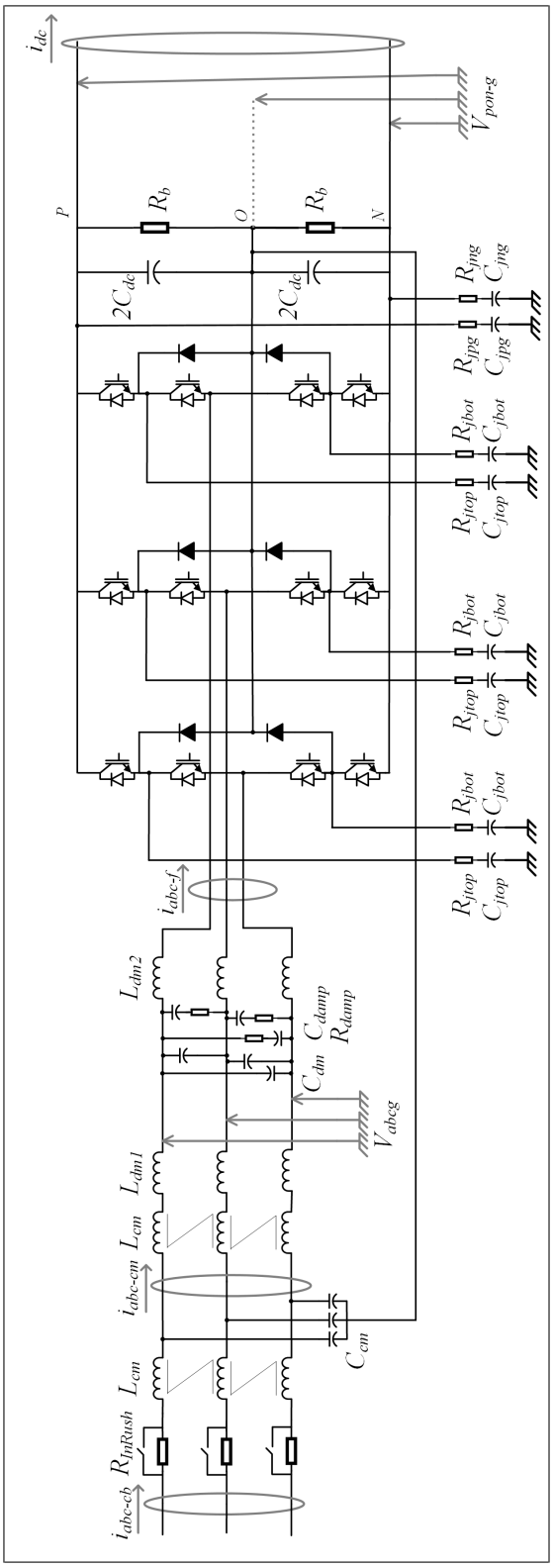

Figure 5.3: Diagram of grounding with Parasitic Capacitance

is the only isolated PEC in the model.

5.6 State Space Nodal Grounding Requirements

OPAL-RT is capable of using a SSN solver method. The SSN solver is avalible in OPAL-RT's ARTEMIS blockset. Each SSN group requires a ground reference. In cases where an SSN group split caused there to be no ground reference, a large resistance was added line to line, with a capacitance to ground from the center point of that resistance. Since the bus voltage is 12 kV a resistance was selected to minimize the amount of current through this branch that might have caused unrealistic behavior. Using a small resistance for this ground reference would behave exactly like a high impedance line to line fault. Thus, 1e8 ohms of resistance was used with the intention of pushing this simulation artifact current into a range several orders of magnitude smaller than any current of interest in the model.

In cases where the model needed to be split, the voltage to ground was measured, and the voltage sources on the other side of the cut, were directly tied to ground to ensure the ground remained the same on the other side of the split as in Fig 5.2. A possible alternative to this would be to measure the line to ground voltage and then extract the differential mode, and common mode voltage from these measurements. The method for mathematically doing so can be found in [11]. Then, use a set of voltage sources to function as each of those measurements, in whatever configuration needed to match the measurements. The same methodology applies to current. When done correctly the multiple MVdc buses should have the same ground reference, and since they are non-isolated, a LG fault on one bus should result in the same reference point shift on the other bus.

5.7 Accelerated Mode Modeling

Having gained experience with multi-core real time simulation with eHS. I am confident that given enough FPGAs running eHS, and OPAL-RT cores the entire ship could be simulated in real time, although the task would be challenging. Given cost and time constraints as well as available

hardware, this work was continued using accelerated mode.

In accelerated mode, the time to compute one time-step is non-real time. A discrete time, time step of 1 μs was chosen as the time-step for the accelerated model. The amount of time required per time-step is highly dependent on the system in question. The number of switches, states, and SSN groups directly effects the amount of time spent each time-step. When using the ARTEMIS-5 with backward Euler solver with SSN enabled, from Opal-RT. SSN groups should be kept small, in number of switches, in order to keep the amount of memory used by the system low. However, the number of SSN groups should be kept low, proportional to the number of CPU cores used, in order to ensure the simulation can be executed in real time with no computational over-runs. Optimizing the placement of SSN group splits to maximize the size of each group while keeping the group count low is thus a task when running real time.

It was discovered that as the model grew, it eventually reached a point where optimizing SSN groups to be as large as possible had resulted in memory requirements unreachable with available hardware due to their large size. As such, when running in accelerated mode, a careful balance must be reached, in number of SSN groups vs the size of SSN groups. Keeping this in mind, even a poorly optimized simulation, will run approximately 12 to 16 times faster in accelerated mode than it will in the default SPS solver. The table below highlights some of the times to complete a run of the simulation together with the number of states and switches, and the Artemis SSN approximated memory requirements 5.1. After the model grew to a particular size, it was no longer practical to spend the time to observe a full offline run. The initial runs of the model where at a scaled down power level, with various numbers of loads, or converters. The final model is similar in structure to the diagram on the following page, an IPES0B with the LV portions simplified Fig 5.4.

The final model is a four-zone ship featuring, two PGMs with NPC1 active rectifiers, one PMM with an NPC1 functioning as an inverter, four PCM-1As supplying a low voltage dc bus, and four constant power loads (see Fig 6.8). The PMM is driving an induction machine and is using closed speed loop, constant volts per hertz, based control. The PGMs are each a synchronous machine, connected to an active rectifier with inner loop Id and Iq current control, and outer loop voltage

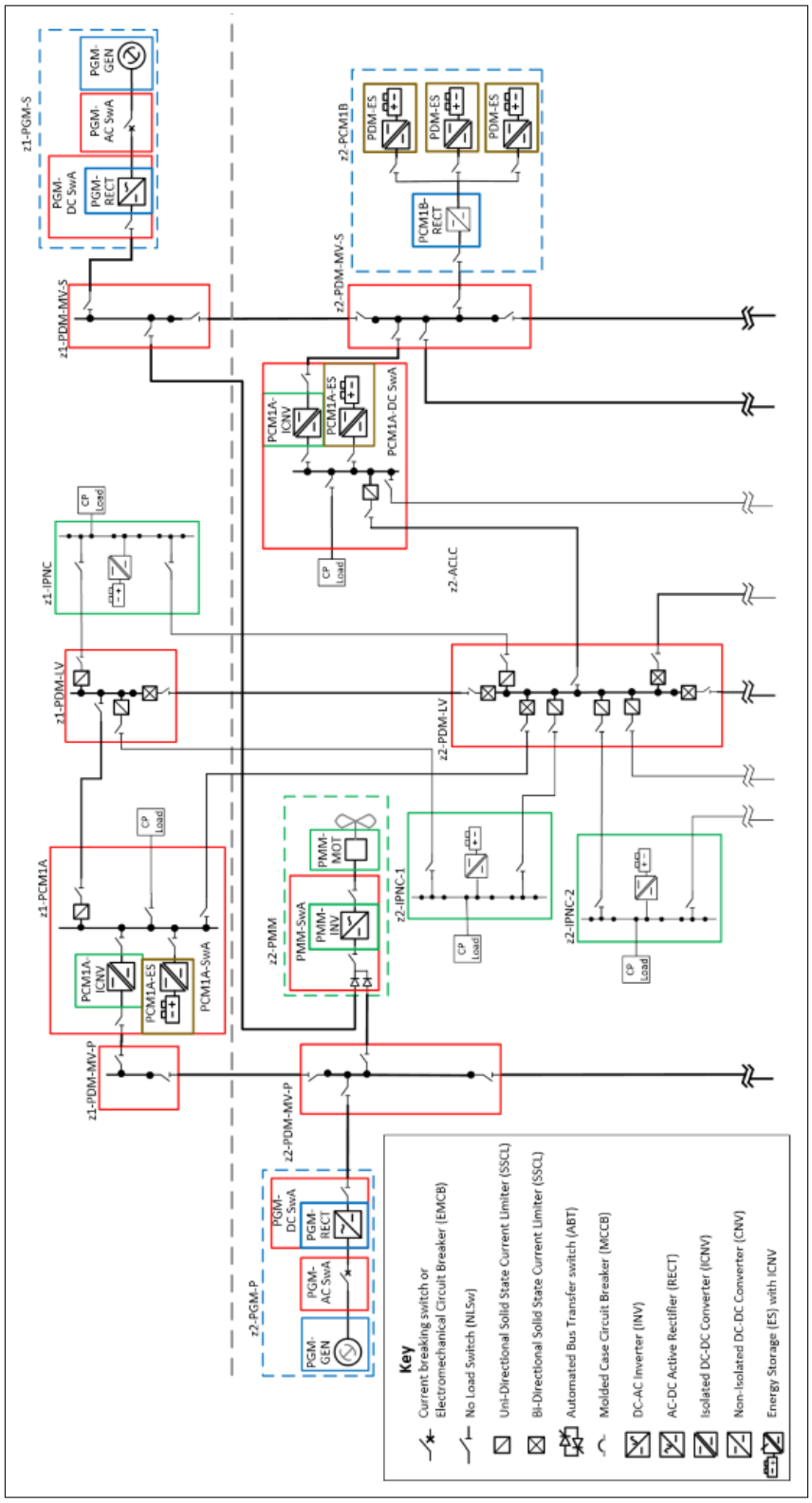

Figure 5.4: IPES1B-X Modified for Simulation

Table 5.1: OPAL-RT Accelerated Mode vs SPS

States	Switches	Memory Required (Mb)	Time Offline (hours)	Time Accelerated (hours)
119	128	269.3	6.8	0.53
219	253	770.5	16.54	1.23
221	293	843.1	Not Observed	2.15
285	319	410.4	Not Observed	2.72

control. A voltage droop was added to allow for paralleling. The PCM-1As consist of an Input Series Output Parallel (ISOP) dual active bridge. The interested reader can find more information about the NPC1 here [36]. As well as additional information about dual active bridges [37] [38].

It should be noted that auctioneering diodes were added to the positive bus lines at the input to the PCM-1A and PMM. Although there exists possible down sides to this design choice, there are also many benefits. Negative leg diodes were not added, which prevents the possibility of doubling the voltage during dual line to ground faults. However, this decision ensures negative leg common mode circulation [39]. The design decisions regarding the use of auctioneering diodes, warrants additional study in future models. Ease of locating faults must be weighted against possible downsides.

Each PGM rectifier has an output power of 2MW, while each PCM-1A has a power rating of 0.2MW. All of the constant power loads are rated at 0.1MW. At these power levels, the model is a close parallel to a ship running off auxiliary power only. As the larger prime mover chillers, pumps, ect, would require an amount of power to remain operational or become operational. Additionally, these coolers, pumps, and ancillary support systems would be considered critical loads and could draw power around this level. Interestingly in this set up, an advantage of the IPS is highlighted. The PMM can be run off these aux generators, as the motor drive doesn't care where it gets its power from. In a non-IPS ship, use of propulsion would require the starting of a prime mover connected to the propulsion shaft. Although with only 3.6MW of power available from the Aux after critical loads are satisfied, the ship wouldn't go very fast, but it would be moving.

CHAPTER 6
HIL SIMULATION RESULTS

6.1 Demonstration of State Machines Based Control Strategy

After the development of all of the state machines. The system was black started to ensure the correct operation of the state machines. At the start of this test, the synchronous machines in the PGMs were spinning, but the electrical system started at zero voltage. The PMM had an additional pre-charge stage added, to help lower its current transient upon leaving pre-charge. Some noticeable influence of the system state machines is visible in the per unit voltage of the PGM-rectifier and PMM-inverter dc links Fig 6.1.

1. PGM-rectifier is in Pre-charge.
2. PGM-rectifier Pre-charge ends the voltage quickly climbs to the diode rectified voltage level, and the voltage command is 'ramped up' to 1 per unit.
3. The NLSw state machine at the PMM's input exits the closing state entering the closed state, connecting the PMM to the bus.
4. The PMM leaves the first stage of Pre-charge, and enters the second stage of Pre-charge.
5. The PMM leaves the second stage of Pre-charge.
6. The PMM dc link reaches 1 per unit.

6.2 Piece-wise Linear Electric Circuit Simulator vs electrical Hardware Solver

Modeling parasitic capacitance of the NPC1 converter in PLECS is the first simulation result shown. Determining the size of the time-step of the simulation as well as the refine factor, was something of an iterative process. Smaller time-steps increased both the simulation run time, and the size of the output data file. To put things in perspective, each time-step, each signal outputs

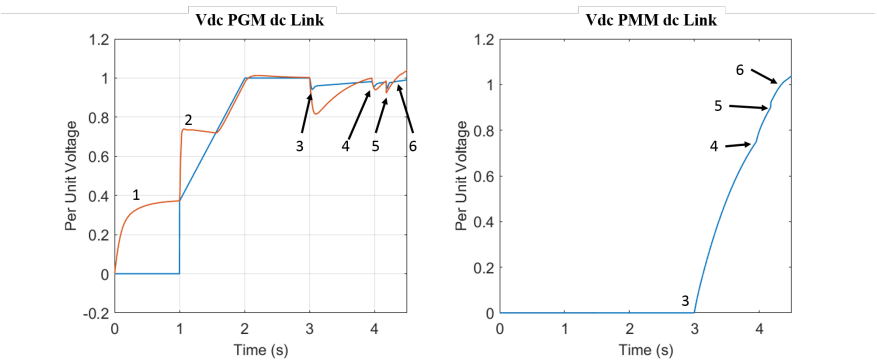

Figure 6.1: Black Start of the Testing Model

a double precision floating point value, at 8 bytes in size. So, saving just two voltages and a current at a time step of 100ns for a simulation one second long, yields 30e6 double precision floating point values. This will end up being roughly 250Mb for one second of data. There comes a point where making the time-step smaller is just plotting artifacts of the simulation, or the lack of modeled skin effect and other phenomena that would normally be modeled in a finite element analysis simulation. Fig 6.2 below is a Positive Line-to-Ground (PLG) fault .

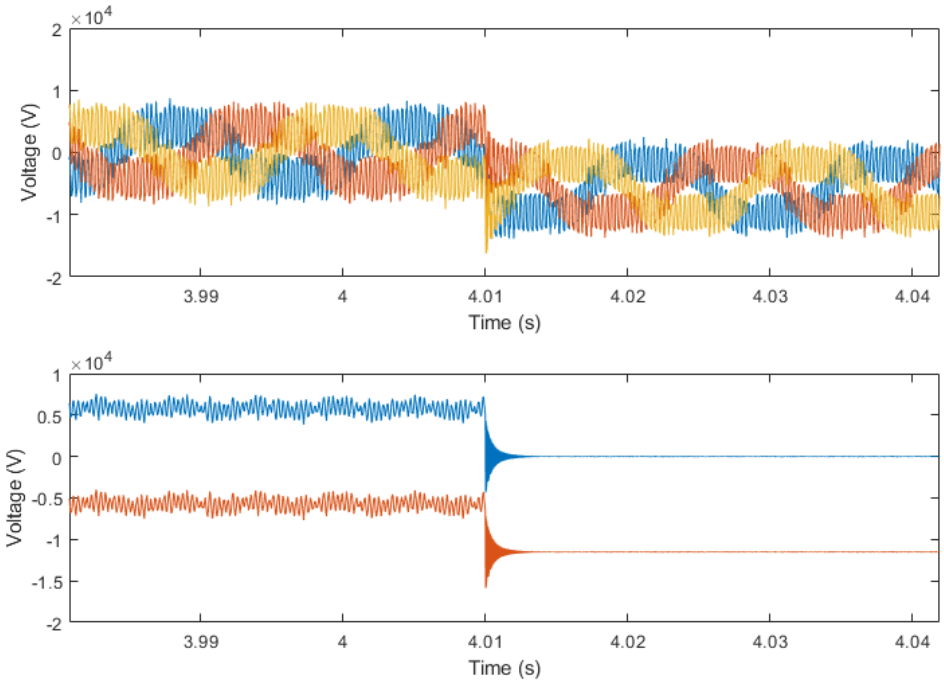

Figure 6.2: PLG Fault in PLECS with Realistic Parasitics

Following that the same simulation was built in eHS. However, due to the time step of the FPGA solver the oscillations around the fault did not appear in the results. When the same PLG fault was applied. Seen in Fig 6.3.

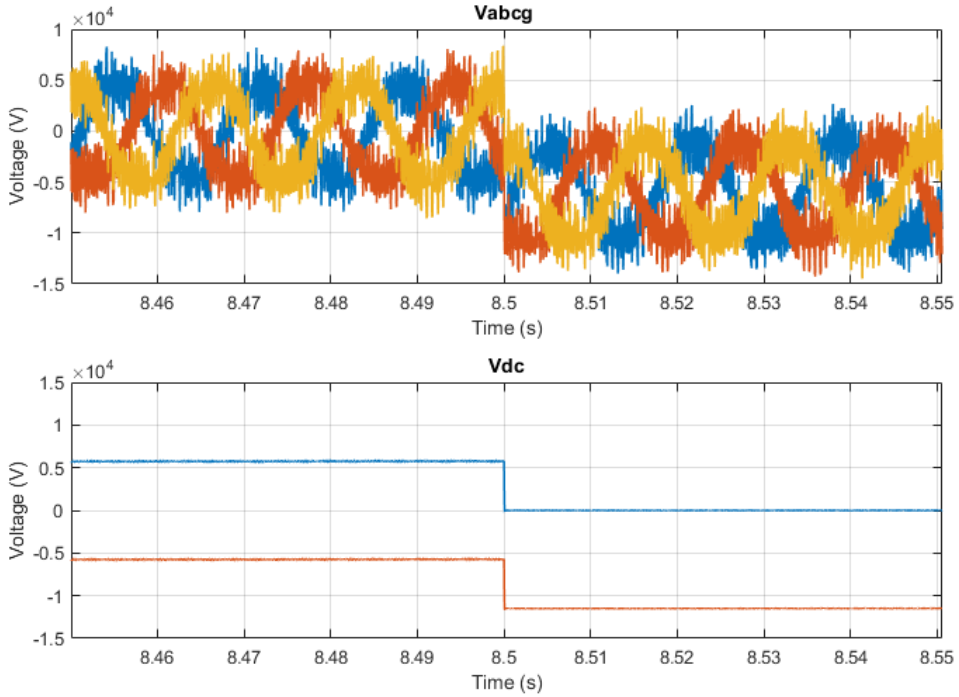

Figure 6.3: PLG Fault in eHS with Realistic Parasitics

Since it was now proven that the time-step of eHS eliminated all, the ringing from the parasitic capacitance. Further models simplified this capacitance to a total of 100nF. This preserves our floating ground. While simply neglecting a phenomena that are too fast relative to the time-step of the simulation. All models are inaccurate, but some are useful. At least in this case the inaccuracy is known.

6.3 Fast Fault Transients

In order to see these fast fault transients, a custom FPGA simulator with a faster time-step would be required. Parallel work has yielded results using a custom solver on a National Instruments (NI) platform [30] [40]. During the testing phase of this work, controls built in NI Compact RIO (cRIO)

were interfaced with an OPAL-RT model to ensure proper controller function. A Control Hardware in the Loop (CHIL) set up was used that can be summarized in the following diagram 6.4.

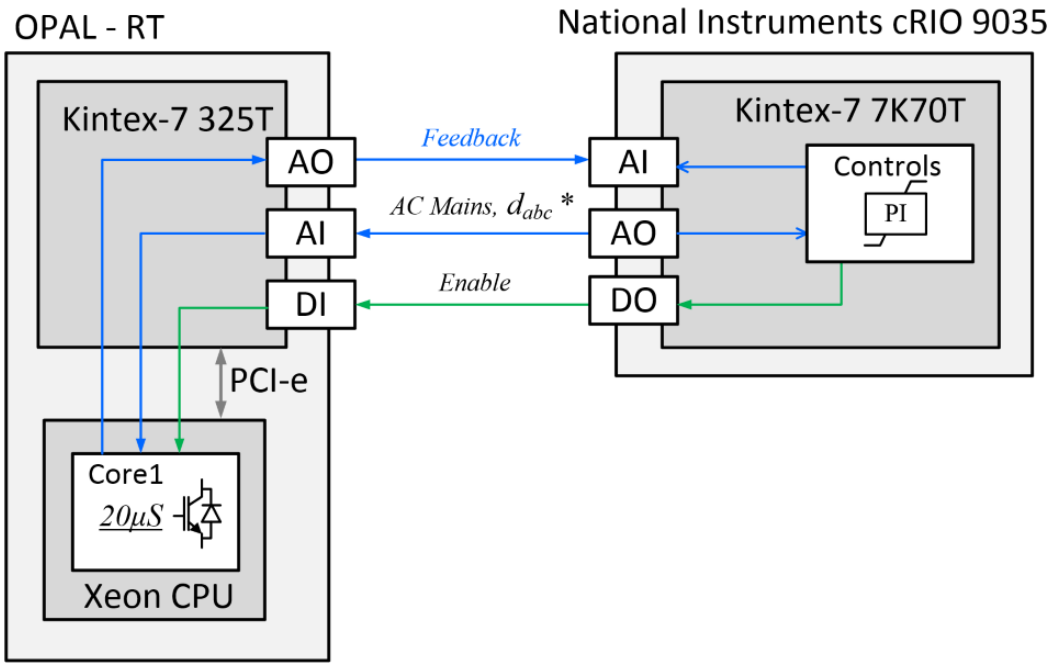

Figure 6.4: CHiL System Configuration

Once controls issues were troubleshot using this configuration, the cRIO controls were interfaced with the solver on the same FPGA as the controls. This allowed for data logging to occur at a rate of 20 MHz [40] (as well as an additional work by the same team of authors not yet published).

6.4 Multi-Core electrical Hardware Solver Simulations

Following this work multi-core and multi-core with eHS simulations were conducted. These simulations allowed for the development of the technical know-how, to build a full ship model. The ability to build a full ship model being limited by two factors, time and available hardware/software licensing. Below are figures highlighting the two separate builds done in order to determine this feasibility 6.5a 6.5b.

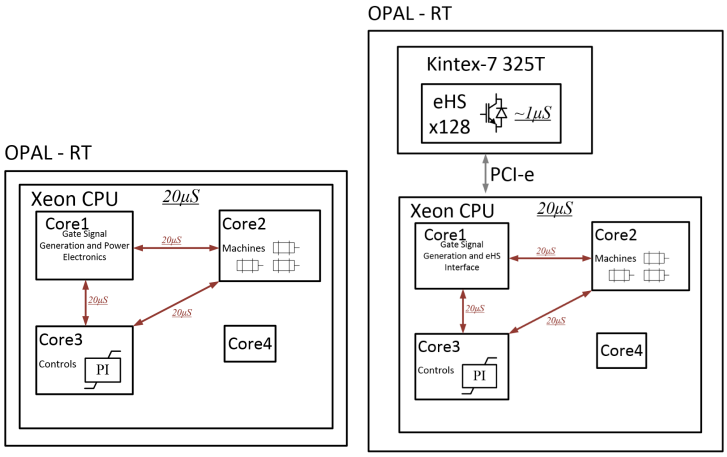

Figure 6.5: Simulation CPU and FPGA Configuration: (a) Multi-Core Simulation, (b) Multi-Core with eHS Simulation

6.5 Testing Smaller Models

Following the work in multi-core eHS models, the decision was made to pursue accelerated mode models. As a fast run time relative to the size of the model is a requirement, but available hardware limitations were going to become an issue as the model grew in size. This model had become too large for iterative testing. So, a small test bed model was constructed in order to test features to be used within the larger model. This test model was built in such a way that it could be run real time. However, running such a small model in accelerated mode, resulted in faster than real time, run times. The test model was built with a variety of loads designed to be substituted for each other, as an individual testing need became apparent. It was during a series of tests using this model that it was discovered that the LL fault behavior, of the test model did not mirror the expected behavior. It turns out that the Artemis solvers three level bridge leg model. Was the source of this unexpected behavior. The bridge leg functions correctly when switched, the bridge leg diode bridges correctly when not switched, but the leg will not simulate the unexpected operating conditions during a fault. To bypass this problem and get underway, the Artemis solver was disabled, and the leg replaced with discrete SPS blocks. Following these changes all testing model behavior was as expected. However, disabling the Artemis solver resulted in slower model

execution rate. Seen below are a LL fault Fig 6.6 and the isolation of a LL fault Fig 6.7 in the testing model.

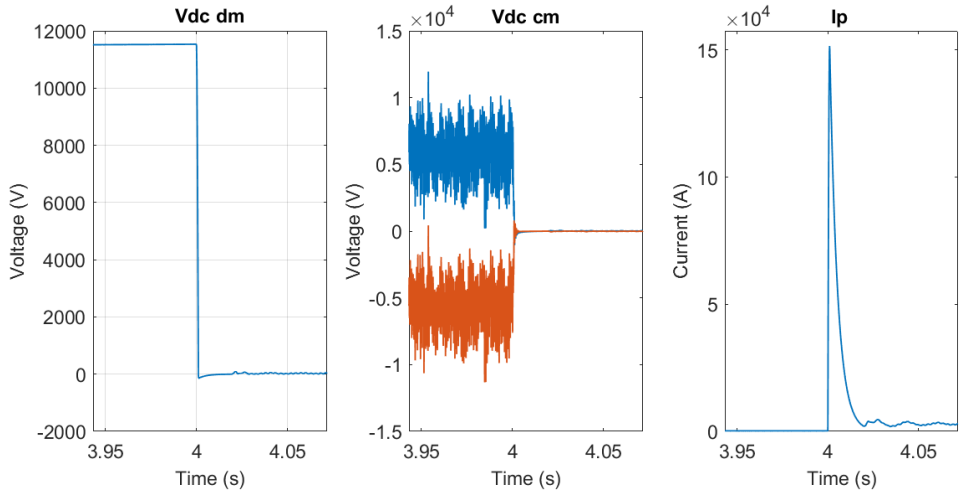

Figure 6.6: LL Fault Testing Model

Once correct fault behavior was verified, a modified version of the no-load switch state machine was added. This modified version was designed to mimic a SSCB with an 80us delay from fault detection to opening of the breaker Fig 6.7.

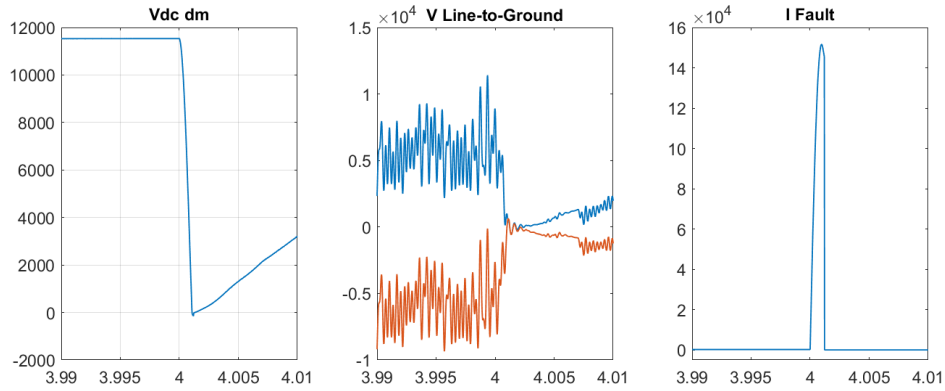

Figure 6.7: LL Fault Isolating in Testing Model

Having successfully isolated a fault, in the testing model all the controls pieces are in place to test non-unit-based protection. However, an accurate model of a MVdc SSCB has not yet been constructed.

6.6 Accelerated Model Results

Integration of lessons learned in the testing model were added to the main model. At which point a series of tests were conducted. The accelerated model has a discrete time step of 1μs. However, it should be noted that running the controls this fast would be unrealistic. Thus the controllers and state machines within the model were run at slower time steps of 20μs or 80μs. It is also important to note that the summation of loads on the LVDC bus is less than or equal two the maximum output power of two PCM1As. This decision allows for the loss of one MVDC bus, within this simplified four zone model. While maintaining power to all loads on the LVDC bus. The sizing of the output power of the PCM1As and each zone's low voltage constant power load, is such that a given PCM1A can supply power to two zones. In the event of losing three out of four PCM1As in the model, load shedding would be required. As of yet, no load shedding logic is in the model, future efforts could add load shedding logic to the loads on the LVDC bus. Putting some of the constant power loads into a low voltage ride-through state would be an effective way of implementing this. This represents a problem with the sizing of the PCM-1A maximum output power, and not the amount of energy storage available. Although, tests to determine how much energy storage a PCM-1A should contain for survivability purposes are an area that can and should be studied in the future.

Following this point, a series of faults were added to the model, to ensure their behavior was as expected. Note, the only fault not yet defined earlier is the negative line-to-ground fault (NLG). In the first three scenarios is a single fault on the MVDC bus between PDMs in Zone2 and Zone3. The fourth fault scenario is a PLG fault on one bus with a NLG fault on the other MVDC bus. Seen in Fig 6.8.

Initially a PLG 6.9 and NLG 6.10 fault were tested independently. Followed by a LL fault, all these faults were applied to the starboard side bus, which is fed by the zone three PGM. Below are the plots of the voltage at various points in the system, during these faults. Only one PCM-1A MV bus was shown here since the behavior is similar in the other PCM-1A 6.11. The PCM-1As on

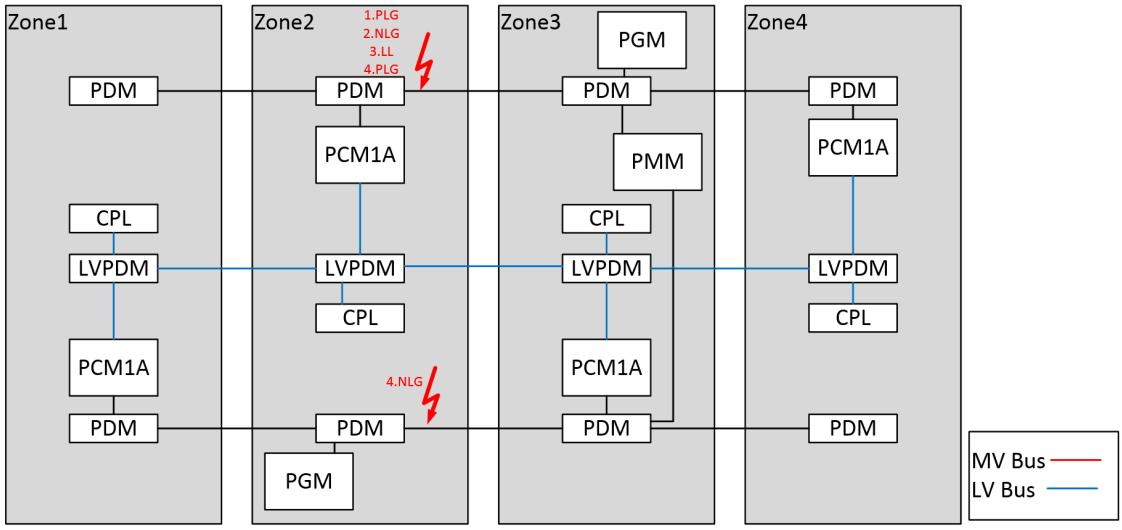

Figure 6.8: Accelerated Model Implementation

the faulted bus, enter their low voltage ridethrough state, and stop providing power to the LV bus. The auctioneering diodes at their inputs prevent the PCM-1A capacitors from discharging into the fault. The Voltage and current at the LL fault can be seen in Fig 6.12.

At this point a PLG fault was added to the starboard side bus, and a NLG fault was added to the port side bus. Since the system lacks isolation between these two buses. The behavior should be that of a LL fault. The common mode currents of the port and starboard inputs to the PMM together have the same waveform shape as a Line to Line fault. With one bus contributing the positive leg behavior, and the other contributing the negative leg behavior; due to the presence of auctioneering Diodes.

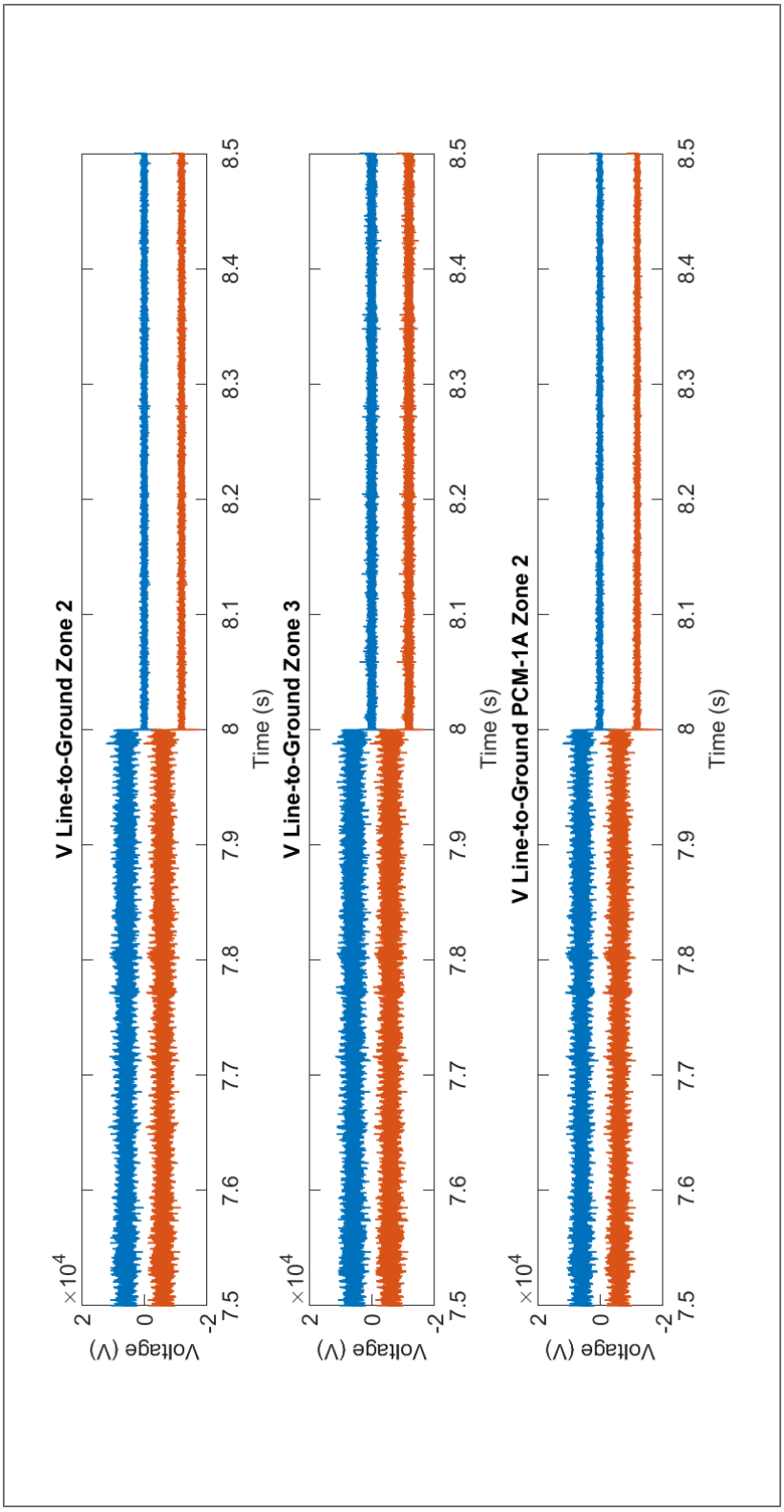

Figure 6.9: Accelerated Model Positive-Line-to-Ground Fault

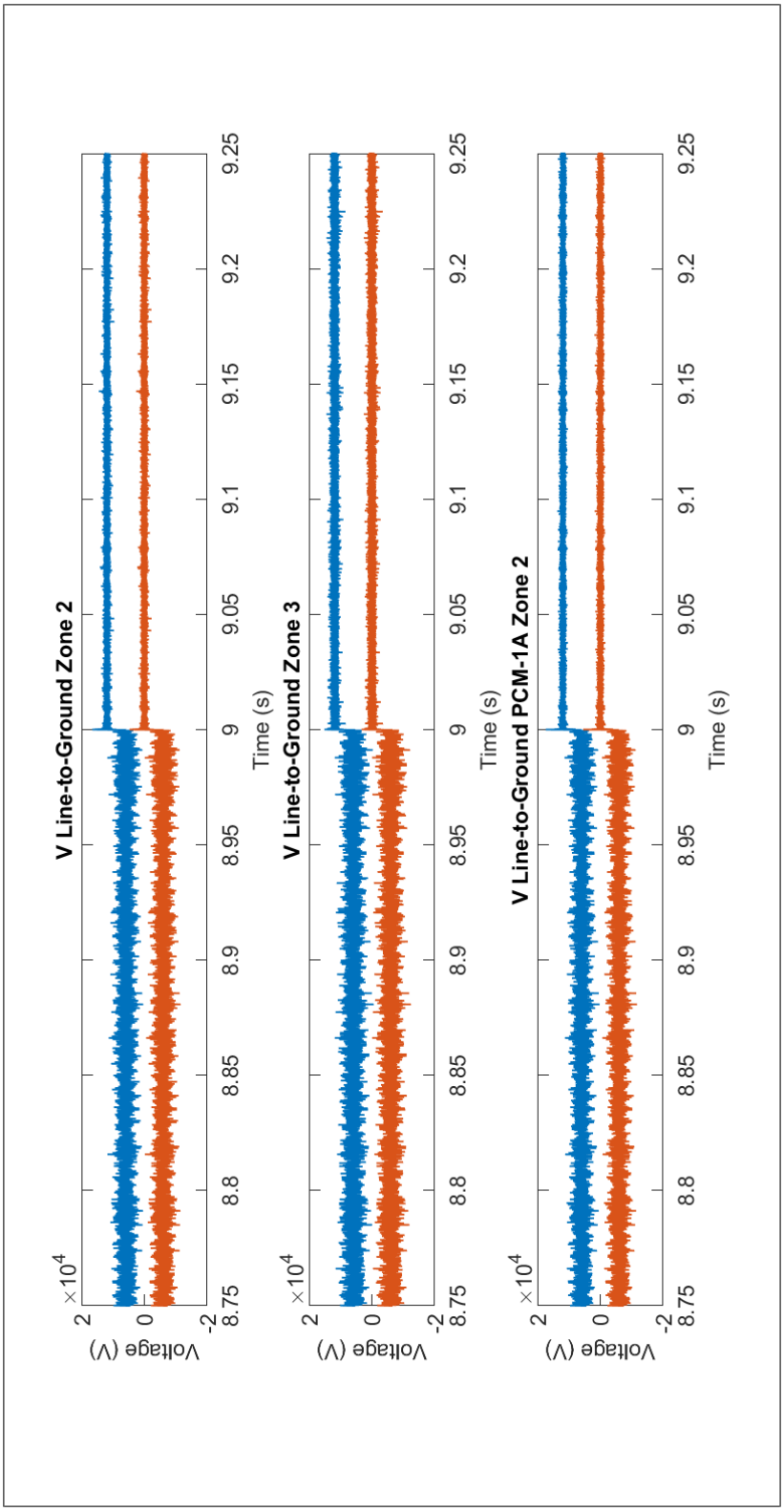

Figure 6.10: Accelerated Model Negative-Line-to-Ground Fault

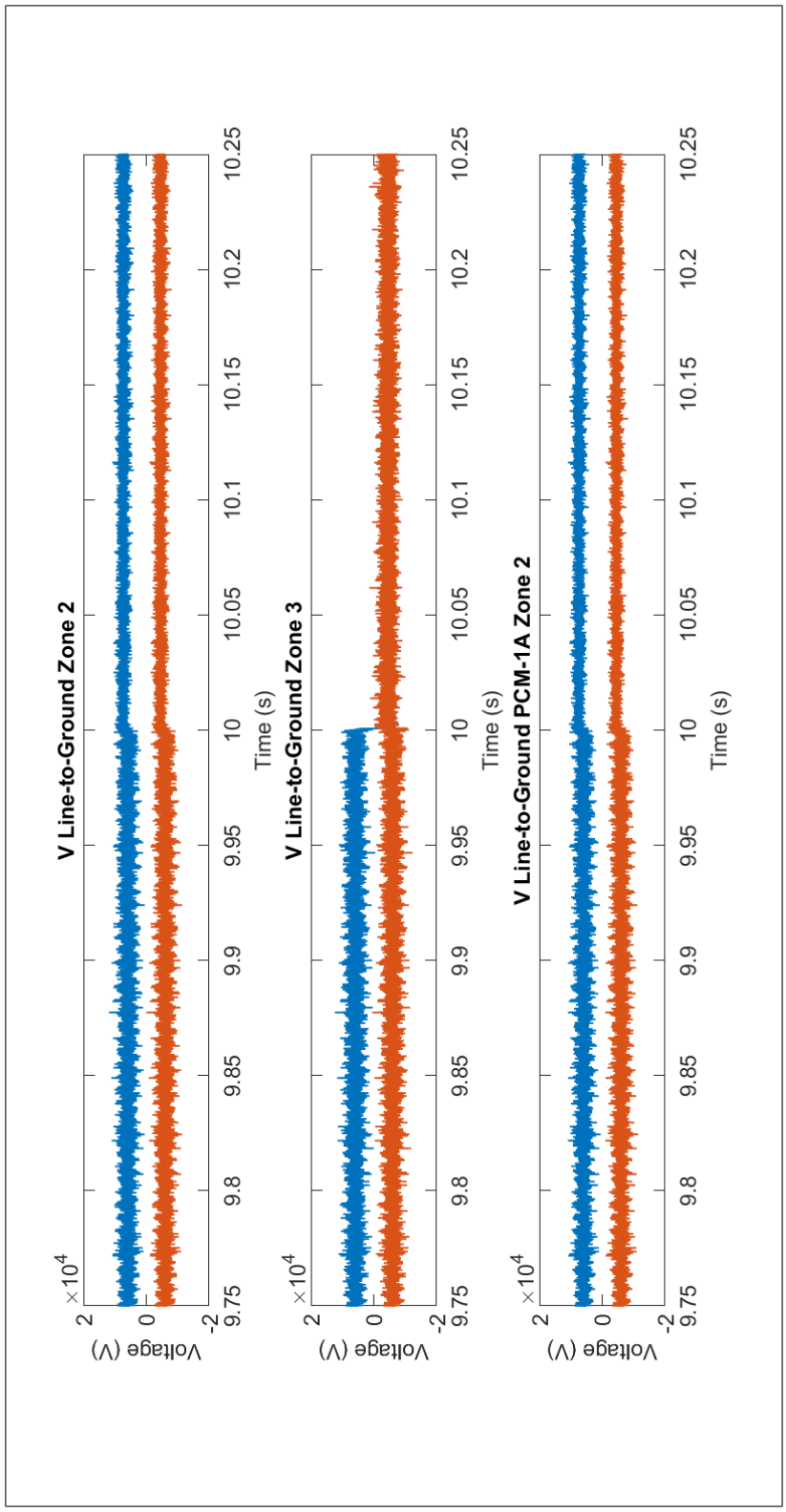

Figure 6.11: Accelerated Model Line-to-Line Fault

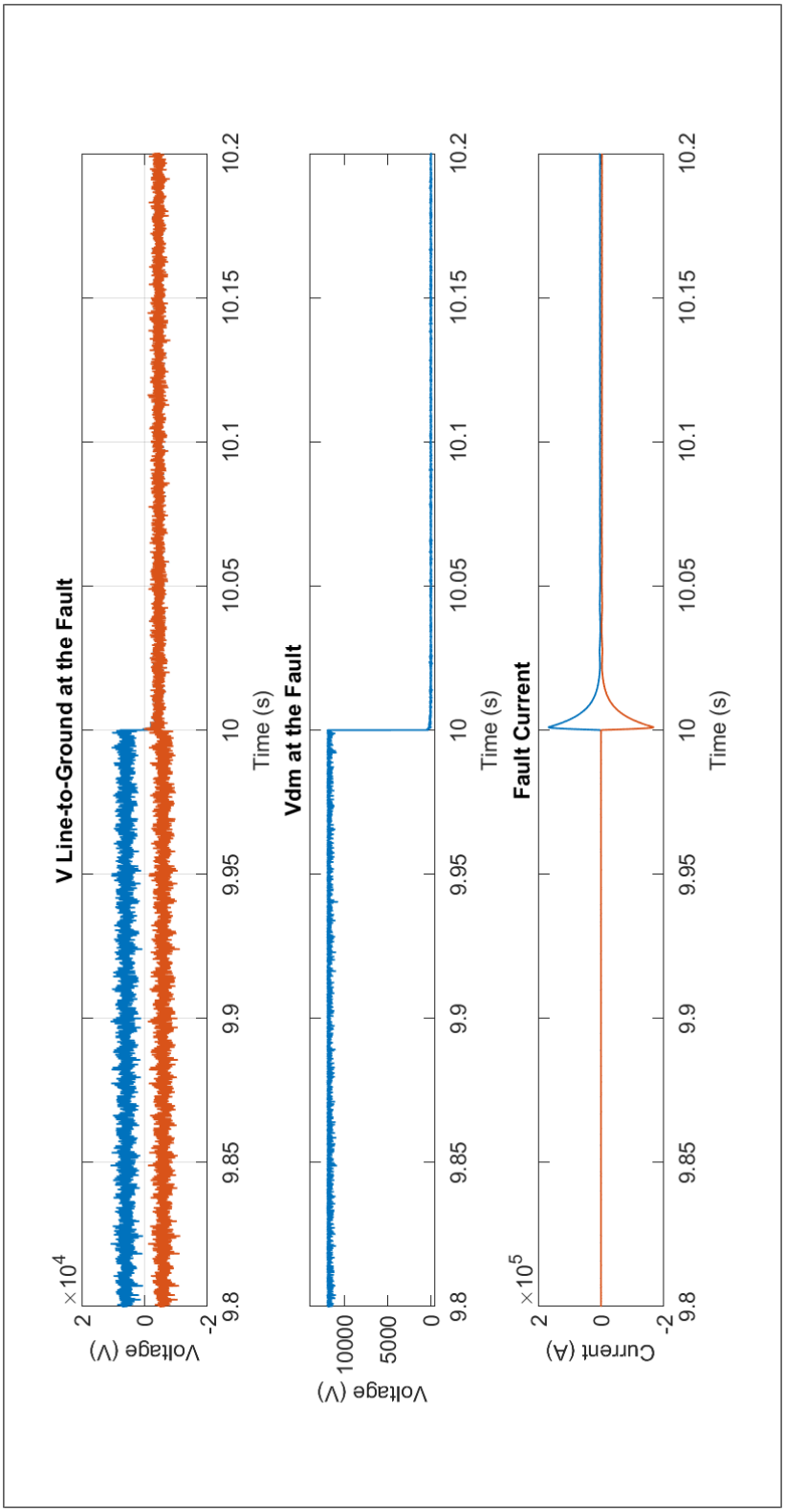

Figure 6.12: Accelerated Model Line-to-Line Fault

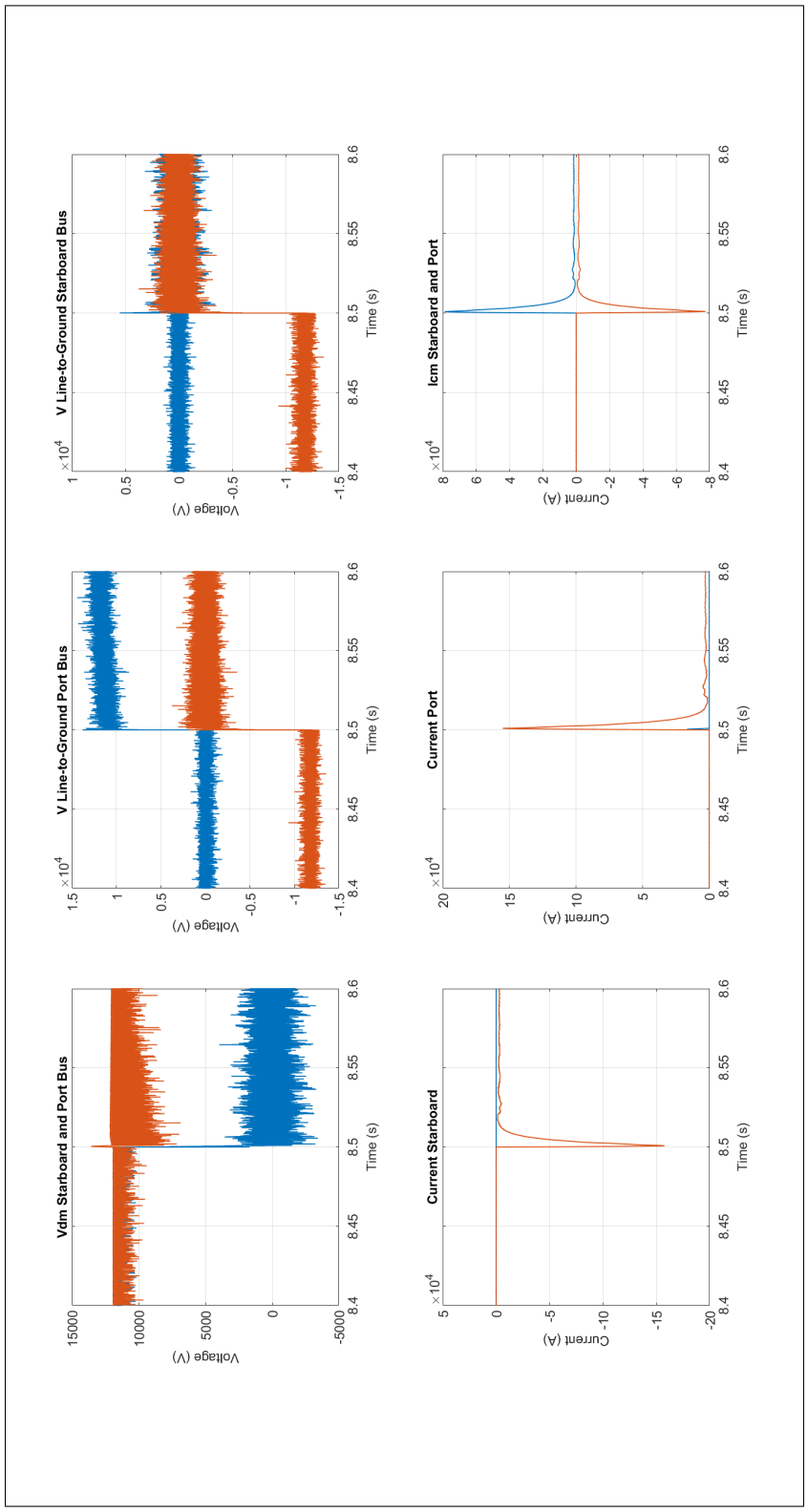

Figure 6.13: Accelerated Model PLG and NLG Fault on Two Busses

6.7 Accelerated Model Non-Unit-Based Results

Following this the logic within a PDM state machine was modified so that it would mimic a MVdc Solid State Circuit Breaker (SSCB) 6.14. It should be noted that, the circuit was modified to mimic a SSCB, a fully functional SSCB model was not added. Due to this transient behavior around isolation, especially the voltage transient experienced by the 'SSCB' itself, will not be accurate. Also, the current limiting inductor was intentionally oversized, as close form design equations were not yet derived. The Metal Oxide Varistor and other parts of the SSCB were modeled with a voltage source. This was deemed an appropriate approximation until MVdc SSCBs are further developed and realistic features can be added to the model. However, this test serves as a second proof of concept, of non-unit-based operation within the models that were built, using these particular state machines. At this point a LL fault was added as in Fig 6.8 fault 3. The modified state machine then instructs the PDM switch to open, thus isolating the fault 6.15 6.16.

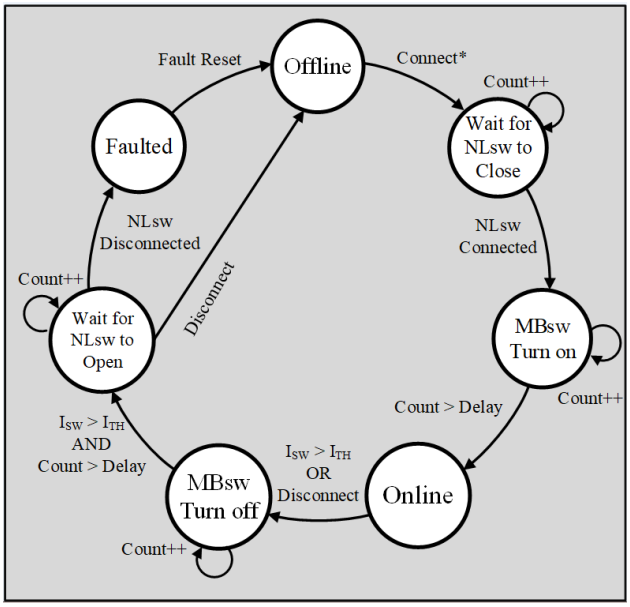

Figure 6.14: Modified State Machine for SSCB Emulation

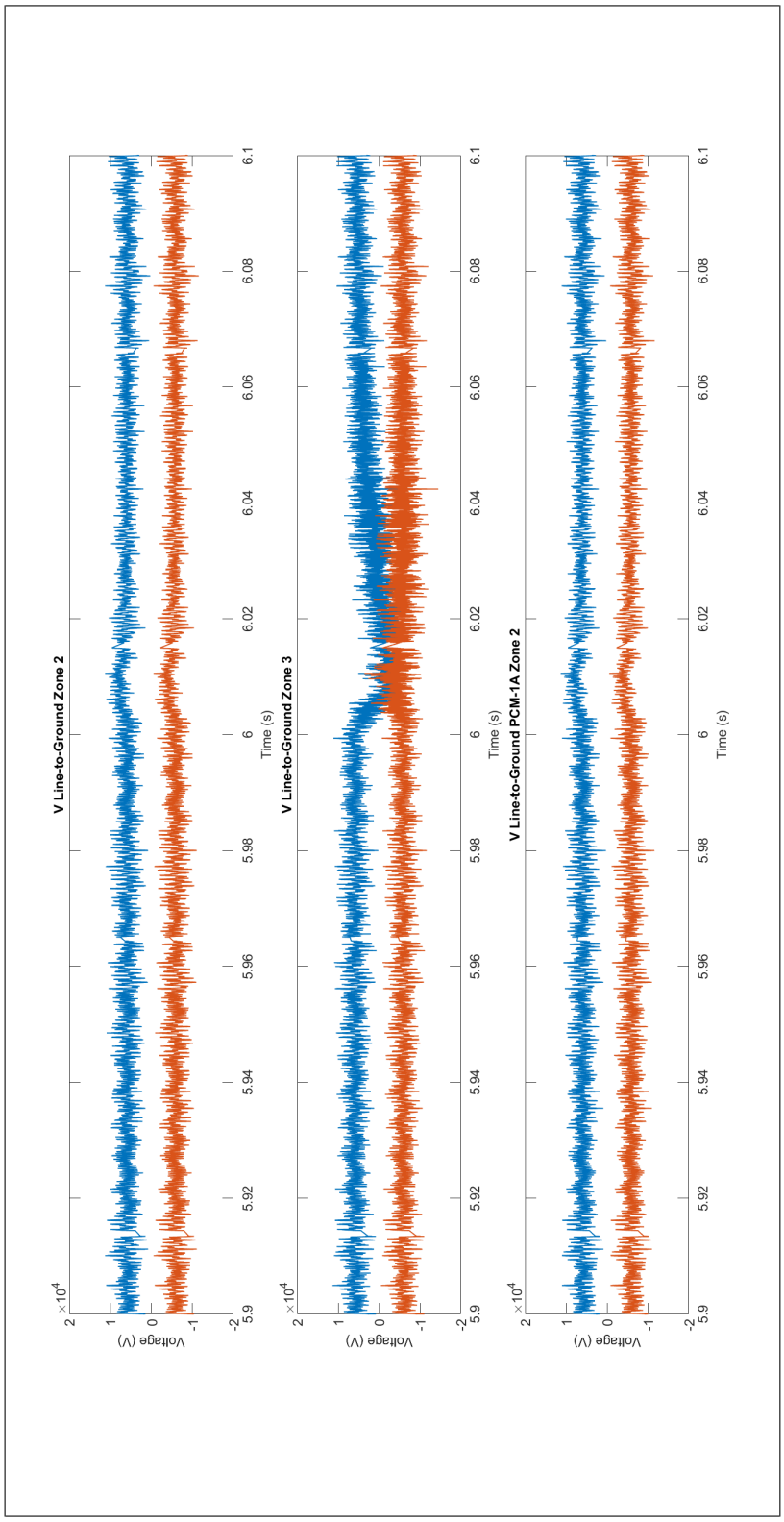

Figure 6.15: Accelerated Model Non-Unit-Based Protection Line-to-Line Fault Isolation, System Voltages

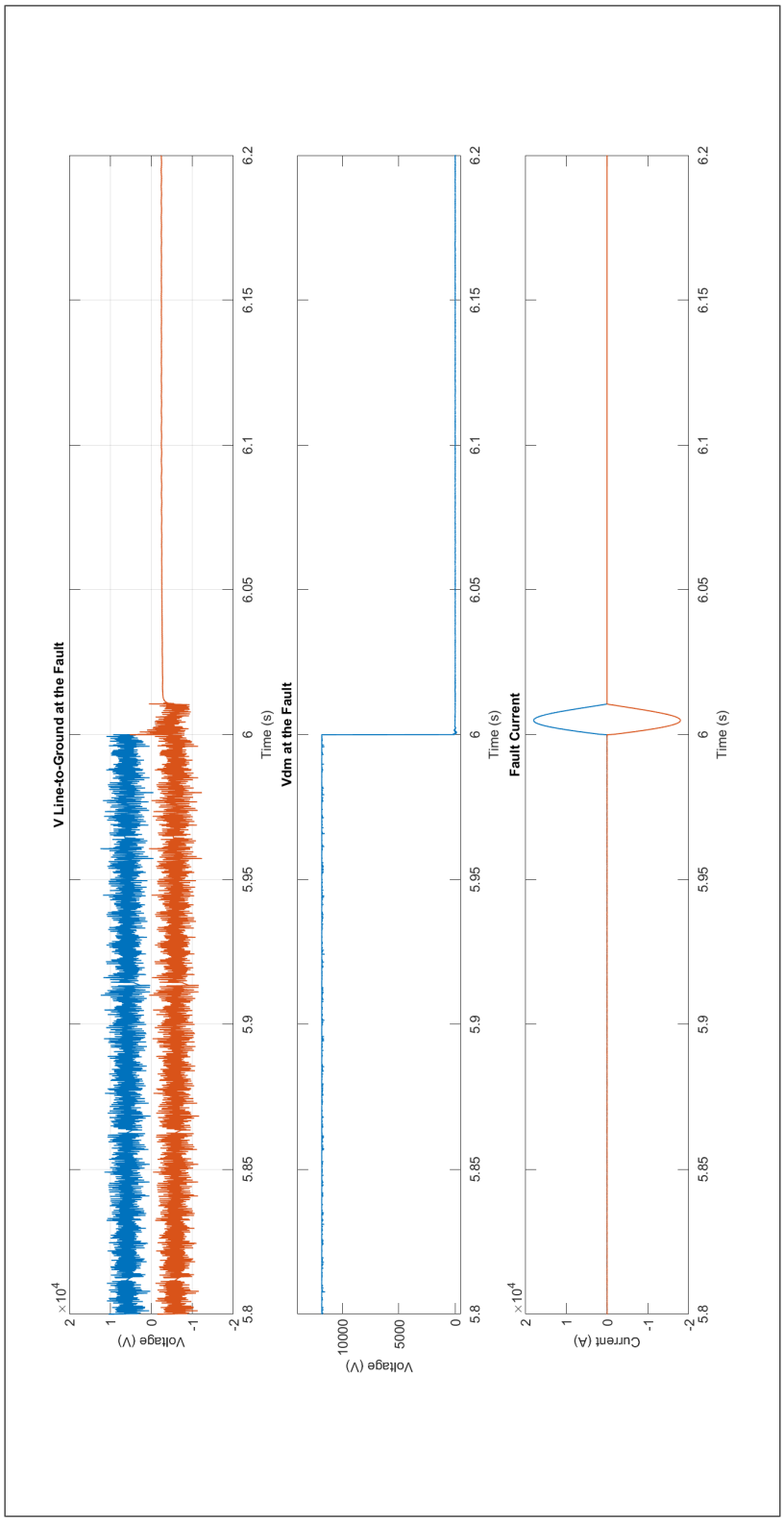

Figure 6.16: Accelerated Model Non-Unit-Based Protection Line-to-Line Fault Isolation, Current and Voltage at Fault Location

6.8 Accelerated Model Unit-Based Results

Since, the NPC1 is incapable of fully controlling its output current, and development on closed loop controls for a topology capable of doing so has not yet begun. A modified NLSw state machine, functioning as a SSCB was added to the output isolating switches of the PGMs. This makes it so that the output current can be brought to zero by opening these isolating switches. While leaving the other NLSw state machines unmodified, this modification to the PGMs, allows for the testing of unit-based protection strategies. This is also a reason to use the terms, non-unit-based vs unit-based instead of saying breaker-based. In this case the addition of one bidirectional MVdc SSCB breaker at each PGM allows for the over all strategy to be unit-based. At this point a LL fault was added as in Fig 6.8 fault 3. As seen in Fig 6.17, after the fault occurs the Breakers at the output of of the Zone 3 PGM open, prior to the bus voltage reaching zero. However, at the other side of the Zone 3 Starboard PDM measurements at the input of the PMM show the Bus crashing, and then recovering after a short time. In Fig 6.18, it can be seen, that the differential voltage at the fault crashes to zero. So what happened here? The following steps explain:

1. The fault occurs.
2. The SSCB at the output of the Zone 3 PGM detects an over current transient, and its internal state machine commands the SSCB to open. At the same time the PDM feeding the fault, has recognized that a fault has occurred but is unable to open, its state machine enters the 'waiting for zero' state.
3. The bus voltage both at the fault, and at the PMM's starboard input crash to zero.
4. With no power being supplied to the fault, the fault current reaches zero and the NLSw state machine at the PDM opens its NLSw.
5. When the PDM has finished isolating the fault, it sends a signal to the PGM informing it that isolation has occurred.
6. The PGM closes its SSCB and the bus voltage at the PMM recovers.

Known issues with this test include: If the differential mode voltage is viewed at the PMM there is actually an over voltage transient when the PGM closes its SSCB. This is due to the sudden change in voltage on the bus when the PGM reconnects at 0.75 per unit voltage. However, since dc link capacitors at all of the loads have not crashed due to the presence of auctioneering diodes. The current upon closing is not as extreme as it could have been if every load on that bus had entered pre-charge simultaneously (less than 50 Amps was observed, further observation is needed to determine what amount of this is real vs a simulation artifact) Within 0.124 s, the starboard bus is completely recovered, and the current into the PMM is back to being shared roughly equally between both buses. Additionally, like the previous Non-Unit-Based test the SSCB is modeled as a large current limiting inductor and a voltage source, the exact transient behavior of this has not been explicitly compared to a 'real' SSCB but, is considered an appropriate approximation.

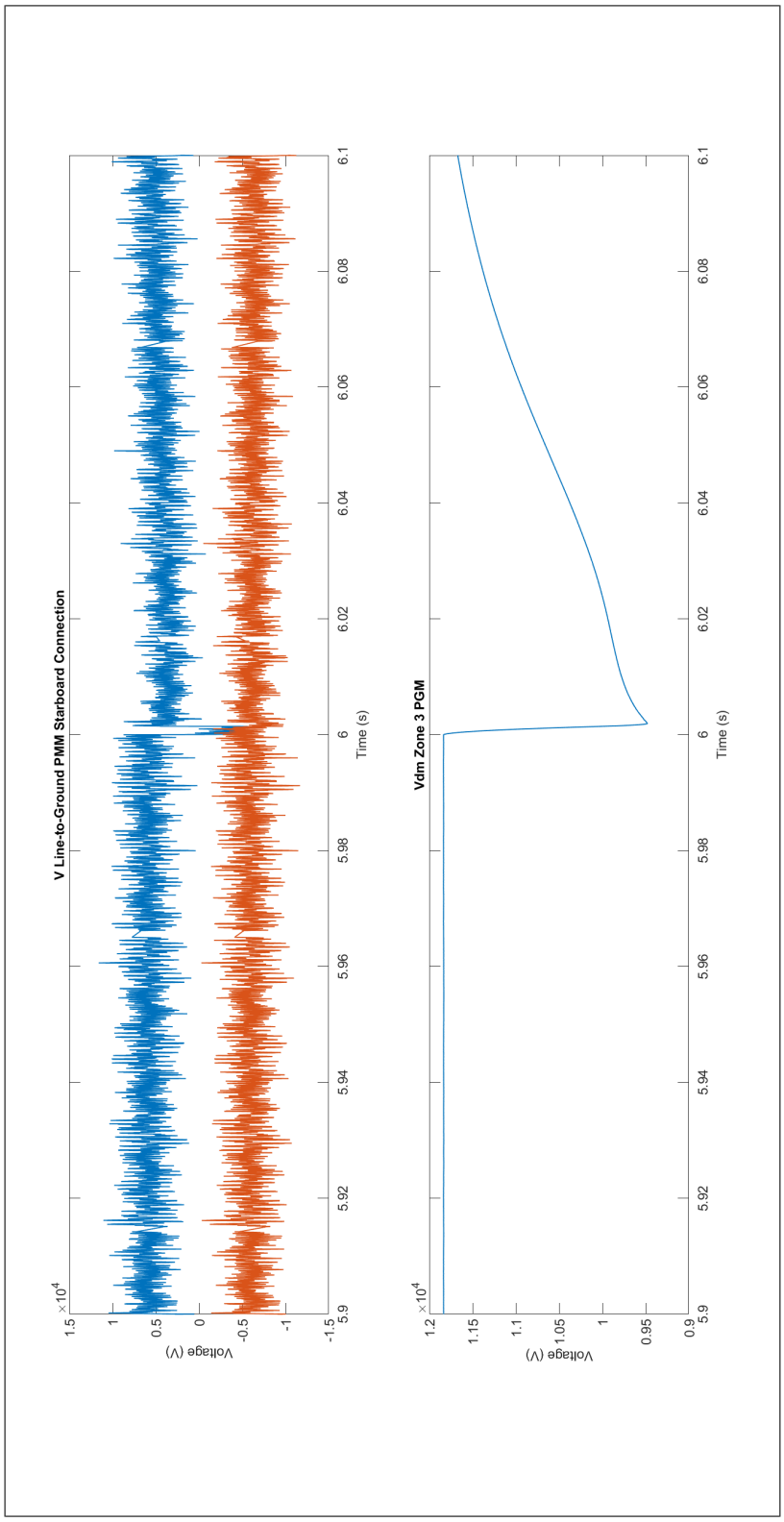

Figure 6.17: Accelerated Model Unit-Based Protection Line-to-Line Fault Isolation, PMM Input Voltage and Vdm Zone 3 PGM

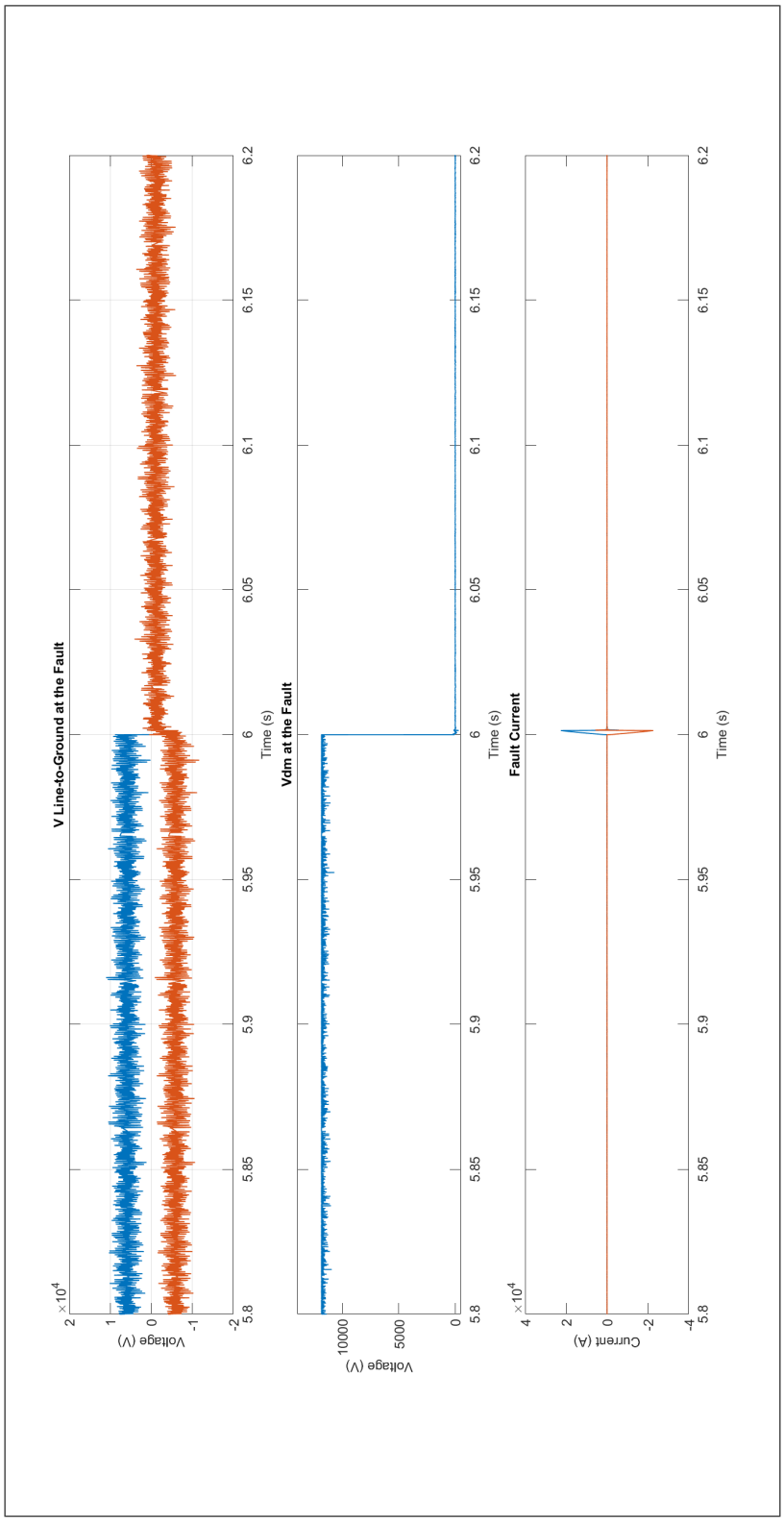

Figure 6.18: Accelerated Model Unit-Based Protection Line-to-Line Fault Isolation, Current and Voltage at Fault Location

CHAPTER 7
CONCLUSION AND RECOMMENDATIONS FOR FUTURE WORK

This work has outlined background and methodology needed to experiment on protection strategies of large floating ground systems within a real time or accelerated simulation environment. It has highlighted the need for system level state machines to enable the inter-module communication needed to test the system environments created by the various protection strategies as applied to IPES. It has laid out the foundation needed to determine the amount of energy storage required within modules in order to increase survivability. This exploration of methods has contributed to the field by creating the most detailed, largest simulation of its type, to the authors knowledge. Larger models certainly exist but, not with the set of challenges encountered such as short cable lengths, all PEC based system, and accurate line to ground behavior.

Follow on work with this model would be to simulate unit-based protection and non-unit-based protection in a variety of fault scenarios; as well as to add additional PGMs in order to get to a four-energy source model. With the intention of having two of them at a higher power level in order to simulate a system closer to 100 MW. Following this addition, this model could be used to simulate various fault isolation and recovery scenarios as well as help in making educated determinations about the amount of energy storage required in the ship given a known set of loads. For example, the amount of energy storage needed at a PCM-1A to ensure its output remains stable while the MVdc bus is reconfigured following a fault. Additionally, phenomena associated with various fault scenarios could be explored, with four energy sources in the model. There are negative aspects of adding auctioneering diodes. However, the addition of auctioneering diodes, simplifies locating faults from a system level perspective. The protective strategy needs to acknowledge this design choice and the advantages and disadvantages should be carefully described. Additional testing could be conducted to determine the behavior of PGMs when they have many paralleled output converters. A PGM with a synchronous generator capable of 10MW would require several

converters operating in parallel to handle the high current requirements of operation at that power level.

Additional future work could be the discovery of power density and efficiency, advantages and disadvantages associated with the selection of unit-based or non-unit-based protection. This future work would need to factor in not only possible protection strategies but, topology selection within those strategies and the amount of ancillary equipment needed to run the selected system as designed. Further work would be to compare the advantages and disadvantages of all 8 IPES architectures. The decisions surrounding the selection of A or B type system topologies requires further development.

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