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Health Condition Assessment of Multi-Chip IGBT Module with Magnetic Flux Density

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HEALTH STATE ASSESSMENT OF MULTI-CHIP IGBT MODULE WITH MAGNETIC FLUX DENSITY

by

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ABSTRACT

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Under the Supervision of Professor Lingfeng Wang

To achieve efficient conversion and flexible control of electronic energy, insulated gate bipolar transistor (IGBT) power modules as the dominant power semiconductor devices are increasingly applied in many areas such as electric drives, hybrid electric vehicles, railways, and renewable energy systems. It is known that IGBTs are the most vulnerable components in power converter systems. To achieve high power density and high current capability, several IGBT chips are connected in parallel as a multi-chip IGBT module, which makes the power modules less reliable due to a more complex structure. The lowered reliability of IGBT modules will not only cause safety problems but also increase operation costs due to the failure of IGBT modules. Therefore, the reliability of IGBTs is important for the overall system, especially in high power applications. To improve the reliability of IGBT modules, this thesis proposes a new health state assessment model with a more sensitive precursor parameter for multi-chip IGBT module that allows for condition-based maintenance and replacement prior to complete failure.

Accurate health condition monitoring depends on the knowledge of failure mechanism and the selection of highly sensitive failure precursor. IGBT modules normally wear out and fail due to thermal cycling and operating environment. To enhance the understanding of the failure mechanism and the external characteristic performance of multi-chip IGBT modules, an electro-

thermal finite element model (FEM) of a multi-chip IGBT module used in wind turbine converter systems was established with considerations for temperature dependence of material property, the thermal coupling effect between components, and the heat transfer process. The electro-thermal FEM accurately performed temperature distribution and the distribution electrical characteristic parameters during chip solder degradation. This study found an increased junction temperature, large change of temperature distribution, and more serious imbalanced current sharing during a single chip solder aging, thereby accelerating the aging of the whole IGBT module.

According to the change of thermal and electrical parameters with chip solder fatigue, the sensitivity of fatigue sensitive parameters (FSPs) was analyzed. The collector current of the aging chip showed the highest sensitivity with the chip solder degradation compared with the junction temperature, case temperature, and collector-emitter voltage. However, the current distribution of internal components remains inaccessible through direct measurements or visual inspection due to the package. As the relationship between the current and magnetic field has been studied and gradually applied in sensor technologies, magnetic flux density was proposed instead of collector current as a new precursor for health condition monitoring. Magnetic flux density distribution was extracted by an electro-thermal-magnetic FEM of the multi-chip IGBT module based on electromagnetic theory. Simulation results showed that magnetic flux density had even higher sensitivity than collector current with chip solder degradation. In addition, the magnetic flux density was only related with the current and was not influenced by temperature, which suggested good selectivity. Therefore, the magnetic flux density was selected as the precursor due to its better sensitivity, selectivity, and generality.

Finally, a health state assessment model based on backpropagation neural network (BPNN) was established according to the selected precursor. To localize and evaluate chip solder degradation, the health state of the IGBT module was determined by the magnetic flux density for each chip and the corresponding operating conduction current. BPNN featured good self-learning, self-adapting, robustness and generalization ability to deal with the nonlinear relationship between the four inputs and health state. Experimental results showed that the proposed model was accurate and effective. The health status of the IGBT modules was effectively recognized with an overall recognition rate of 99.8%. Therefore, the health state assessment model built in this thesis can accurately evaluate current health state of the IGBT module and support condition-based maintenance of the IGBT module.

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Chapter 1 Introduction

1.1 Motivation

As the key technology that can achieve efficient conversion and flexible control of electronic energy [1], the application of power electronics has been widely used in industrial, commercial, and residential areas [2]. With an increase of the market size of power electronics, insulated-gate bipolar transistor (IGBT) modules dominate the high voltage and current market [3, 4], as shown in Figure 1-1. Because of the excellent performance such as high power density, high switching frequency, low power loss, and cost effectiveness [5, 6], the application of IGBT power modules is increasing in many areas such as electric drives, hybrid electric vehicles, railways, and renewable energy systems [3], as presented in Figure 1-2.

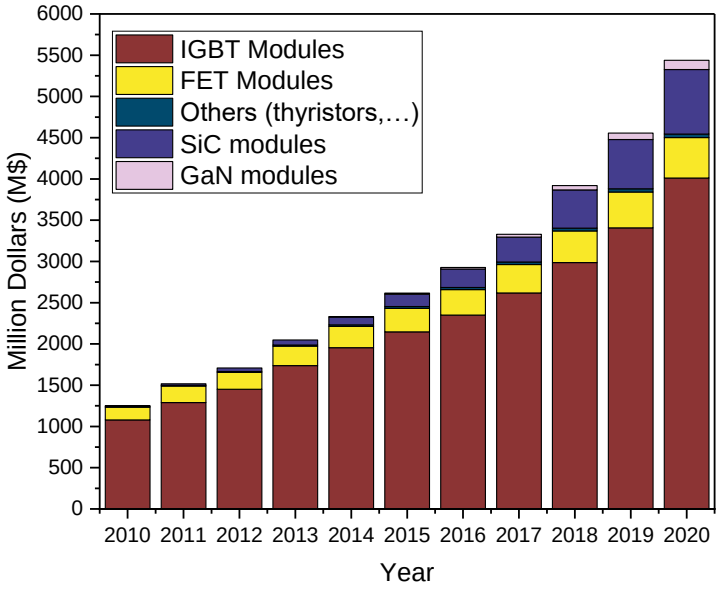


Figure 1-1 2010-2020 power modules market [4].

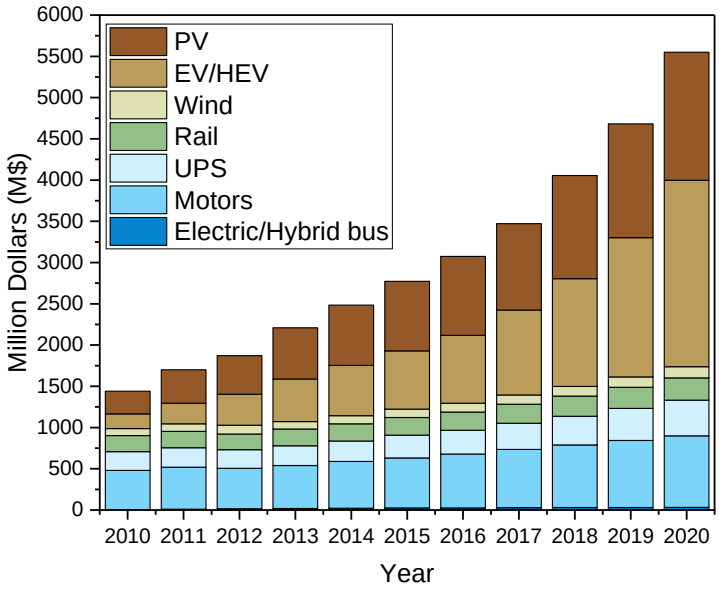


Figure 1-2 Increasing applications of IGBT power modules in many areas [3].

However, the fast growth on the application of power electronics in these areas challenges reliability of the overall systems. For instance, it is pointed out that power converters dominate the failures of wind turbines [7], and 38% faults of variable speed ac drives in industry is caused by power converters failures [8]. In addition, power semiconductor devices and solder joints account for 34% of total failures in power converter system, which indicates that power semiconductor devices are the most vulnerable components in power converter system [7, 9, 10]. Any failure of the components or the devices will lead to shutdown of the overall system. These sudden breakdowns increase maintenance and repair costs or even influence human lives. For instance, in a PV generation plant, the power electronic inverters were responsible for 37% of the unscheduled maintenance and 59% of the associated cost [10]. The increasing operating costs and unexpected disruption to services partially offsets the benefits of the application of power electronic systems.

As mentioned above, the reliability of the overall system mainly determined by the reliability of the power semiconductor devices. To satisfy the high reliability requirements of the overall

system, both safety consideration as well as limitation of the system operation cost must be considered [1, 9]. It is necessary to work in power semiconductor devices health management area, such as diagnosis, prognosis, and condition monitoring [9]. The reliability of the overall system can be greatly improved by scheduling condition-based maintenance, replacing devices before failure occurs, or taking actions including prognosis, active thermal control, and fault tolerant operation for power devices according to the condition of the power devices [1]. Therefore, accurate condition monitoring (CM) is the basic technique to achieve the improvement of reliability of the overall system. Because IGBTs are the most commonly used power semiconductor devices and there is a low satisfaction level of previous condition monitoring methods [9], it is important to investigate new condition monitoring methods for IGBT modules to improve the reliability of the overall systems.

1.2 Background

CM is a technology of measuring the real-time condition of a component to take an appropriate action before catastrophic failures occur [11, 12]. It is important to enable the condition-based maintenance and replacement and provide data for prognosis and diagnosis. The challenge of CM is finding the relationship between the known degradation based on the knowledge of failure mechanism and the measured operating characteristic parameters which requires practical techniques [12, 13]. Thus, the accuracy of condition assessment depends on the parameters that indicate device degradation and assessment methods. Failure mechanism, current precursors, and health condition assessment methods of IGBT modules are introduced in this section.

Press-pack and wire-bonded IGBT modules are two types of IGBT models classified according to packaging techniques. The connection between chips in press-packaging is achieved

by direct press-pack contact instead of bond wires [14]. Therefore, press-pack IGBT modules have better performance in terms of reliability, power density, and cooling capability [14-16]. However, the cost of press-pack IGBT modules is higher than that of wire-bonded IGBT modules. Therefore, wire-bonded power device modules are mainly used in power electronics area [17]. This thesis focusses on the condition monitoring of wire-bonded IGBT modules.

1.1.1 Failure Mechanism of IGBT Module

Failure mechanisms of power modules are generally categorized into chip-related failure mechanisms and package-related failure mechanisms. However, chip-related failure mechanisms occur due to overstress conditions without any prior warning, which is outside of the realm of CM for wear-out fatigue and result in the destruction of the module [11, 18]. Thus, the package-related failure mechanisms are more important and practical to be monitored.

There are many parameters affecting the packaged-related failure of IGBT modules and their relationships are complex, involving multiple factors such as temperature, vibration, and humidity. However, it is found that temperature is the most dominant stressor for the failure [7, 10, 17]. In addition, the packaged-related wear-out caused by thermal stress can increases the possibility of the chip-related failure [11, 18].

Under the effect of thermal stress, the failure of the IGBT module mainly occurs in the solder layer and the bonding wire because of mismatched coefficients of thermal expansion (CTEs) of adjacent materials, such as wire bond and silicon, silicon and direct bonded copper (DBC) ceramic substrate, and DBC substrate and base plate. Therefore, solder layer fatigue and bond wire lift-off are the most common failure modes of IGBT modules [5, 12, 17, 19, 20]. Power cycling or thermal cycling is generally used to study the above two failure mechanisms under experimental conditions [21].

1) Bond wire lift-off

Aluminum bonding wire is an important part to realize the function of current flowing by connecting chips, and chip and DBC. Because of the large difference in CTEs between the bond wire and the silicon chip, it bears a huge thermal stress under large temperature swings caused by the power dissipation in the chip and the ohmic self-heating of the bond wire [11]. As thermal cycling repeats, cracks propagate from the edge of joints to the center along the small grain boundaries of bond wires until bond wire lift-off occurs [22], as shown in Figure 1-3. To improve the reliability of the bonding wire connection in the industry, multiple bond wires are generally connected in parallel so that the current through other wires immediately increase after some of the wires lift-off, which accelerates lift-off of the rest bond wires [22].

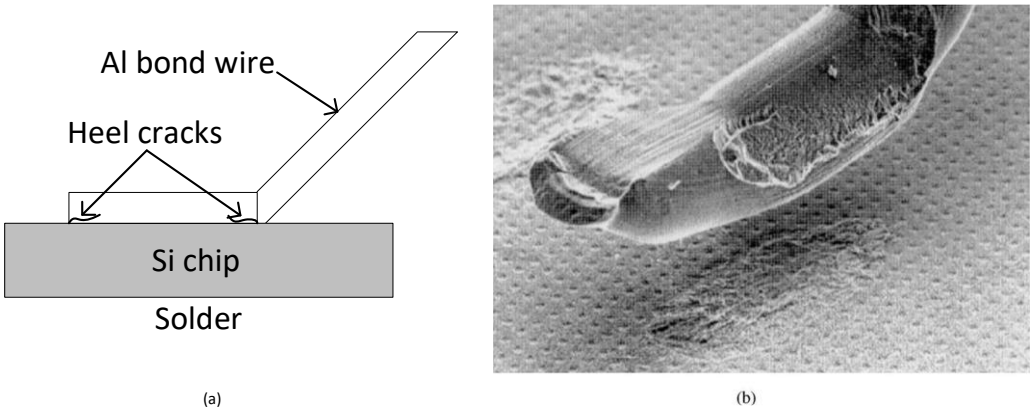


Figure 1-3 Bond wire lift-off due to crack growth. (a) Crack propagation causing bond wire lift-off. (b) SEM image of a lifted bond wire [12].

Research related with bond wire fatigue have been carried out. For example, literature [23] points out that the main failure mode of the IGBT module is bond wire fatigue when the junction temperature fluctuation (ΔT_j) is more than 100^{o}C in the power cycle experiment. Literatures [24, 25] research the influence of bond wire type and layout on the reliability of IGBT modules. Literature [26] analyzes the influence of IGBT module junction temperature fluctuation on the reliability of bond wires and proposes corresponding improvement methods. Literature [27] analyzes the influence of different bonding temperature on the bond wire reliability. In-depth

understanding of the failure mechanism of the bond wire is to accurately monitor its operating state, provide guidance for design and manufacture process, and improve the operating reliability.

2) Solder layer fatigue

The solder layer is an important heat transfer channel of IGBT modules, and its performance directly affects the reliability of IGBT modules. The device is subjected to frequent temperature fluctuations because of the frequent switching of IGBT modules. The CTE mismatches between the silicon chip and DBC substrate, the DBC substrate and baseplate with temperature variation result in shear stress in the solder layer and produce cracks, delamination and voids [28], as shown in Figure 1-4. The solder fatigue reduces the effective area for heat conduction and increase thermal resistance, which increases the junction temperature and accelerates the degradation of itself and other failure modes such as bond wire fatigue [23, 28-31]. The corner is especially subject to large thermal stress, and cracks generally initiate here, and then gradually develop to the center of the solder layer ultimately leading to the failure [5, 32-34].

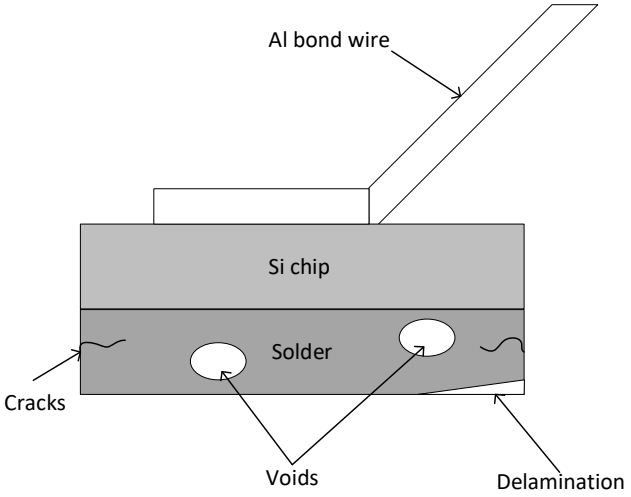


Figure 1-4 Cracking and void formation in solder layer [12].

At present, a lot of researches have been conducted on the fatigue failure mechanism of the solder layer, mainly focusing on thermal parameters and stress analysis. Research [35] indicated that the degradation occurs first on the solders at high temperature level with the same temperature fluctuation. Study in [35, 36] showed that the reliability of the solder can be developed by new solder materials, such as Sn-Ag-Cu. Literatures [23, 34] based on the aging experiments under different ΔT_j found that the main failure mechanism is solder fatigue when ΔT_j is small, and the bonding wire fatigues before the solder layer fatigue and then becomes the main failure mode when ΔT_j is large. Literatures [37, 38] indicated that the most critical solder fatigue occurs in baseplate solder for passive thermal cycling, especially in the case of copper base plates because of the worst mismatch in the CTEs and the maximum temperature swing combined with the largest lateral dimensions, but chip solder fatigue determines the lifetime of the module for active power cycling.

1.1.2 Precursors for IGBT Condition Monitoring

The external characteristics of the IGBT module is generally affected by the degradation. For instance, the junction temperature (T_j), and thermal resistance (R_{th})of the device increase, and on-state collector-emitter voltage ($V_{ce,on}$) changes when solder or bond wire fatigues [1, 11, 12]. A number of IGBT health monitoring methods exist which are mainly based on the change of the electrical characteristic parameters and the temperature characteristic parameters, summarized in Table 1-1.

Table 1-1 Existing failure precursors for health condition monitoring.

Degradation monitored	Precursor
Bond wire lift-off	On-state collector-emitter voltage ($V_{CE,on}$) [39-44] Gate-emitter voltage (V_{GE}) [45]

Die-attach fatigue	$V_{CE,on}$ [39] Collector current change rate (dI_C/dt) [46] Temperature gradient (∇T) [47]
Baseplate solder fatigue	$V_{CE,on}$ [39] Case-above-ambient temperature (T_{ca}) [48] Thermal resistance (R_{th}) [49]
Junction temperature	$V_{CE,on}$[50-52] $V_{GE(th)}$ [53, 54] dI_C/dt [55, 56] Transconductance (G_M) [56] collector voltage slope (dV/dt) [57] Turn-off delay (t_{off}) [51, 55] Turn-on delay (t_{on}) [55] Power loss [58] Thermal model [59, 60]

A failure precursor is an indicative parameter of an impending failure [61]. From Table 1-1, it can be found that all those precursors are related to temperature. According to failure mechanism analysis, junction temperature and thermal resistance are the two parameters that directly reflect the degradation of the module. However, direct measurement of junction temperature and internal temperature distribution in the module is impractical because most sensing devices are eventually damaged by excessive junction temperature, intrusive measurement has effect on the characteristics of the module, and contactless measurement is costly [12, 61]. In addition, a great error can be caused by the position of the sensor. The external temperature like case temperature is easily measured, but the difficulty lies in understanding the electrothermal interaction, and the masking effects of a variable working condition and other mechanisms of degradation, such as bond wire lift-off [12]. The accuracy of the evaluation method based on power loss and thermal

model is strongly dependent on the measurement accuracy of instantaneous power losses and the correct identification of the thermal network. However, the thermal network also relies on aging effects and is nonlinear at high temperature [62]. Therefore, fast and cheap junction temperature estimation methods and health state monitoring methods based on temperature sensitive electrical parameters (TSEPs) and fatigue sensitive parameters (FSPs) get more attention to estimate junction temperature or the condition of the power module.

In Table 1-1, $V_{CE,on}$ is the most widely used TSEPs. However, the measurement of $V_{CE,on}$ is difficult with extremely high requirement for measurements accuracy because of small variation, strictly control of temperature and current to keep the same operating points, and insertion of measurement devices which needs high voltage isolation [12, 46]. The gate signals are low-voltage quantities and sensitive for degradation, but they interrupt the IGBT's normal switching operations since the measurement requires external signal injection to the gate [12, 13, 46, 62, 63]. For switch time, the duration is very short [12]. For collector current, it still needs to work on nonintrusive and contactless measurement. Thus, the limitations of existing techniques largely prevent the wide application of CM for power electronics reliability. It still needs efforts oriented to improve the sensitivity and to reduce the cost of CM.

1.1.3 Health Condition Assessment Methods

Generally, existing condition assessment methods can be categorized into two sets: model-based method and data-driven method [5]. The model-based method establishes physics of failure (PoF) model with the consideration for actual operating point and external load missions during the life cycle, and an understanding of their effect on failure mechanism [64, 65]. Both reliability prediction and lifetime prediction can be ideally done based on physics-of-failure analysis [1]. However, the PoF model is computationally costly for building relationships between different

factors. In contrast, data-driven methods take advantage of the information from available measurements without prior knowledge of the failure mechanisms by statistical and probabilistic analysis [61]. Data-driven methods are computationally efficient for a complex multivariate system with different failure mechanisms [5].

There are increased researches combining the two methods in IGBT health condition assessment. Literature [66] accurately predicted the on-state resistance of the IGBT with DC link voltage and output voltage ripple based on three kinds of artificial neural network (ANN) structure. Study in [67] proposed a multiclassification fusion system leverages the strengths provided by Backpropagation Neural Networks (BPNNs), Support Vector Machine (SVM), Deep Belief Networks (DBNs), Self-organizing Maps (SOMs), and Mahalanobis Distance (MD) to form a robust classification model of IGBT health condition after identifying health parameters as inputs and dividing different health state as outputs. Paper [68] solved the complex nonlinear relationship between the electrical parameters and the junction temperature of the IGBT module from the BPNN point of view. A health condition evaluation method based on multivariable IGBT bond wire aging parameters was proposed using ANN with only 2.47% average error, which was more accurate than the univariate evaluation [69].

1.3 Research Gap

Multi-chip IGBT power modules are designed for large current ratings with a number of chips connected in parallel. The physical structure of the multi-chip IGBT modules are more complex than the IGBT modules with only one or two chips, which results in the increased complexity in the physics of failure as well as their characteristic formation owing to the uneven lay-out of power semiconductor chips combined with the heterogeneous construction of power modules [6], such

as thermal coupling effect [70] and imbalanced current sharing [71]. Researches have been carried out in current distribution [72, 73], temperature distribution [74], bond wires degradation [6], and baseplate degradation [75] of the multi-chip IGBT modules, but the failure mechanisms and the change of external characteristics of the modules caused by wear-out is not clear till now, especially for chip solder fatigue. Chip solder fatigue cannot be ignored for lower temperature swings at active power cycling, and it even appears earlier than the bond wire degradation.

In addition, the existing techniques in Table 1-1 are mainly applied to IGBT modules with only one or two chips. It is more challenging to achieve health condition monitoring when there are more IGBT chips in parallel in multi-chip IGBT power modules. The parallel structure can accelerate chip failure and the failure signature of the chip can be concealed [6]. Hence, the investigation of new method for multi-chip IGBT power modules health condition assessment, and the failure mechanisms and change of external characteristics caused by chip solder fatigue have been identified as a research gap in this thesis.

1.4 Research Methodology

The main objective of this research is the development of a novel online health state evaluation method for multi-chip IGBT power modules. It is common to have parallel IGBT chips with anti-parallel diode chips within the power module. This research focusses on the health condition of the IGBT chips and ignores the effect of the diode chips because IGBT chips are more susceptible to failures compared with diode chips. IGBT chips experience higher thermal stress compared with diodes due to higher turn-on and turn-off power dissipation, and IGBT chips own a more complex semiconductor structure compared with diodes which makes IGBT chips less reliable [6]. Because of the package, the internal component degradation is hard to notice until the IGBT module ceases

to function. Therefore, health condition monitoring is necessary for multi-chip IGBT power modules.

Because CM relies on the knowledge of failure mechanism and selection of failure precursor, to enhance understanding of the failure mechanism and external characteristic performance of single chip solder degradation, an electrical-thermal finite element model of Infineon FF450R17ME4 was established in COMSOL. The 3D Multiphysics FEM can generate more accurate thermal and electrical characteristic performance with considerations of temperature dependence of material property, thermal coupling effect between components, and heat transfer process. The validity of the model is verified by calibrating the output characteristic curve and transient thermal impedance curve from datasheet as well as comparing the temperature distribution with the measurement results of the experiment in other paper. Based on the simulation model with high accuracy, on-state distribution of thermal and electrical characteristic parameters under different chip solder degradation is performed, and the failure mechanism of the multi-chip IGBT module under single chip solder degradation is analyzed.

According to the change of thermal and electrical parameters with chip solder fatigue, the sensitivity of FSPs is analyzed and compared, and collector current I_c of the aging chip shows highest sensitivity. However, the internal components are inaccessible for direct measurements or visual inspection due to the package. Because the relationship between the current and magnetic field has been dug up and gradually applied in current measurement [73], magnetic flux density is proposed instead of I_c as a new precursor for health condition monitoring. An electro-thermal-magnetic finite element model of the multi-chip IGBT module is built by adding an air layer above the original model to extract magnetic flux density distribution under different chip solder degradation. The magnetic flux density distribution only depends on the current distribution. The

magnetic flux density has even higher sensitivity than $I_{c.}$ new precursor is verified. Therefore, the magnetic flex density is selected as the precursor due to better sensitivity, selectivity, and generality.

Finally, a health state assessment model based on BPNN is established. To localize and evaluate chip solder degradation, the health state of the IGBT module is determined by the magnetic flux density for each chip and the corresponding operating conduction current. Because the relationship between the health state and the four inputs is nonlinear, data-drive method instead of model-based method is more suitable for health state assessment model. Furthermore, BPNN is the most common type of supervised ANN which is normally used in pattern recognition and multi-class classification for its strong nonlinear processing ability and good self-learning, self-adapting, robustness and generalization ability. The trained model is tested by test set of samples, which shows high accuracy in health state evaluation.

1.5 Contribution to Knowledge

The main outcome of this research is the implementation of a new precursor on multi-chip parallel IGBT module health state assessment. Consequently, this research has made the following contributions:

- New failure precursor for IGBT power modules.
- New discovery of the correlation between external characteristic parameters and chip solder fatigue in the multi-chip parallel IGBT modules.
- New IGBT health state assessment model based on magnetic flux density.

1.6 Thesis Organization

An electro-thermal finite element model of a multi-chip parallel IGBT power modules is built in Chapter 2, which is validated to analyze the change of external characteristic parameters of the module during the chip solder degradation. Chapter 3 analyzes the electrical parameters and thermal parameters which is widely used as precursor for condition monitoring. In addition, magnetic flux density is proposed as a new precursor, and it shows higher relative sensitivity and better selectivity and generality. Chapter 4 proposes a health state assessment model based on backpropagation neural network with the new precursor. Finally, Chapter 5 concludes the thesis.

Chapter 2 Multiphysics Finite Element Modeling of IGBT Module

As an important part of converter, IGBT module is key part of power electronic system to work as essential energy conversion technique in many areas such as renewable energy generation, electric vehicle, and aerospace. The working condition often includes stringent stressors such as moisture, vibration, high voltage, and high temperature. Because of the adverse operation circumstances and the frequent change of output power, the IGBT module can experience large temperature fluctuation during the actual operation.

However, due to a multi-layer structure and the mismatch of the coefficient of thermal expansion (CTE) of materials of different structures, a large thermal stress can be created by temperature cycle on the material surface, which causes the fatigue of the solder layer of IGBT modules or the aging of the bonding wires. The aging of the module can further influence the temperature distribution of the module. The failure rate can accelerate when the operating temperature increases [76]. In addition, temperature sensitive electrical parameters (TSEPs), like turn-off time, turn-on time, collector-emitter saturation voltage, and current distribution are also changed when temperature distribution is changed. Therefore, temperature is an important factor which limits the reliability of the IGBT module.

As the demand for high power density devices continues to grow in the industrial field, it is necessary to carry out accurate electro-thermal modeling of the power module to save maintain cost and development time caused by over design or under design and improve the reliability when the design cycle starts [77]. In previous studies, electrical and thermal characteristics have been analyzed using analytical method in isolated electrical and thermal domain for individual component [78-81]. However, modeling the module in electrical and thermal field separately cannot accurately capture the temperature effect on the electrical characteristics, like power loss.

In [82-86], these researches have extracted electrical equivalent thermal network as electro-thermal model of the power module based on the manufacture or experiment data, but component interaction such as thermal coupling phenomena has been ignored.

To solve these difficulties, physics-based modeling is extracted with the consideration of the physical structural, material properties and the environment parameters, which can clearly observe the component interaction in electro-thermal domain. However, the analytical approach to analyze electro-thermal problems is not suitable for 2D or 3D structures because of complex geometry and boundary conditions [87]. Numerical approaches such as finite element analysis (FEA) are applied in the modeling [78, 88-92]. This model built with FEA is called finite element model (FEM). The electro-thermal FEM can be used to solve coupling relationship between electrical domain and thermal domain and obtain the component interaction, which can give more accurate results. Therefore, electro-thermal FEM is built in this thesis for reliability analysis.

In this chapter, the electric-thermal FEM of a parallel multi-chip IGBT module is established with the consideration of the temperature dependence of the chip material, and the validation of the model is verified according to the datasheet and results of the experiment. By establishing the accurate multi-physical field coupling FEM, it is helpful to study thermal and electrical characteristics of the device and provide the accurate simulation to support analyzing precursor parameters of degradation and evaluating the health state of IGBT module.

2.1 Electro-thermal Coupling Theory of Finite Element Model

2.1.1 IGBT Module Packaging

Press-pack and plastic case are two common IGBT packaging types. For plastic case packaging, there are bond wires and solder to realize electrical connection. Unlike plastic case,

press-packs use surface contact by clamping force instead of bond wires for improved reliability [14]. This research focuses on the plastic packaged IGBT power modules as they are the main packaging style for high-voltage and high-power-density application because of low manufacturing costs and easy installation.

Figure 2-1 illustrates a simplified diagram of a common high-power-density IGBT module, in which IGBT chips and freewheel diode (FWD) chips are placed in anti-parallel on the direct bond copper (DBC) layer. All the chips are soldered to the copper layers through the solder layers, while the ceramic layers serve mainly as electrical insulation. The DBC layers is also soldered to the copper baseplate through the solder layers. There are bond wires between chip and chip, or chip and copper, or copper and copper to achieve electrical conduction. To get better heat dissipation effect, IGBT modules are usually placed on the heat sink by thermal grease. The common cooling methods include water cooling and air cooling.

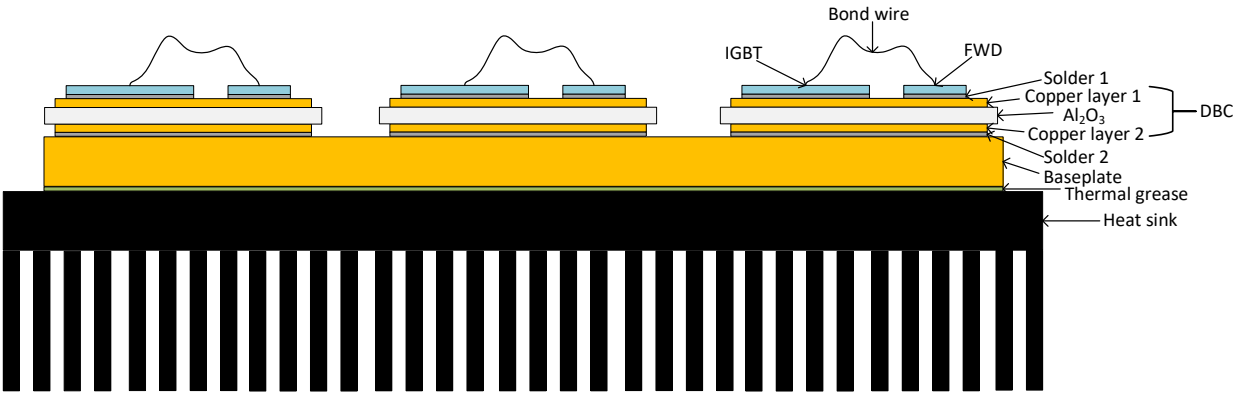


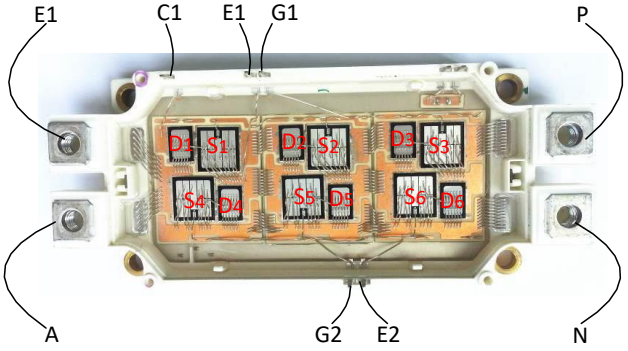
Figure 2-1 The multilayer structure diagram of the IGBT power module.

The model studied in this research is Infineon FF450R17ME4, and its configuration, inner structure, and equivalent circuit topology are demonstrated in Figure 2-2. This kind of power module is commonly applied in motor drives, servo drives, ups system, wind turbines, etc. As indicated in Figure 2-2(c), it is a half-bridge (phase-leg) power module, in which each leg comprises of three IGBTs with anti-parallel freewheel diodes (FWDs) in parallel. This parallel

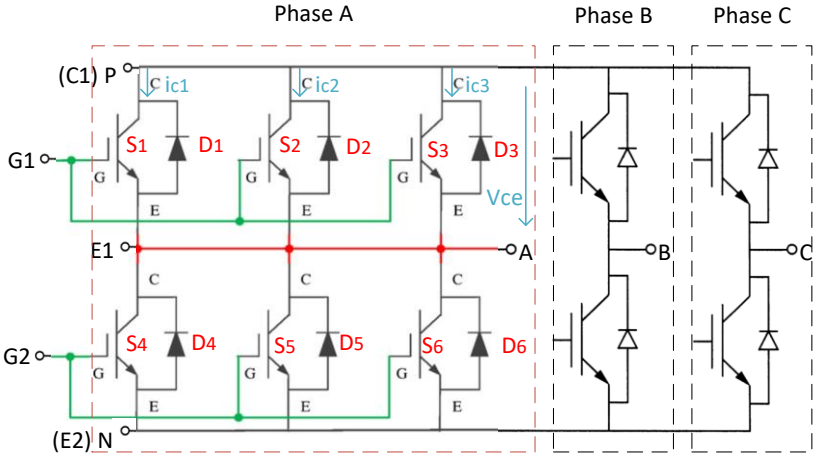
structure helps the module to achieve high current specification. S_1 to S_3 are the parallel IGBT chips, and D_1 to D_3 are the anti-parallel FWD chips. They form the upper leg. In the lower leg, S_4 to S_6 are the parallel IGBT chips, and D_4 to D_6 are the anti-parallel FWD chips. The upper leg and the lower leg are in series. G, E and C represent gate terminals, emitter terminals, and collector terminals, respectively. P and N are signs for positive terminal and negative terminal in the power loop. i_{c1} to i_{c3} are collector currents of parallel chips, and V_{CE} is collector-emitter voltage.

The chips and bond wires in the module are main part to generate heat due to power dissipation in the switching and conduction states [93], and the temperature will be fluctuating during the operating process. Under the action of alternating temperature, thermal stress will be generated, which will cause failures, such as bonding wire lift-off and solder joint cracking [14, 94].

(a)



(b)



(c)

Figure 2-2 Schematic diagram of studied multichip power module. (a) Configuration, (b) Inner structure, (c) Topology.

2.1.2 Mathematical Model of Multi-physical Field Coupling

When IGBT module is in the operating condition, the power dissipation due to current and voltage in electrical filed is the heat source in the thermal field, which causes non-uniform temperature distribution in the IGBT module. Some material properties are temperature dependent, like the electrical resistivity. Therefore, the current and voltage in electrical filed can be affected by the change of temperature. Due to the coupling relationship, to obtain the temperature distribution accurately, the electro-thermal coupling effect must be considered. The interaction among the electrical field and thermal field in the IGBT module is expressed in Figure 2-3.

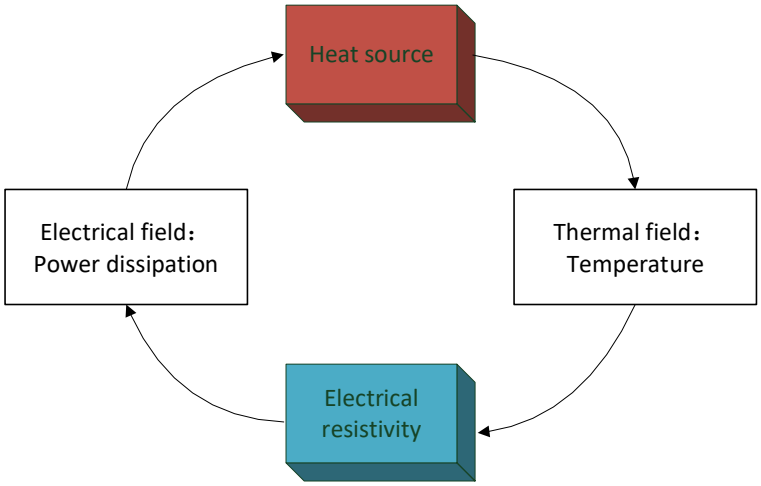


Figure 2-3 Coupling relationship between electrical field and thermal field.

As shown in Figure 2-2 (c), the external electrical circuit is connected to the collector terminals and emitter terminals of IGBT module during actual operation. When the chip is turned on, the temperature of the module rises because of power loss. The heating area of the module is concentrated above the DBC ceramic layer. The change of temperature makes the electrical characteristics of materials of the module change, which can change the current distribution of the module, and then affect the temperature distribution of the whole device. Therefore, the entire

transient temperature change process of the IGBT module is an electro-thermal coupling dynamic equilibrium process.

There are several differential equations to describe the coupling dynamic equilibrium process in the finite element model. When there is a boundary current source, the expression equation of current in IGBT module is [47]:

$$\nabla \cdot J = \nabla \cdot \gamma(-\nabla\varphi) = Q_j \tag{1}$$

where J and γ are the current density and electrical conductivity, respectively. Q_j is the boundary current source.

The chips become main heat sources when they are on-state since there is power dissipation. The amount of power per unit volume, also called power density, can be calculated from the results of the current calculation [95]:

$$Q_v = \frac{1}{\gamma} |J|^2 \tag{2}$$

where Q_v is the power density.

Some material properties of the layers of the IGBT module temperature dependent, especially for electrical resistivity of the chips. In the linear region of output characteristic curve of the IGBT, the resistivity is approximately linear with the temperature [47], as presented in formula (3).

$$\sigma = a \cdot T_j + b \tag{3}$$

where T_j is junction temperature, a and b are constant.

According to the theory of heat transfer, if the effect of heat source in is considered, the heat transfer equation is [47]:

$$\nabla \cdot (k\nabla T) + Q_v = \rho c \frac{\partial T}{\partial t} \tag{4}$$

where k is the thermal conductivity, T is the temperature, ρ is the density of the object, c is the specific heat capacity, and t is the time.

The above heat transfer equation is mainly applicable to the main heating region, like the chips. For the non-heat source region such as ceramic layer and baseplate layer, the heat conduction equation is as expressed in formula (5).

$$\nabla \cdot (k\nabla T) = \rho c \frac{\partial T}{\partial t} \tag{5}$$

The electro-thermal coupling effect affects not only the calculation of power loss, but also the accurate description of thermal conductivity characteristics. Therefore, the consideration of electro-thermal coupling effect is the precondition of obtaining accurate temperature distribution of IGBT module.

2.1.3 Transient Solving Process of Multiphysics Finite Element Model

According to the mathematical analysis of electrical-thermal coupling effect, The heat generated in the electrical field is used as the heat source in the thermal field, and the temperature becomes a feedback to the electrical field by the formula (3) until the equilibrium is reached. It is necessary to solve the coupling process in order when the finite element simulation is used to solve the multi-physical field coupling model of IGBT module, as indicated in Figure 2-4.

For the transient state simulation, the outer layer of the solving process is the time iteration, and the inner layer is the convergence iteration of the multi-physical field within each time step. The detailed steps are as follows:

1) Before numerical analysis, the physical model is built according to the actual size of the IGBT module, and initial material property parameters including temperature-dependent parameters of some materials need to be set in multi-physical field. Boundary conditions

in each field also need to be set accurately according to actual operation condition and work principle of the IGBT module.

2) The finite element model needs to be divided into multi-level mesh to improve the computational accuracy.
3) According to the actual operating current load condition and boundary conditions of electrical field, current and voltage distribution are obtained. The power density calculated in the electrical field is loaded as the heat source in the thermal field. Temperature distribution is obtained by combining the heat source, the heat dissipation condition, and boundary conditions of thermal field.
4) Convergence condition needs to be satisfied to end the iteration. If the difference between the results of the last two adjacent calculations do not meet the requirements of accuracy, the number of iterations will be increased and some initial parameters, like conductivity parameters, will be updated in the beginning of new iteration according to the last calculated results. The distribution of electrical and thermal characteristics of the IGBT module can be updated by increasing the iteration times until the calculation accuracy is satisfied.
5) Calculation time is set to end the whole calculation at a specific time. If it has not reached the set time, the time step is increase and step 3)~4) are repeated until the calculation is completed. At the end of simulation, the results of simulation can be viewed or processed.

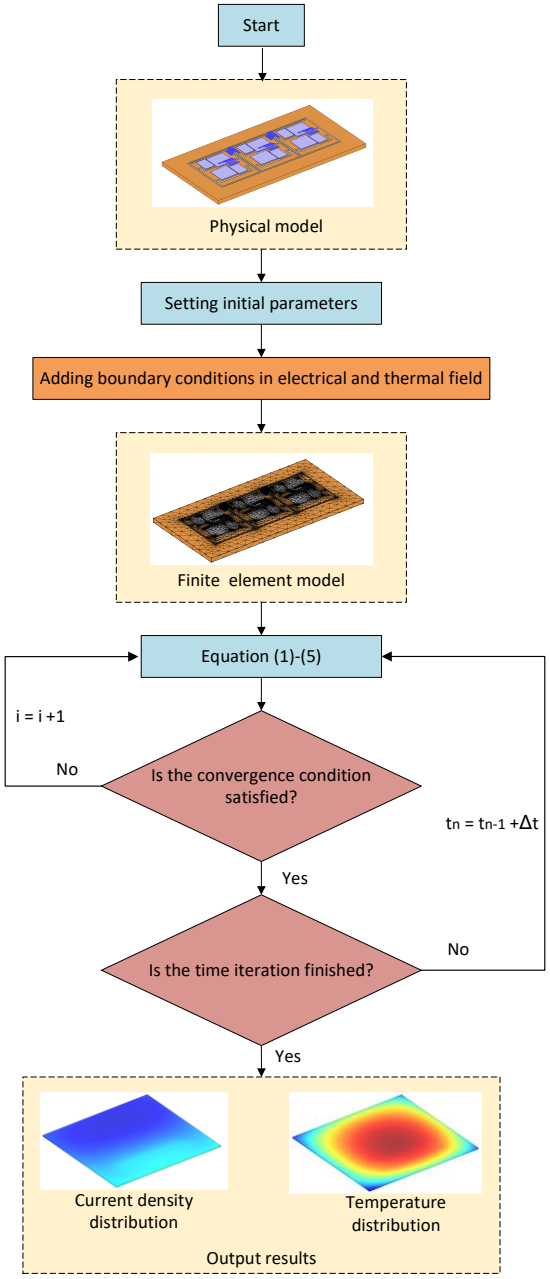


Figure 2-4 The flowchart of calculation of electrical-thermal coupling model.

2.2 Electro-thermal Finite Element Modeling of IGBT Module

2.2.1 Setting Material Property Parameters

Some important parameters of Infineon FF450R17ME4 is shown in Table 2-1. The physical parameters of some materials in IGBT modules change with temperature, so the temperature

characteristics must be considered. In the model, the electrical resistivity of silicon chips is assumed to change with temperature, while that of other materials is constant. This research focusses on the health condition of the IGBT chips and ignores the effect of the diode chips because IGBT chips are more susceptible to failures compared with diode chips. IGBT chips experience higher thermal stress compared with diodes due to higher turn-on and turn-off power, and IGBT chips own a more complex semiconductor structure compared with diodes which makes IGBT chip less reliable [6].

Table 2-1 Parameters of the IGBT module.

parameters	values
Rated voltage, V_{CES}	1700V
Rated collector current, $I_{C\,nom}$	450A
Thermal resistance (junction to case), R_{thJC}	0.06 K/W
Temperature under switching conditions, $T_{vj\,op}$	-40°C~150°C

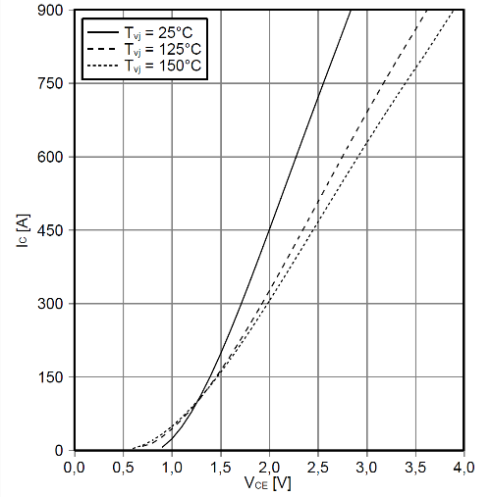


Figure 2-5 The output characteristic curve of the IGBT chip.

Figure 2-5 displays the typical output characteristic curve of the IGBT chip when the turn-on gate voltage is 15V. 15V is the optimal gate voltage to keep the on-state collector-emitter voltage drop V_{CE} at a low value and cause less electrical stress in the dielectric region at the same time [96]. Figure 2-5 indicates that on-state collector-emitter voltage V_{CE} is a non-linear function of

the collector current I_C and the junction temperature T_j when the turn-on gate voltage is fixed. When I_C is smaller than the value of the point of the intersection, V_{CE} decreases as T_j increases, which means negative temperature coefficient. When I_C is higher than the value of the point of the intersection, V_{CE} increases as T_j increases, which means positive temperature coefficient. The relationship of V_{CE}, I_C, and T_j can be expressed by equation (6) in theory in the region where V_{CE} has almost linear relationship with I_C and has positive coefficient with T_j [44].

$$V_{CE}(T_j, I_C) = \left[V_0 - \alpha_1(T_j - T_{j0})\right] + \left[R_{CE0} + \alpha_2(T_j - T_{j0})\right] \cdot I_C \tag{6}$$

where V_0 represents the threshold voltage drop and R_{CE0} represents on-state resistance of the IGBT chips at the reference junction temperature T_{j0}; α_1 and α_2 are the temperature coefficients for on-state voltage drop and on-state resistance, respectively.

When the collector current I_C is specified, the equation (6) can be deduced to equation (7), which can be expressed by equation (8).

$$\frac{V_{CE}(T_j, I_C)}{I_C} = \left[\frac{V_0}{I_C} + R_{CE0}\right] + \left[\frac{\alpha_1(T_j - T_{j0})}{I_C} + \alpha_2(T_j - T_{j0})\right] \tag{7}$$

$$R_{on}(T_j) = R_{on0} + \alpha_3(T_j - T_{j0}) \tag{8}$$

where

$$R_{on} = \frac{V_{CE}}{I_C}$$

$$R_{on0} = \frac{V_0}{I_C} + R_{CE0} = \frac{V_{CE0}}{I_C}$$

$$\alpha_3 = \frac{\alpha_1}{I_C} + \alpha_2$$

and R_{on0} represents virtual on-state resistance of the IGBT chips at the reference junction temperature T_{j0}. α_3 is the temperature coefficient for virtual on-state resistance.

For a silicon chip, the material difference between the upper and lower layers of the chip is ignored, which can be regarded as a uniform resistance. The resistance of the IGBT chip can be obtained from the output characteristic curve and the formula (8). According to the formula (9), the resistivity of the chip can be obtained.

$$R = \sigma \frac{d}{S} \tag{9}$$

where R is the resistance, σ is the resistivity, and d and S are the height and the area of chips, respectively.

$$\sigma = \sigma_0 + \alpha_3 (T_j - T_{j0}) \tag{10}$$

Equation (10) can be obtained by combining equation (8) and (9). In this study, this linear fitting method is used to describe the resistivity variation of the chip with temperature change in the linear region of output characteristic curve. Figure 2-6 illustrates the temperature dependence of the resistivity of the IGBT chip.

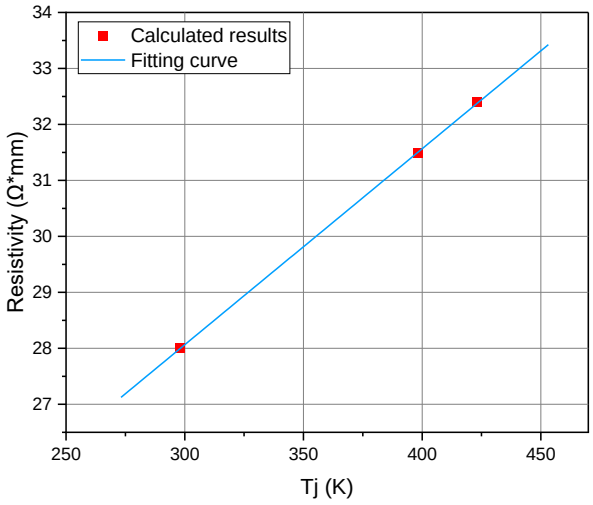


Figure 2-6 Temperature-dependent electrical resistivity of IGBT chip.

Table 2-2 exhibits material parameters of the IGBT module [47, 75, 97, 98]. According to IGBT chip size, the electrical resistivity and temperature coefficient of IGBT chips under different current are calculated in Table 2-3.

Table 2-2 Material parameters of IGBT module.

IGBT Module	Material	Size (mm)	Electrical Conductivity (S/m)	Thermal Conductivity (W/(m·K))	Poisson's Ratio	Young's Modulus (GPa)
Bond Wire	Al	Radius 0.15	3.77×10^{7}	238	0.33	70
IGBT	Si	13×13×0.12	Temp.	148	0.28	170
Chip Solder	Sn-Ag-Cu	13×13×0.05	6.67×10^{6}	70	0.4	43
Copper 1	Cu	32×38×0.1	6×10^{7}	401	0.35	110
Ceramic	Al_2O_3	32×38×0.25	1	55	0.27	275
Copper 2	Cu	31×37×0.1	6×10^{7}	401	0.35	110
DBC Solder	Sn-Ag-Cu	31×37×0.05	6.67×10^{6}	70	0.4	43
Baseplate	Cu	122×62×3	6×10^{7}	401	0.35	110

Table 2-3 Resistivity and temperature coefficient of the IGBT chips.

I_C /A	90	150	210	270	330	390	450	510
Resistivity /Ω·mm	69	47	37	31	27	24	22	21
V_{CE} /V	1.23	1.4	1.54	1.65	1.77	1.89	2.00	2.11
Temperature coefficient	-0.0001	0.0178	0.0288	0.0359	0.0370	0.0388	0.0392	0.0395

2.2.2 Boundary Conditions for Multiphysics Finite Element Model

As presented in Figure 2-2, the collector and emitter of the IGBT module are connected to external circuit, and current flows into the collector and flows out from the emitter respectively. Therefore, the coppers connected with the collectors are set as boundary current source, and the coppers connected with the emitters are set as the ground. When the current is loaded into the IGBT module, it flows through the bonding wires, coppers and chips in the module, and the

ceramic layer is set as the insulation boundary in the electrical field due to its low conductivity. Therefore, the layers under the ceramic layer are also electrical insulation.

In actual application, the IGBT module is closely connected with the heat sink through the thermal grease. If the heat sink model is taken into account in the modeling process, it needs to couple flow field with the existed field, which may bring huge amount of calculation. On the other hand, because of the difference of the physical size of the heat sink and the IGBT module is big, especially for the heat sink and the bond wire. For example, the size of the heat sink in usually exceeds 25×15 cm, and the diameter of the bond wire is less than 1mm. Even if different mesh grid method is used for different structure, it still consumes huge computing resources, and lead to non-convergence or less accurate result.

Therefore, the model of heat sink is simplified to equivalent heat transfer function. In the model, the bottom surface of the baseplate is set as the convective heat transfer boundary, and parameters of heat transfer function is obtained according to experiment cooling condition. Because the IGBT module is completely packaged in operation and the silicone gel filling into the package has low thermal conductivity and electrical conductivity which provides thermal isolation and electrical insulation, other surface of the module is set as thermal isolation surface. The bottom surface of the baseplate is the only surface to achieve hear transfer. What's more, it is supposed that there is no relative movement of the layers, and all the materials combine well. Figure 2-7 indicates the boundary condition setting of IGBT module in the finite element model.

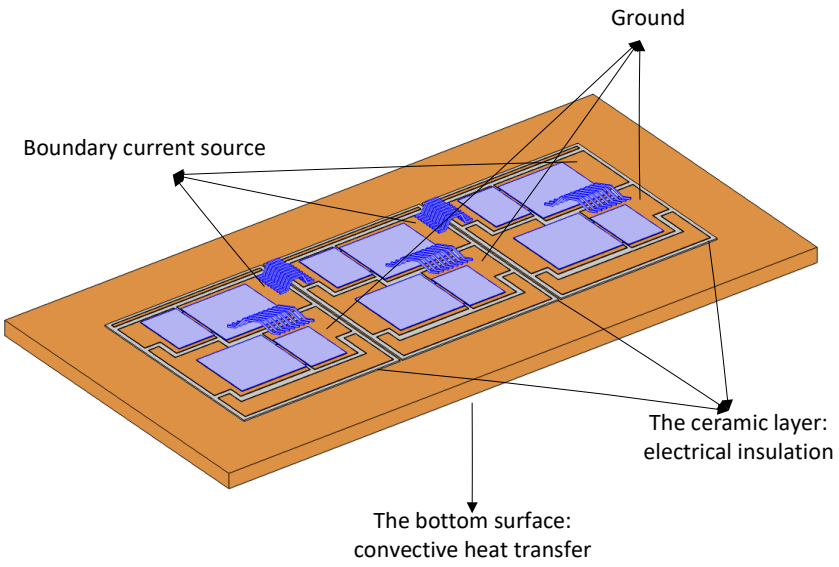


Figure 2-7 Boundary conditions of multi-physical field model.

The mesh grid is directly related to the precision and accuracy of the computation results. The IGBT module studied in this research has a large difference in physical dimensions between different parts. If same mesh grid method is applied to different parts, it can lead to low accuracy and precision or the poor computation efficiency. To improve the convergence of the iteration calculation and achieve high accuracy and efficiency, a multi-level mesh grid method is adopted. For smaller parts, such as the bond wires, chips and the solder layers, are divided by fine mesh, while for larger parts, such as copper layer and ceramic layer, the grid is divided by normal mesh. Figure 2-8 displays the mesh grid of the finite element model.

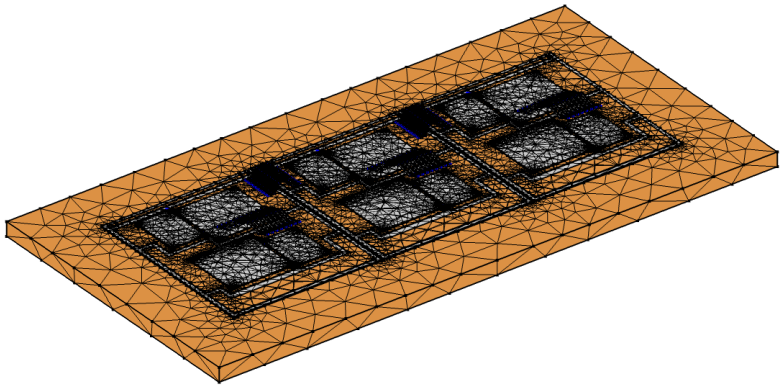


Figure 2-8 3D finite element model of the IGBT module.

2.3 Validation of the Multiphysics Finite Element Model

During the operation of the module, only upper bridge leg or lower bridge leg is working. At the same time, IGBT chips is easier to be failure than FWD chips, which makes IGBT chips become the key component to determine the reliability of the module [6]. To reduce the computation time of the finite element model, only the IGBT chip of the upper bridge arm is studied in this research. Considering that IGBT and anti-parallel FWD have one-way conduction characteristic, FWD chips needs to be set as electrical insulation when IGBT chips is conducted. Therefore, the bond wires connected to the top of all FWD chips and the IGBT chips of the lower bridge arm are removed to achieve electrical insulation.

2.3.1 Validation of the Finite Element Model in Electrical Field

To verify the accuracy of the finite element model built in last section, the simulation results of the model and results of the manufacture datasheet are compared under different electrical operating conditions. According to [75], the cooling method for the IGBT module is water cooling method when the module is used in wind turbines as an inverter. The speed of the cooling water is set as 1m/s, and the temperature of the water is 20℃. Thus, the finite element model sets the same cooling water speed and temperature for heat transfer function as initial condition. The current source is set as 90A, 150A, 210A, 270A, 330A, 390A, and 450A, and the cooling condition of the model is adjusted to keep the junction temperature as 25℃, 125℃, and 150℃, respectively, to verify the output characteristics of the IGBT module.

Figure 2-9 illustrates output characteristics curves from datasheet and simulation. Good consistency is observed with voltage error less than 0.03V as the collector current and junction temperature rise.

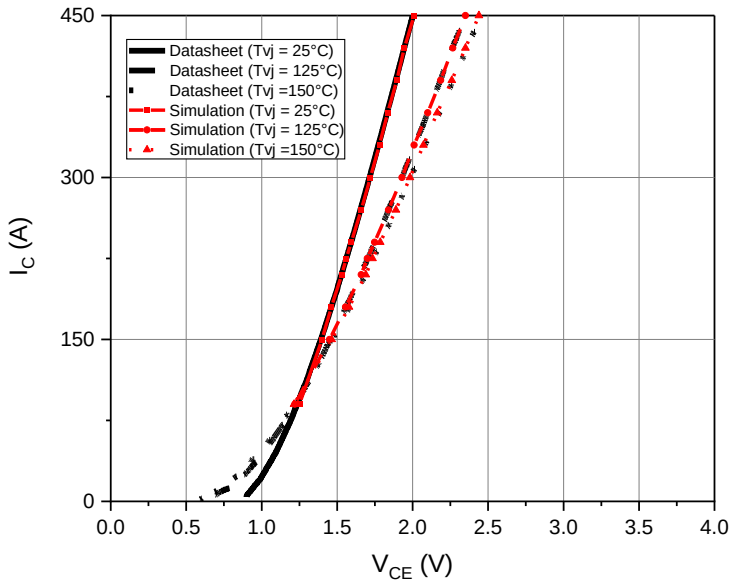


Figure 2-9 Output characteristics curves from datasheet and simulation.

2.3.2 Validation of the Finite Element Model in Thermal Field

The corresponding parameters and boundary are set for the finite element model. Firstly, the transient temperature characteristic of IGBT module is analyzed. The load current is set as 300A. The transient temperature impedance can be calculated according to Equation (11) [84]. The transient temperature impedance curve obtained from simulation is compared with transient temperature impedance curve from manufacture datasheet, as shown in Figure 2-10. The two curves basically coincide, which proves the accuracy of the finite element model.

$$Z_{thjc}(t) = \frac{T_j(t) - T_c(t)}{P_{loss}} \tag{11}$$

where Z_{thjc} is transient temperature impedance between junction and case, and P_{loss} is average dissipated power.

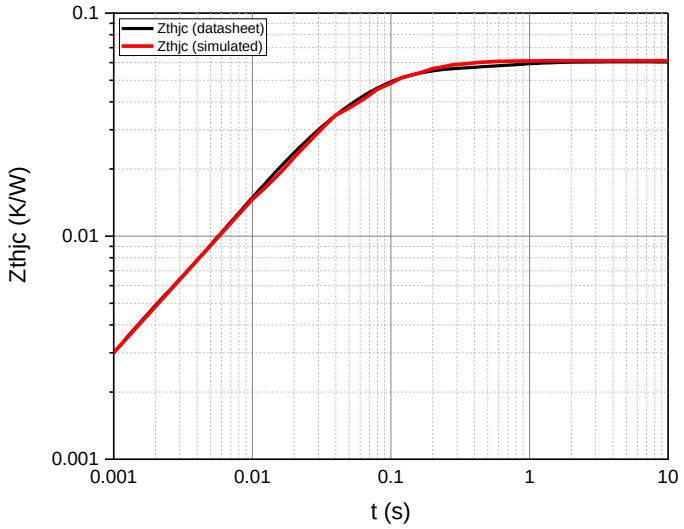


Figure 2-10 Comparison of transient thermal impedance curve from datasheet and simulation.

Before 1s, the transient thermal impedance gradually rises. After 1s, both transient thermal impedance curves enter the steady state. Under the steady state, thermal resistance between junction and case R_{thjc} can be obtained from Equation (12) [83]:

$$R_{thjc} = \frac{T_j - T_c}{P_{loss}} \tag{12}$$

The calculated thermal resistance value is 0.063 K/W, and thermal resistance value in the datasheet is 0.06 K/W. The simulation result and the datasheet value as shown in Table 2-4. It can be found that the error between simulation result and the datasheet value is small, which is 5%. The error is mainly caused by using the equivalent convective heat transfer parameters instead of the heat sink model. However, the result still confirms that the model has a high computational accuracy for the low error.

Table 2-4 Comparison of thermal resistances from simulation and datasheet.

Chip	Simulation value	Datasheet value	Error
IGBT	0.063	0.06	5%

The temperature characteristic of IGBT module at steady state is analyzed. To be compared with the experimental results obtained from [75], the speed of the water is set as 1m/s, and the temperature of the water is 30°C. The conduction current is set to 90A, 150A, and 225A. Figure 2-11 displays the temperature distribution for the module under different current load. It can be found that the high temperature area is mainly concentrated in the surface of the chips and the bond wires at the steady state, and the temperature gradually decreases from the center of the chip to the edge. The junction temperature of the middle chip is the highest because of thermal coupling effect, and the junction temperature of the right chip is higher than the junction temperature of the left chip. As the load current increases, the junction temperature and the case temperature also increase. The corresponding case temperatures are shown in Table 2-5.

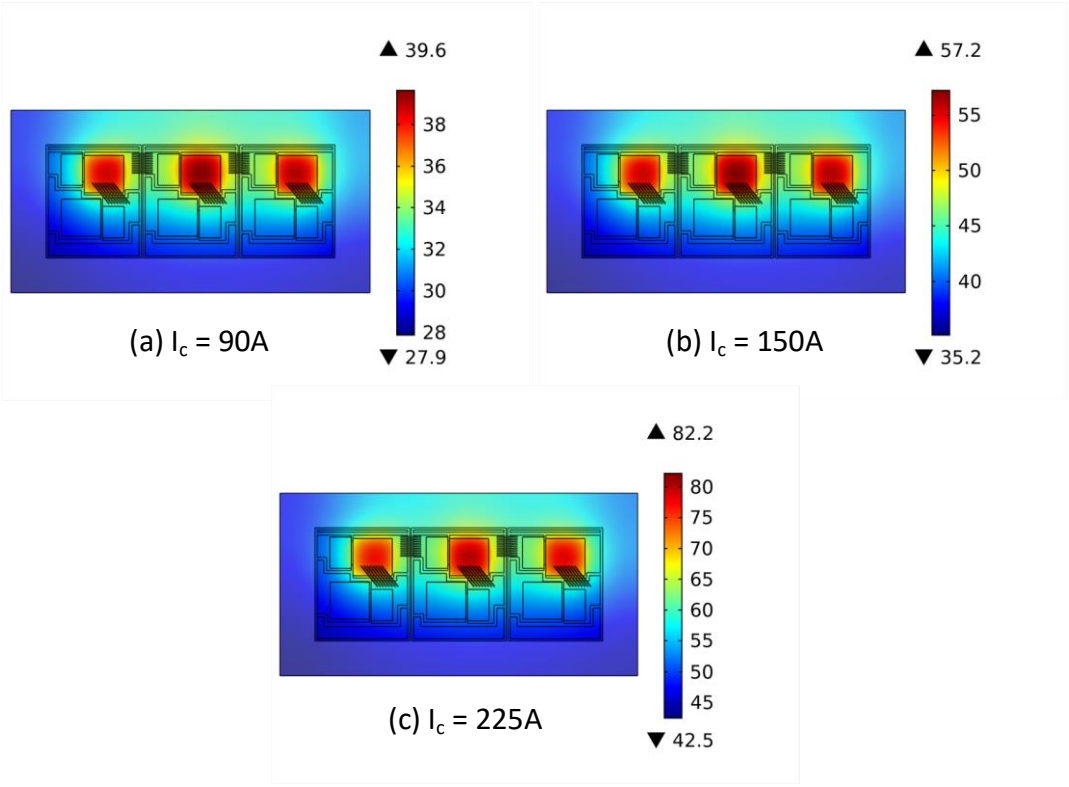


Figure 2-11 Temperature distribution of the IGBT module.

According to [75], temperature sensors are installed close to the bottom surface of the IGBT module and the positions are under the center of each IGBT chip to record the case temperature of

each chip. The case temperatures at steady state under different conduction current are monitored by the temperature sensors. The results are collected in Table 2-5.

Table 2-5 Comparison of case temperature obtained from experiment and simulation at steady state.

Current		Case temperature		
		Chip L (S_1)	Chip M (S_2)	Chip R (S_3)
90A	Experiment values	36.4℃	37.8℃	36.7℃
	Simulation values	36.4℃	37.3℃	36.7℃
	Error	0	1.32%	0
150A	Experiment values	49.1℃	53.6℃	51.6℃
	Simulation values	51.1℃	52.8℃	51.7℃
	Error	4.07%	1.49%	0.19%
225A	Experiment values	67.4℃	73.9℃	70.7℃
	Simulation values	69.7℃	72.5℃	70.5℃
	Error	3.41%	1.89%	0.28%

The simulation results and experiment results of case temperature under different conduction current are shown in Table 2-5. The simulation results and experiment results indicate the same trend that the middle chip has the highest case temperature, and then the case temperature of the right chip is a little bit higher than the case temperature of the left chip. When the conduction current is 90A, the error only appears in the middle chip (S_2). There is 0.5℃ difference between the simulation result and the experiment result, and the error is about 1.32%. When the conduction current is set as 150A and 225A respectively, the maximum error appears in the left chip (S_1) and the highest one is 4.07%, which is still in the acceptable range of the accuracy. This is because that the simulation sets up ideal current excitation and heat dissipation conditions, while the experiment result is affected by the environment condition and the measurement accuracy of the temperature sensor, etc. Therefore, it is inevitable to deviate from the simulation value.

The above results illustrated in this section verified the validation of the finite element model in electrical field and thermal field. It can be concluded that the model established in this research

has high accuracy and is effective to obtain the electrical-thermal characteristics of the IGBT module, and it can be reliable support for follow-up research.

2.4 Summary

Compared with thermal analysis in isolated electrical field and thermal field, thermal analysis by building electro-thermal FEM is more accurate. In this chapter, an electro-thermal coupling FEM of multi-chip IGBT module is firstly established, which considers the temperature dependent electrical resistivity of IGBT chips and simplify the heat sink model to equivalent convective heat transfer equation.

Secondly, the validity of the model is verified by calibrating the output characteristic curve and transient thermal impedance curve from datasheet. The deviation of simulated collector-emitter voltage from the manufacture data as the collector current and junction temperature rise is less than 0.03V. There is good consistency between the simulated transient thermal impedance curve and the curve from datasheet. Moreover, the thermal resistance calculated by the simulation model is close to the original data, the maximum error is 5%.

In addition, the temperature distribution of the electro-thermal FEM is close to the measurement results of the experiment. The maximum error of the case temperature appears in the left chip (S_1), which is 4.07% when the conduction current reaches 225A. All the error is within an acceptable range for ideal current excitation and heat dissipation condition of simulation, and measurement error of experiment.

The FEM established in this paper will provide a strong support for the electrical and thermal analysis of the multi-chip IGBT modules and precursors extraction in the following chapters.

Chapter 3 Precursor for Chip Solder Fatigue

As IGBT module is a multi-layered structure of materials with different coefficient of thermal expansion (CTE), it experiences repetitive thermo-mechanical stresses during switching operations under harsh environment and temperature swings. Different failure modes such as solder fatigue, wire bond lift-off and wire bond heel cracking can be caused by this thermal-mechanical stress. A study indicates that chip solder cracks occurs because of the thermo-mechanical stresses generated by mismatch of the CTE between the silicon chip and the substrate when the fluctuation of the junction temperature (ΔT_j) between maximum value of T_j ($T_{j\ max}$) and maximum value of T_j ($T_{j\ min}$) is less than 80℃, and wire bond heel cracking occurs when ΔT_j is more than 100℃ [23]. Because ΔT_j region of most power modules is lower than 100℃, the solder degradation appears early than bond wire degradation, and becomes the dominant failure mode [23, 47]. Moreover, if there is solder fatigue, because of change of heat transfer path and increase of thermal resistance, the bond wire degradation will be accelerated [23, 47, 99]. Thus, this research extracts precursor to evaluate the health condition of multi-chip IGBT module with a focus on the IGBTs' chip solder fatigue.

In this chapter, a new precursor for locating the position of degraded chip solder and evaluating the degradation degree of the chip solder of the multi-chip IGBT module is proposed. Firstly, based on the 3D electro-thermal finite element model of the multi-chip IGBT module, the junction temperature and case temperature of the IGBT module with different fatigue degrees for three fatigue scenarios are analyzed. In addition, current distribution and variation of collector-emitter voltage with different fatigue degrees are studied. Furthermore, the relative sensitivity of fatigue sensitive parameters (FSPs) is analyzed and compared. Based on the analysis, a 3D electro-thermal-magnetic finite element model of the multi-chip IGBT module is built to extract magnetic

flux density as a new precursor for health condition assessment, and high relative sensitivity of the new precursor is verified. For better sensitivity, selectivity, and generality, the magnetic flex density is proposed as a new precursor for building health state assessment model.

3.1 Thermal Analysis of IGBT Module under Chip Solder Fatigue

3.1.1 Temperature Distribution at low output frequency

There is a large-scale derating for the IGBT module in actual application and the working current is usually much lower than the rated current. For instance, the power converter in wind turbines has two parallel structures, and the actual conduction current for the IGBT module is about one half or one third of the rated conduction current [75]. Therefore, the collector current I_c for the IGBT module is 150~300A.

The generating frequency in wind power plants is usually slow, and temperature swings on the chip with the same frequency can be produced when the generating frequency is smaller than 5 Hz [100]. Figure 3-1 presents junction temperature swing and case temperature swing for each chip when the collector current is 150A and the generating frequency is 5Hz. Symbol L, M, and R are used to represent the position of the chip. The frequency of the temperature swings is the same as the generating frequency. After 1s, the temperature reaches steady state, which indicates same time constant with the transient thermal impedance.

At the steady state, the zooming in figure demonstrates that the junction temperature and case temperature of the middle chip is higher than that of the other two chips though the junction temperature and case temperature swings for each chip are the same, which is about 10℃ and 7℃, respectively.

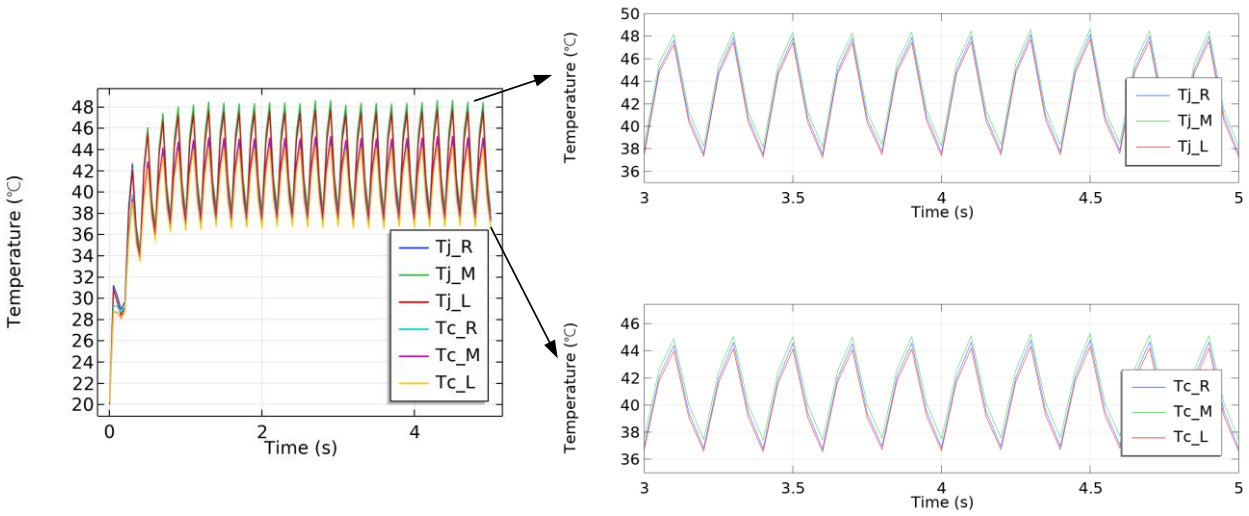


Figure 3-1 Temperature distribution and swing when Ic=150A, f=5Hz.

3.1.2 On-state Temperature Distribution under Chip Solder Fatigue

Solder voids and solder delamination are two common fatigue modes of solder, as indicated in Figure 3-2. Both of them are generated by strain mechanisms including elastic, plastic and creep during long-term temperature swings [29]. The voids appearing in the corner of the solder layer has more severe effect on the performance of the thermal conduct of the solder layer, and the effect can be seen as a reduction in the effective cross-section area of the solder layer [30, 47]. The delamination gradually forms by crack diffusion under strain mechanisms and spreads from the edge of the solder layer to the center region [5, 23, 29]. The results of these two fatigue modes are both the increase of the thermal resistance and the increase of junction temperature. Thus, the chip solder fatigue in the module can be simplified as a reduction in cross-section area of the chip solder layer toward the center in the simulation.

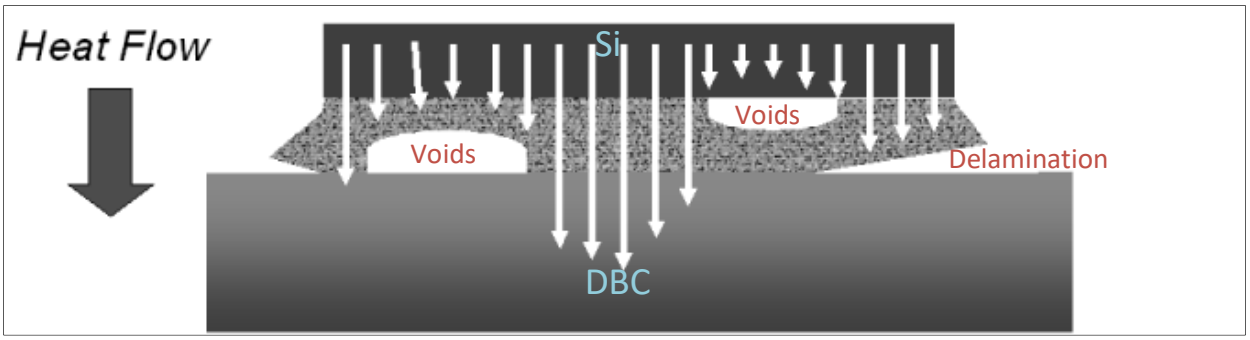


Figure 3-2 Voids and delamination in chip solder layer [29] .

The concept of shedding degree is introduced to characterize the degree of reduction in cross-section area of the chip solder layer, and its value is the proportion of the reduction area of solder to the total area of solder. Schematic diagram of different shedding degree of the chip solder is shown as follows:

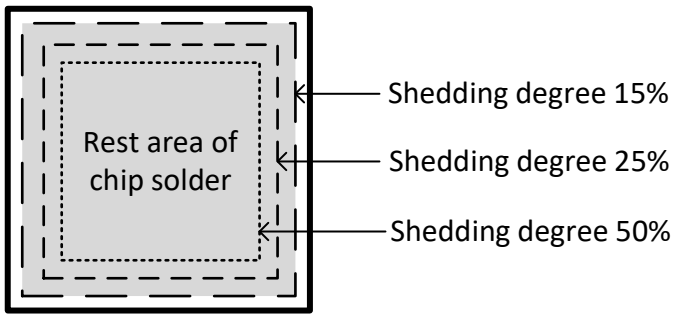


Figure 3-3 Schematic diagram of different shedding degree of the chip solder.

The material properties and boundary condition of the finite element model are set as the same in Section 2.2. The speed of the cooling water is set as 1m/s, and the temperature of the water is 20℃. The conduction current is set as 300A. Because the junction temperature fluctuation of the three IGBT chips in upper leg is almost same and the manufacture quality may be slightly different for each chip, it is possible for one of the chip solders first appears fatigue. Therefore, three possible fatigue situations are studied in this research.

First possible fatigue situation is that only middle chip solder appears fatigue. When the shedding degree is 0%, 4%, 8%, and 17% respectively, the on-state junction temperature distribution under different shedding degree of middle chip solder is demonstrated in Figure 3-4.

It can be seen that the highest junction temperature of IGBT module appears in the middle chip, which is 2.8°C higher than junction temperature of the right chip and 4.3°C higher than junction temperature of the left chip when the shedding degree is 0%. The junction temperature distribution is uneven. This is caused by thermal coupling effect between chips and between different layers [101-103]. The lay-out of the chips is not symmetric so that the thermal coupling effect on the left and the right chip is not the same.

When the shedding degree is increased to 4%, there is 0.3°C increase for the middle chip, and 0.7°C increase for the left chip and right chip. When the shedding degree is increased to 8%, there is 0.8°C increase for the middle chip, and about 2.0°C increase for the left chip and right chip compared with healthy condition. When the shedding degree is increased to 17%, there is 2.2°C increase for the middle chip, and about 5.8°C increase for the left chip and right chip compared with healthy condition. At the same time, the highest junction temperature appears in the right chip. It can be found that all the junction temperature increases as the shedding degree increases, and the rising rate of the junction temperature of the middle chip is lower than the rising rate of the junction temperature of the left chip and the right chip.

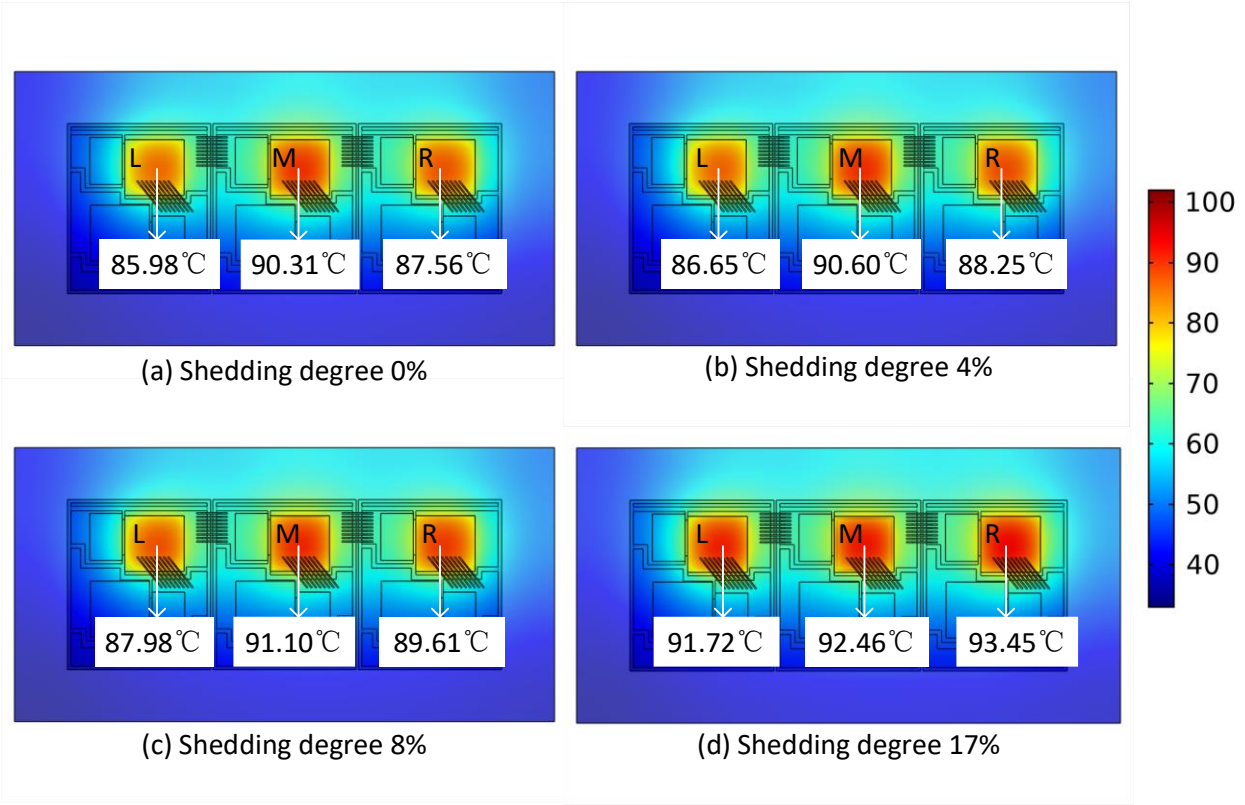


Figure 3-4 On-state junction temperature distribution of the IGBT module under different shedding degree of middle chip solder.

For further analysis of the change of junction temperature, junction temperature change of each chip under different shedding degree of the middle chip solder is illustrated in Figure 3-5. It clearly indicates that the rising rates of the junction temperature of the left chip and the right chip are almost the same, and the difference between the junction temperature of the left chip and the junction temperature of the right chip keeps the same as the middle solder fatigue increases. Because there is no change for the lay-out and heat transfer path of the left chip and the right chip and the change of the junction temperature of the middle chip is small, the change of power loss is the reason for the change of the junction temperature for left and right chips. The rising rate of the junction temperature of the middle chip is smaller than the other two and the variation of the junction temperature of the middle chip is the smallest one when the effective heat transfer area of

the middle chip continually decreases. It means the power loss of the middle chip changes during the fatigue process.

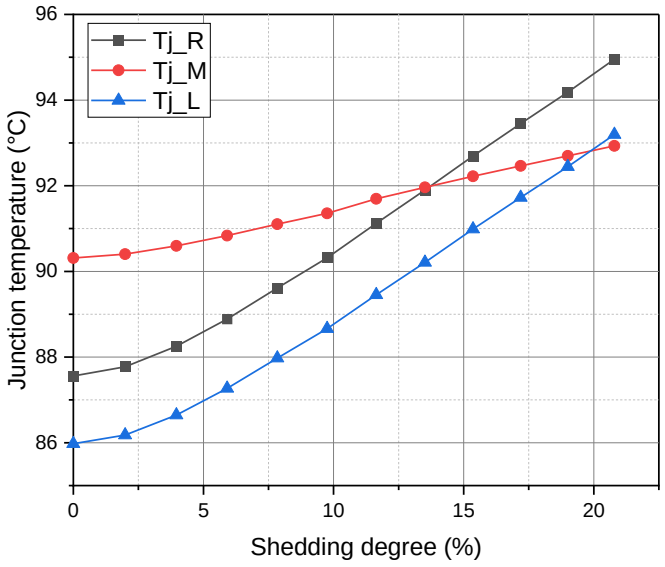


Figure 3-5 Change of the junction temperature as the shedding degree of middle chip solder increases.

When the IGBT is at on-state, the power loss is calculated by equation (13) [104].

$$P_{loss} = V_{CE} \times I_C \tag{13}$$

The change of the power loss for each chip as the shedding degree of middle chip solder increases is presented in Figure 3-6. It demonstrates that the power loss of the left chip and the right chip rises at almost the same rate as the shedding degree of middle chip solder increases. This result shows same trend as the change of the junction temperature of the left chip and right chip with different shedding degree. Meanwhile, the power loss of the middle chip reduces as the shedding degree of middle chip solder increases. The result is different from the result in a single chip module that an increasing power loss is found when chip solder fatigues [48]. The reason for the change of the power loss is the change of V_{CE} and I_C, which is analyzed in Section 3.2. Though the power loss decreases as the shedding degree of middle chip solder increases, the

junction temperature still rises. This is caused by thermal coupling effect and lower heat transfer rate caused by less effective heat transfer area.

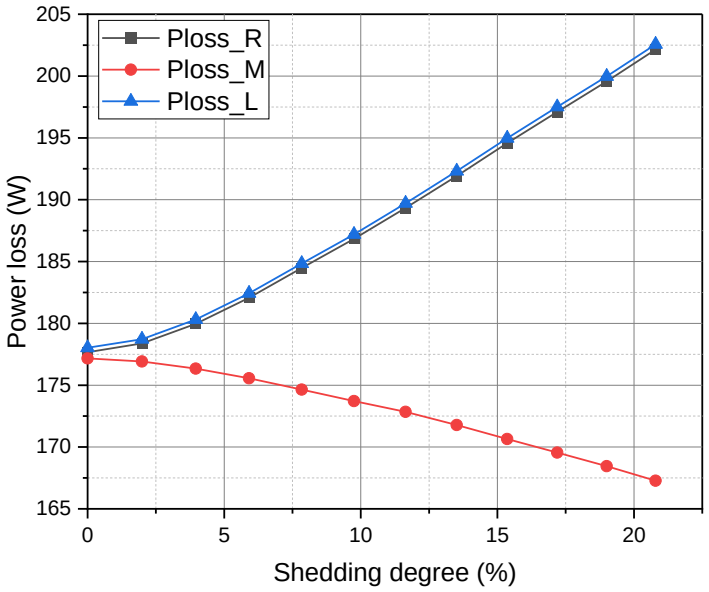


Figure 3-6 Change of the power loss as the shedding degree of middle chip solder increases.

When the shedding degree is 0%, 4%, 8%, and 17% respectively, the on-state case temperature distribution under different shedding degree of middle chip solder is illustrated in Figure 3-4. Like the distribution of the junction temperature, the highest case temperature of IGBT module appears in the middle chip when the shedding degree is 0%, which is 2.8°C higher than case temperature of the right chip and 4.3°C higher than case temperature of the left chip. When the shedding degree is increased to 4%, there is 0.1°C increase for the middle chip, and 0.5°C increase for the left chip and right chip. When the shedding degree is increased to 8%, there is 0.4°C increase for the middle chip, and about 1.6°C increase for the left chip and right chip compared with healthy condition. When the shedding degree is increased to 17%, there is 1.0°C increase for the middle chip, and about 4.6°C increase for the left chip and right chip compared with healthy condition. At the same time, the highest junction temperature appears in the right chip.

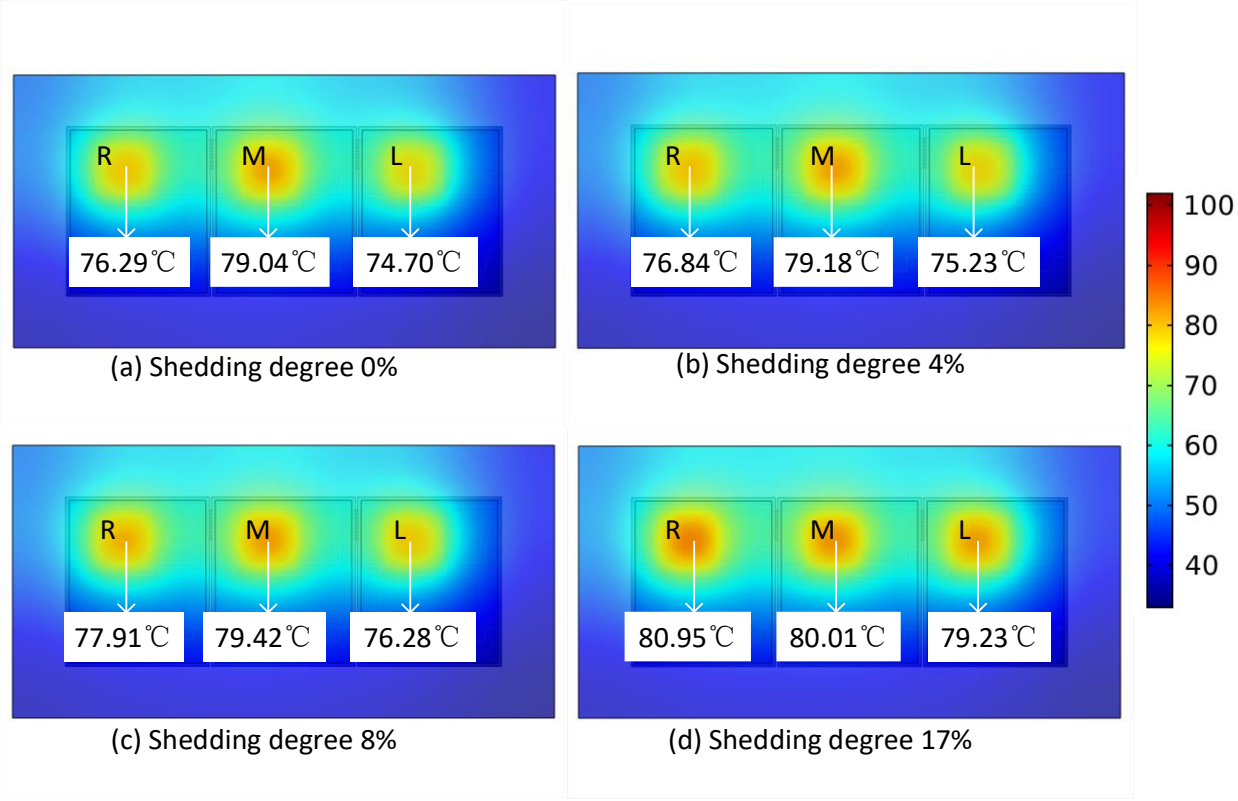


Figure 3-7 On-state case temperature distribution under different shedding degree of middle chip solder.

The trend of the change of the case temperature is similar to the trend of the change of the junction temperature as the shedding degree of the middle chip solder increases. All the case temperature increases as the shedding degree increases. The rising rate of the case temperature of the left chip and the right chip is almost the same, and the difference between the case temperature of the left chip and the junction temperature of the right chip keeps same as the middle solder fatigue increases. The rising rate of the case temperature of the middle chip is smaller than the rising rate for left and right chips. All the results can be obviously observed from Figure 3-8. However, the variation of the case temperature distribution is a little bit lower than the variation of the junction temperature distribution, as demonstrated in Table 3-1. It verifies that when the junction temperature is hard to measure for the encapsulated structure [105, 106], it is an effective way using case temperature instead of junction temperature to monitor solder fatigue [48].

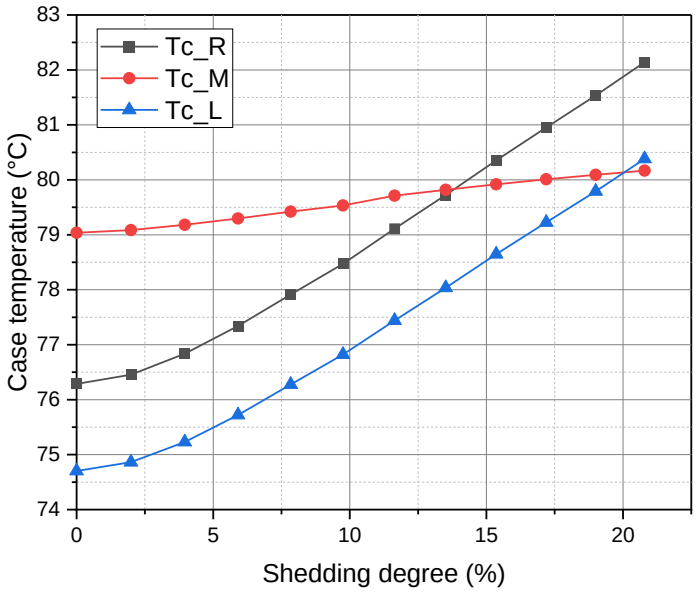


Figure 3-8 Change of the case temperature as the shedding degree of middle chip solder increases.

Table 3-1 Variation of junction temperature distribution and case temperature distribution as the shedding degree of middle chip solder increases.

Shedding degree	Junction temperature variation		Case temperature variation	
	M	L/R	M	L/R
0%	0°C	0°C	0°C	0°C
4%	0.3°C	0.7°C	0.1°C	0.5°C
8%	0.8°C	2.0°C	0.4°C	1.6°C
17%	2.2°C	5.8°C	1.0°C	4.6°C

As well as the change of the temperature distribution, the change of the thermal resistance is the direct result of solder fatigue. Thermal resistance can be calculated according to Equation (12), and the thermal resistance with different shedding degrees for each chip is shown in Figure 3-9. Only thermal resistance of the middle chip changes as the shedding degree increases, which clearly reflects the fatigue of the middle chip solder. It can be found that the thermal resistance of the middle chip increases rapidly when the solder fatigue accumulates to a certain extent, which is

consistent with the existing research results that the fatigue accumulation process is non-linear [65, 107].

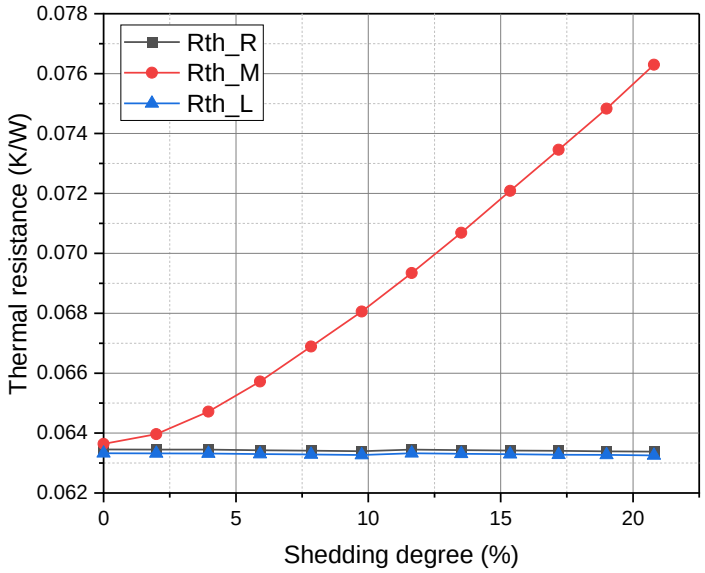


Figure 3-9 Change of the thermal resistance as the shedding degree of middle chip solder increases.

The junction temperature, power loss, case temperature, and thermal resistance with different shedding degree of the left chip solder are illustrated in Figure 3-10. The change of these thermal characteristic parameters as the shedding degree of the right chip solder increases is displayed in Figure 3-11. Different from the scenario that middle chip solder fatigues, the change rates of junction temperature and case temperature of unaged chips are different. Because the rising rate of the power loss for unaged chips are almost the same, the thermal coupling effect is the main reason for the different rising rate of junction temperature and case temperature between unaged chips.

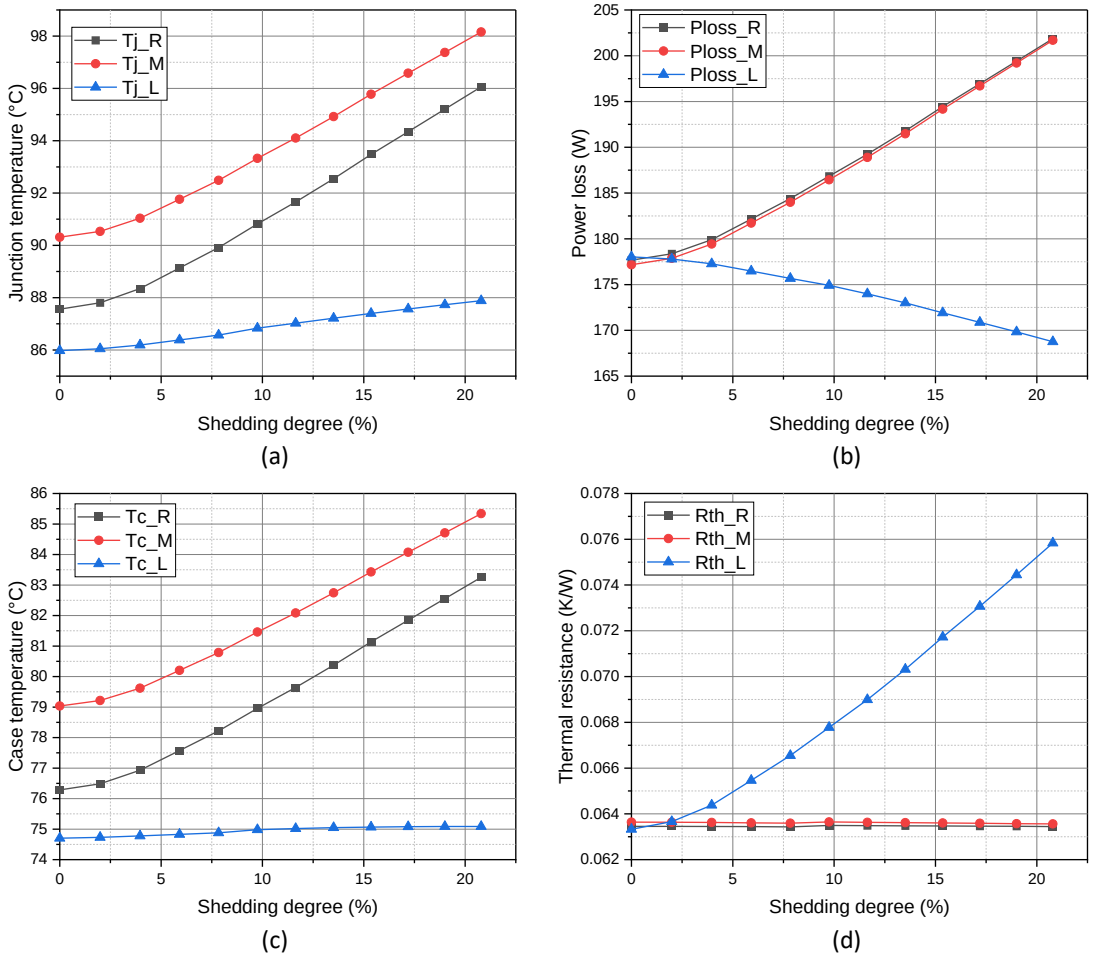


Figure 3-10 Change of thermal characteristic parameters as the shedding degree of left chip solder increases. (a) Change of junction temperature, (b) Change of power loss, (c) Change of case temperature, (d) Change of thermal resistance.

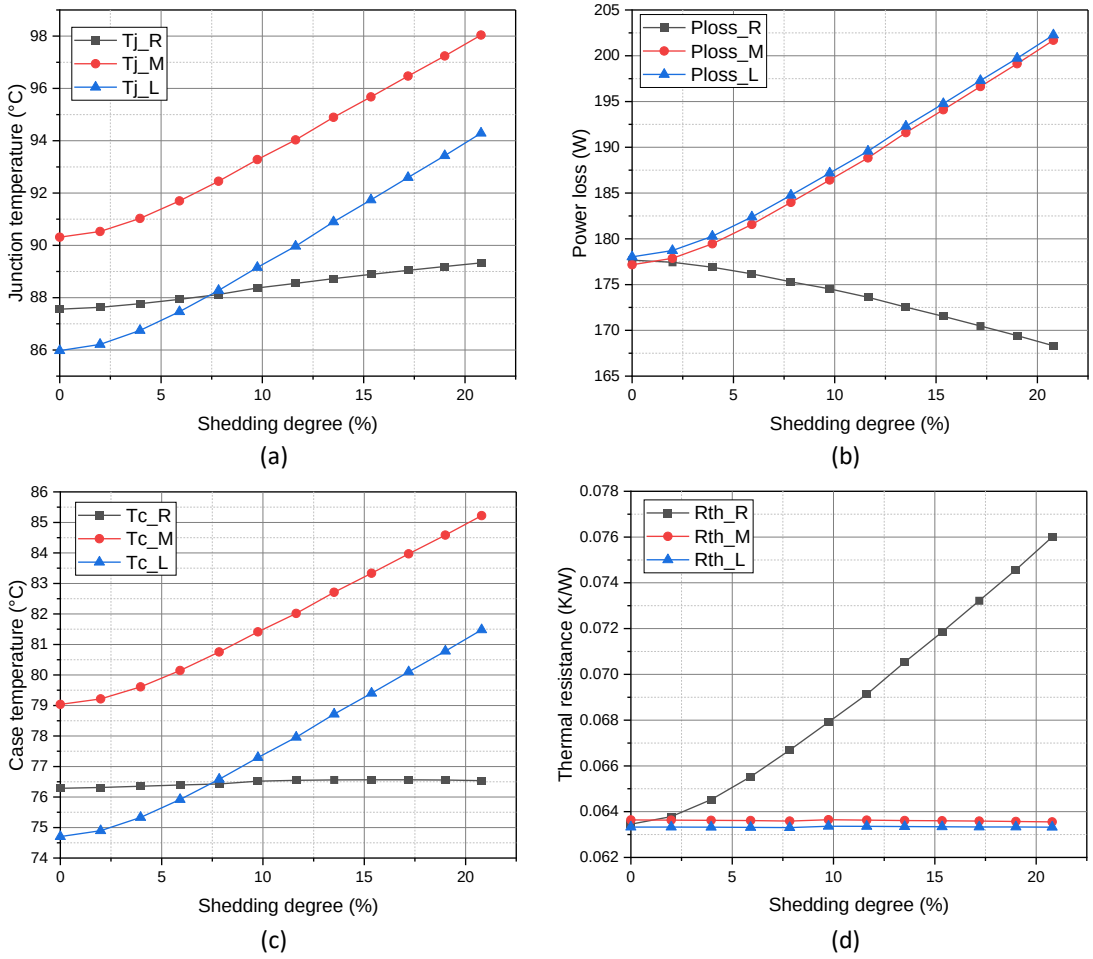


Figure 3-11 Change of thermal characteristic parameters as the shedding degree of right chip solder increases. (a) Change of junction temperature, (b) Change of power loss, (c) Change of case temperature, (d) Change of thermal resistance.

The variation of junction temperature and case temperature with different shedding degree of left chip solder and with different shedding degree of right chip solder aging are presented in Table 3-2 and Table 3-3 respectively. The case temperature variation is always smaller than the junction temperature variation because of different heat transfer structure. Moreover, the variation of both junction temperature and case temperature for aged chip are almost the same in the two scenarios. Meanwhile, the variation of both junction temperature and case temperature for unaged chip are almost the same in the two scenarios, which is caused by the same variation of the power loss.

Table 3-2 Variation of junction temperature and case temperature as the shedding degree of left chip solder increases.

Shedding degree	Junction temperature variation			Case temperature variation		
	L	M	R	L	M	R
0%	0℃	0℃	0℃	0℃	0℃	0℃
4%	0.2℃	0.7℃	0.8℃	0.1℃	0.6℃	0.6℃
8%	0.6℃	2.2℃	2.4℃	0.2℃	1.8℃	1.9℃
17%	1.6℃	6.3℃	6.8℃	0.4℃	5.0℃	5.6℃

Table 3-3 Variation of junction temperature and case temperature as the shedding degree of right chip solder increases.

Shedding degree	Junction temperature variation			Case temperature variation		
	R	M	L	R	M	L
0%	0℃	0℃	0℃	0℃	0℃	0℃
4%	0.2℃	0.7℃	0.8℃	0.1℃	0.6℃	0.6℃
8%	0.6℃	2.1℃	2.3℃	0.1℃	1.7℃	1.9℃
17%	1.5℃	6.1℃	6.6℃	0.3℃	4.9℃	5.4℃

The change of the thermal characteristic parameters due to chip solder fatigue can be summarized in Figure 3-12. As a chip solder fatigues, the corresponding thermal resistance increases, which results in an increase of averaged junction temperature. The increase of the junction temperature of the aged chip is smaller than that of the other health chips, which is caused by the decrease of the power loss for the aged chip and the increase of the power loss for the health chips. The total power loss increases, and the increasing heat flux density results in the increase of the case temperature through the package structure. The increasing junction temperature and stress concentration will result in crack propagation, which will lead to further increase of power loss and temperature.

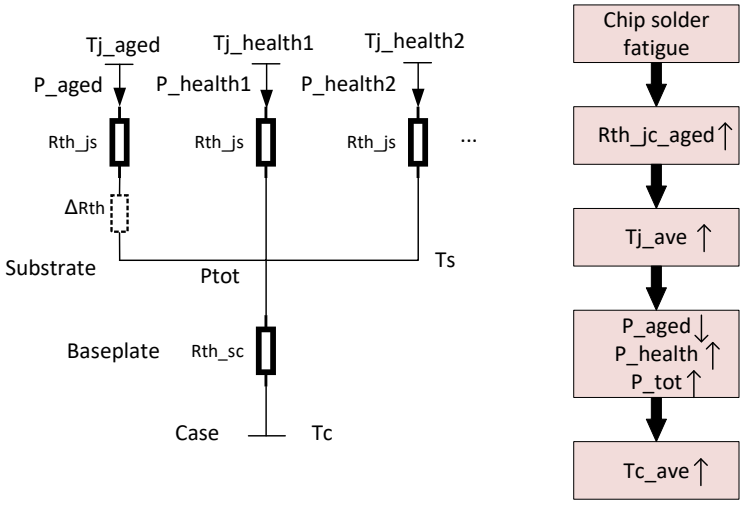


Figure 3-12 Change of thermal network in a multi-chip IGBT module due to chip solder fatigue.

3.2 Electrical Analysis of IGBT Module under Chip Solder Fatigue

3.2.1 Change of On-state Voltage under Chip Solder Fatigue

As discussed in Chapter 2, on-state collector-emitter voltage (V_{CE}) is a temperature sensitive parameter because the electrical resistivity of the chip has positive temperature coefficient when the collector current (I_c) for the IGBT module is 150~300A. The change of V_{CE} with different shedding degree for three different fatigue scenarios is shown in Figure 3-13. It indicates that the curves of V_{CE} with different shedding degree in the three fatigue scenarios are highly overlap. This reason for the slight difference is that the temperature coefficient is small. There is about 0.3V change of V_{CE} for 10℃. Therefore, the different scenario of chip solder fatigue is hard to be identified by the change of the collector-emitter voltage of the module. In addition, the change of ambient temperature influences the assessment of the degradation by the change of the collector-emitter voltage due to temperature sensitivity. Thus, on-state collector-emitter voltage is not good as a precursor for identification of fatigue scenarios and assessment of health state of the IGBT module.

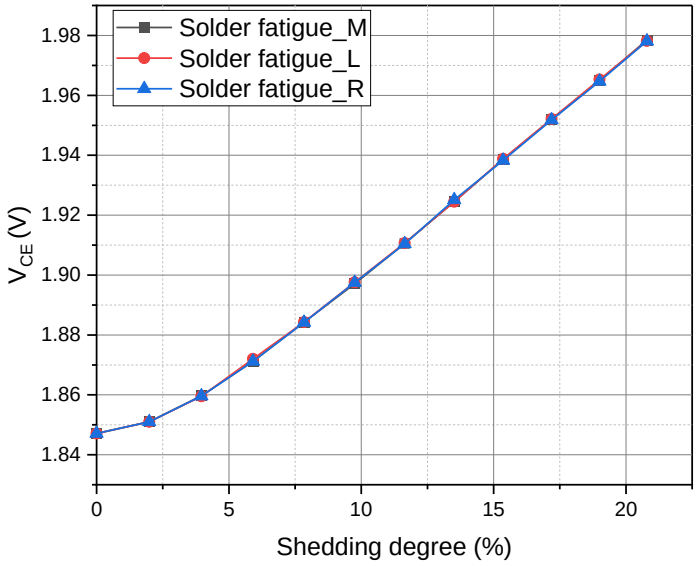


Figure 3-13 Change of V_{CE} with different shedding degree.

3.2.2 Current Distribution of under Chip Solder Fatigue

According to Equation (13), the on-state power loss of the IGBT chip is determined by V_{CE} and I_c. When a chip solder fatigues, the corresponding power loss of the aged chip decreases and V_{CE} increases as the shedding degree increases. It implies that the collector current of the aged chip decreases as the shedding degree increases. This suppose is verified in Figure 3-14. It demonstrates that the collector current of the aged chip decreases as well as the collector current of the healthy chips increase. The variation of the current of the two healthy chip keeps same as the shedding degree increases, which is about a half of the variation of the current of the aged chip. Unbalanced current sharing becomes more serious as the shedding degree increases. Increased junction temperature and resistance of the solder (R_S) caused by increasing shedding degree are the reasons for more serious unbalanced current sharing [108], like Figure 3-15 shows .

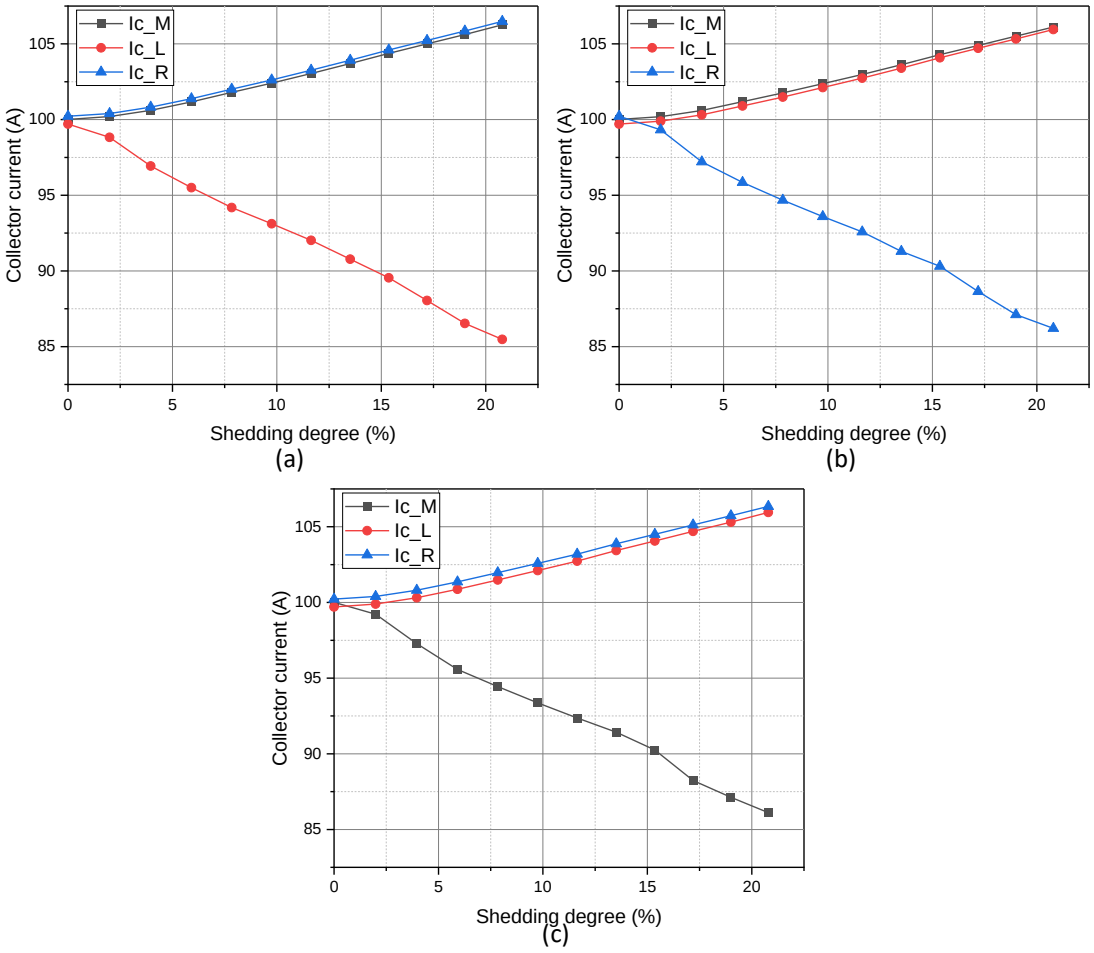


Figure 3-14 Current distribution with different shedding degree. (a) Middle chip solder fatigue, (b) Left chip solder fatigue, (c) Right chip solder fatigue.

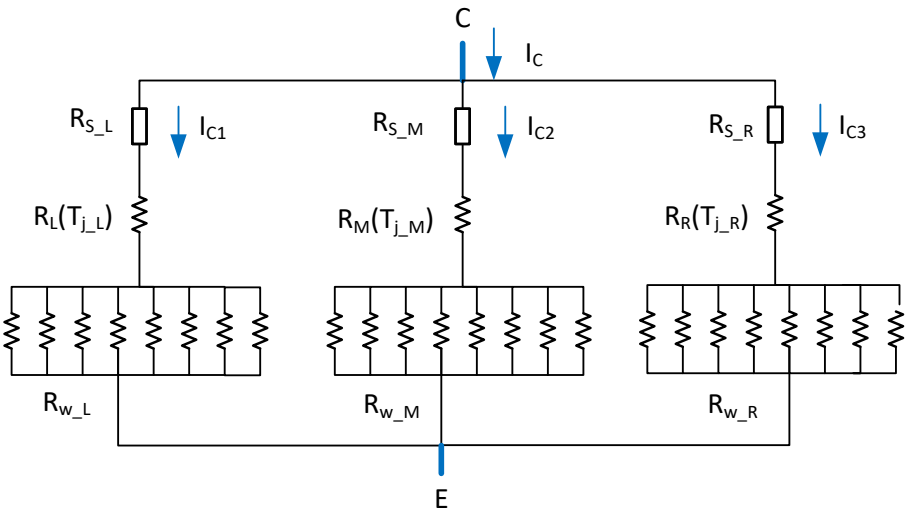


Figure 3-15 Simplified on-state electrical circuit of the multi-chip IGBT module.

In Figure 3-15, as the fatigue of a chip solder increases, both the effective area of heat transfer and electrical conductivity of the chip solder continually reduce. The change of the heat transfer path results in the increase of corresponding junction temperature. The increased junction temperature of the aged chip makes an increase for the resistance of the chip (R) due to positive temperature coefficient. When there is no bond wire lift off, the resistance of the bond wires (R_W) maintains the same. The increased resistance of the chip and resistance of the chip solder (R_S) in the aged branch result in less current through the branch. Higher current through the other healthy branches can produce higher power losses, then increase the junction temperature, which also makes the resistance of these chips increasing. Thus, the total resistance of the module increases and higher V_{CE} is obtained. If the fatigue degree increases, unbalance current sharing is strengthened, which can accelerate the fatigue of other chip solder or form other failure modes.

3.3 Relative Sensitivity for Fatigue Sensitive Parameters

Based on the analysis of the thermal characteristic parameters and electrical parameters, junction temperature, case temperature, power loss, and collector current have obvious change as the fatigue increases and they have different change for three different degradation scenarios. It means that they are sensitive to the chip solder fatigue. It is difficult to directly compare their sensitivity because they are measured in different unit. Thus, a normalized parameter named relative sensitivity is proposed for comparison and calculated by (14) [6]. 'Variation' is the change of fatigue sensitive parameters (FSPs) from health to failure. 'Baseline value' is the value of fatigue sensitive parameters when the module is healthy.

$$Relative\ sensitivity = \frac{|Variation|}{Baseline\ value} \times 100\% \tag{14}$$

A 20% increase of thermal resistance from junction to case is normally used as the failure criteria for solder failure of the IGBT module [48, 49, 63, 109]. The relative sensitivity of the fatigue sensitive parameters is calculated according to the failure criteria and the baseline value, which is exhibited in Table 3-4. Both power loss (P_{loss}) and collector current (I_c) have the highest relative sensitivity of the chip solder fatigue. In other word, the chip that has a decrease of P_{loss} fails when there is a 14% increase of P_{loss} of one chip, or the chip that has a decrease of I_c by 14% fails.

Table 3-4 Comparison of the relative sensitivity of the FSPs.

Scenarios	FSPs	Relative sensitivity		
		R	M	L
Middle chip solder fatigue	T_j	8%	3%	8%
	T_c	8%	1%	8%
	P_{loss}	14%	6%	14%
	I_c	6%	14%	6%
Left chip solder fatigue	T_j	10%	9%	2%
	T_c	9%	8%	1%
	P_{loss}	14%	14%	5%
	I_c	6%	6%	14%
Right chip solder fatigue	T_j	2%	9%	10%
	T_c	0.3%	8%	9%
	P_{loss}	5%	14%	14%
	I_c	14%	6%	6%

However, to obtain the power loss in practical application, forward voltage V_{CE} and collector current for each chip need to be measured. It has lower attraction to use power loss as the precursor for more complex measurement when it has the same relative sensitivity as the collector current. Thus, I_c is the ideal precursor used for health state assessment.

3.4 Magnetic Flux Density as A New Precursor

Though collector current has high relative sensitivity about the degradation, the measurement of it is a problem. The tradition current measurement circuit is usually invasive which directly contacting with the terminals of IGBTs [49]. For multi-chip parallel IGBT module without integrated shunt resistor, only total conduction current can be measured by contacting with the terminals of the module, and the collector current of each parallel IGBT chip is difficult to be identified because of the encapsulation structure. The same problem occurs with current transformer that it is difficult to assembly in laminated bus bar structures or connect with bond wires of each chips [110, 111].

Nonintrusive condition monitoring techniques would be ideal. New current measurement technologies such as Rogowski-coils [112], Giant Magnetoresistance (GMR) [113], and magnetic flux sensor [114, 115] are all base on the distribution of the magnetic field. It means if there is a change for current, there would be a change for magnetic field. In addition, electromagnetic radiation (EMR) signature is proposed as a precursor for the health assessment of the converters [116]. Those new technologies conform the possibility of using magnetic field quantities instead of current as a precursor for condition monitoring, which can be monitored by nonintrusive techniques.

3.4.1 Electromagnetic Theory and Electro-thermal-magnetic FEM

According to quasi-static approach ($\nabla \cdot \vec{J} = 0$) of electromagnetic theory, the distribution of the magnetic field of the IGBT module with steady current can be solved by equation (15)-(18) [117].

$$\vec{B} = \nabla \times \vec{A} \tag{15}$$

$$\vec{B} = \mu_0 \mu_r \vec{H} \tag{16}$$

$$\nabla \times \vec{H} = \vec{J} \tag{17}$$

$$\vec{J} = \sigma \vec{E} + \overrightarrow{J^e} \tag{18}$$

These quantities in equation (15)-(18) are:

- Magnetic flux density $\vec{B}$
- Magnetic vector potential $\vec{A}$
- Magnetic field intensity $\vec{H}$
- Permeability of vacuum μ_0
- Relative permeability of the material μ_r
- Current density $\vec{J}$
- Electric field intensity $\vec{E}$
- Electric conductivity σ
- Externally generated current $\overrightarrow{J^e}$

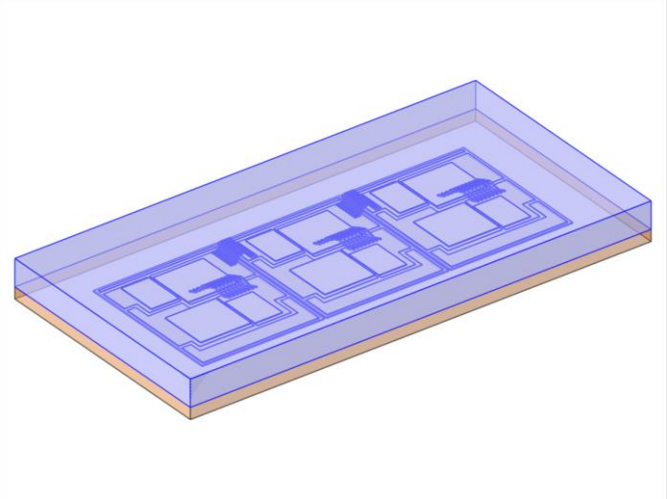


Figure 3-16 The electro-thermal-magnetic FEM.

The value of the magnetic field quantities can be solved by setting magnetic material property and boundary conditions of the finite element model of the IGBT module. Thus, an electro-thermal-magnetic FEM is built based on the accurate electro-thermal FEM of the IGBT module. A 4mm high air layer is built above the electro-thermal FEM because the package of the module is exposed to the air for actual application. The electro-thermal-magnetic FEM is shown in Figure 3-16. After obtaining the current distribution, the magnetic flux density distribution above the bond wires can be solved by equation (15)-(18). The multi-physics coupling relationship in the electro-thermal-magnetic FEM is demonstrated in Figure 3-17.

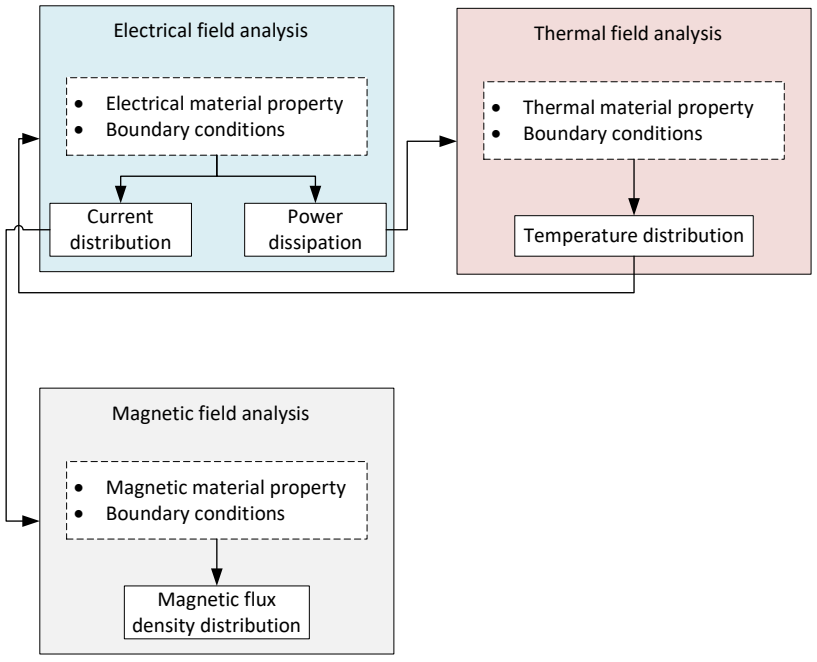


Figure 3-17 Multi-physics coupling relationship in the electro-thermal-magnetic FEM.

3.4.2 Magnetic Flux Density Distribution under Chip Solder Fatigue

The magnetic flux density (B) distribution in health state of the IGBT module is shown in Figure 3-18. It is found that the area above the bond wires connected to the top surface of the chips has higher value of B compared with other area of the air above the IGBT module.

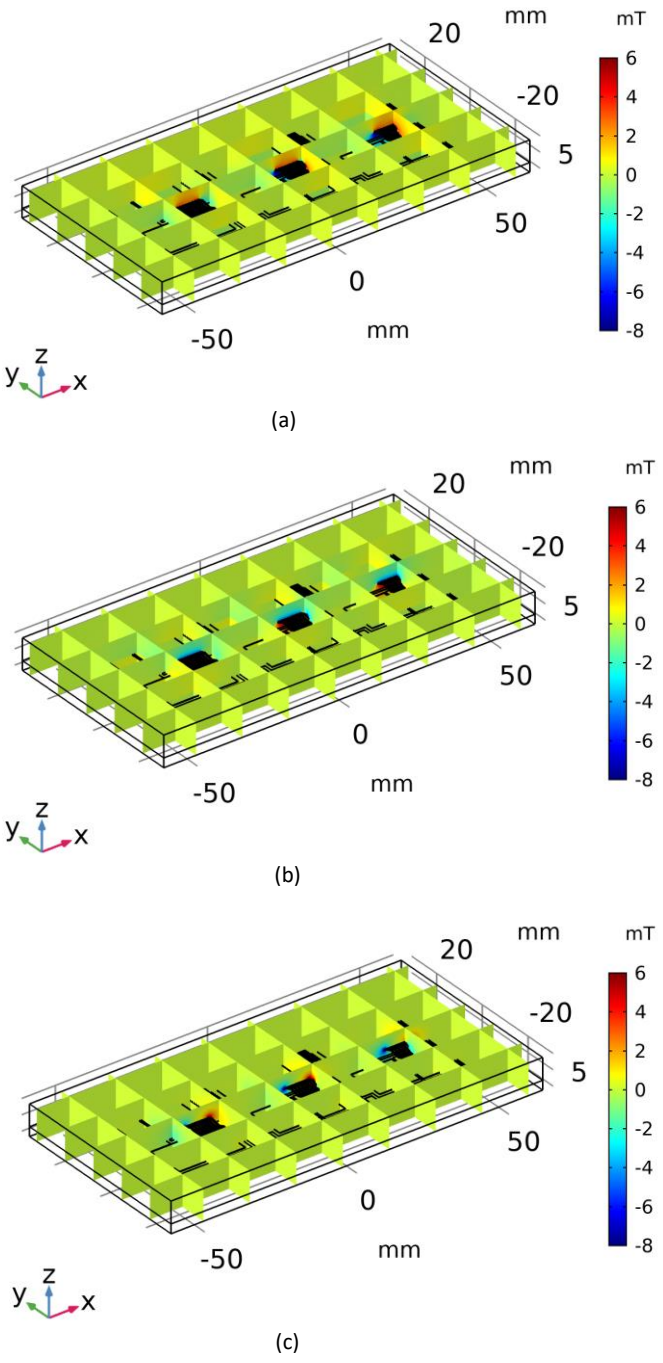


Figure 3-18 Magnetic flux density distribution in health state of the IGBT module. (a) Magnetic flux density in X-axis direction (B_X), (b) Magnetic flux density in Y-axis direction (B_Y), (a) Magnetic flux density in Z-axis direction (B_Z).

Compared with B_Y and B_Z, B_X has higher value at the same point in the area above the bond wires. Thus, B_X is chosen to be analyzed with different shedding degree. A line which is 3mm higher than the line through all the midpoint of the chip bond wires is cut from x = -50mm to x =

50m, and the B_X distribution with different shedding degree of middle chip solder along this line is illustrated in Figure 3-19. The B_X of the points on the line above the bond wires of the left and the right chips increases as shedding degree of middle chip solder increases. The B_X of the points on the line above the bond wires of the middle chip decreases as shedding degree of middle chip solder increases. The change trend of B_X is the same as change trend of I_C.

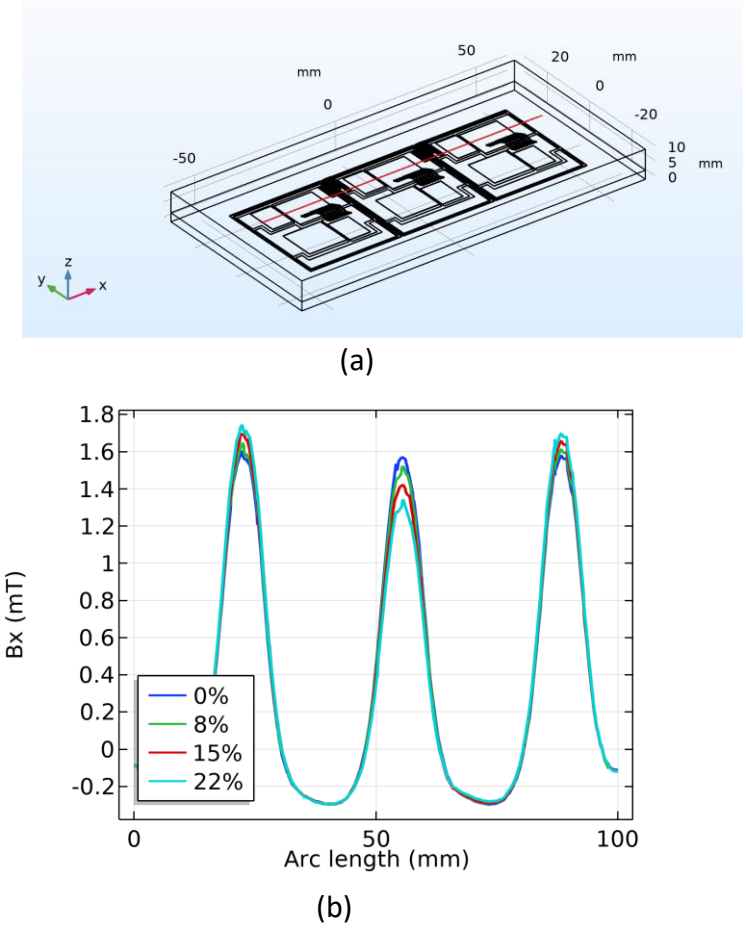


Figure 3-19 The B_X distribution with different shedding degree of middle chip solder along a 3D line. (a) The position of the 3D line, (b) The B_X distribution with different shedding degree of middle chip solder.

Three points where the peak value of B_X of each chip is on the line are chosen. The change of B_X for each chip as the shedding degree of the chip solder increases is presented in Figure 3-20. B_X and I_C not only present the similar change trend according to Figure 3-14 and Figure 3-20, but

also have similar relative sensitivity. The relative sensitivity of B_X for aged chip in each scenario is about 14%, and for healthy chip is about 8% which is higher than the relative sensitivity of I_C.

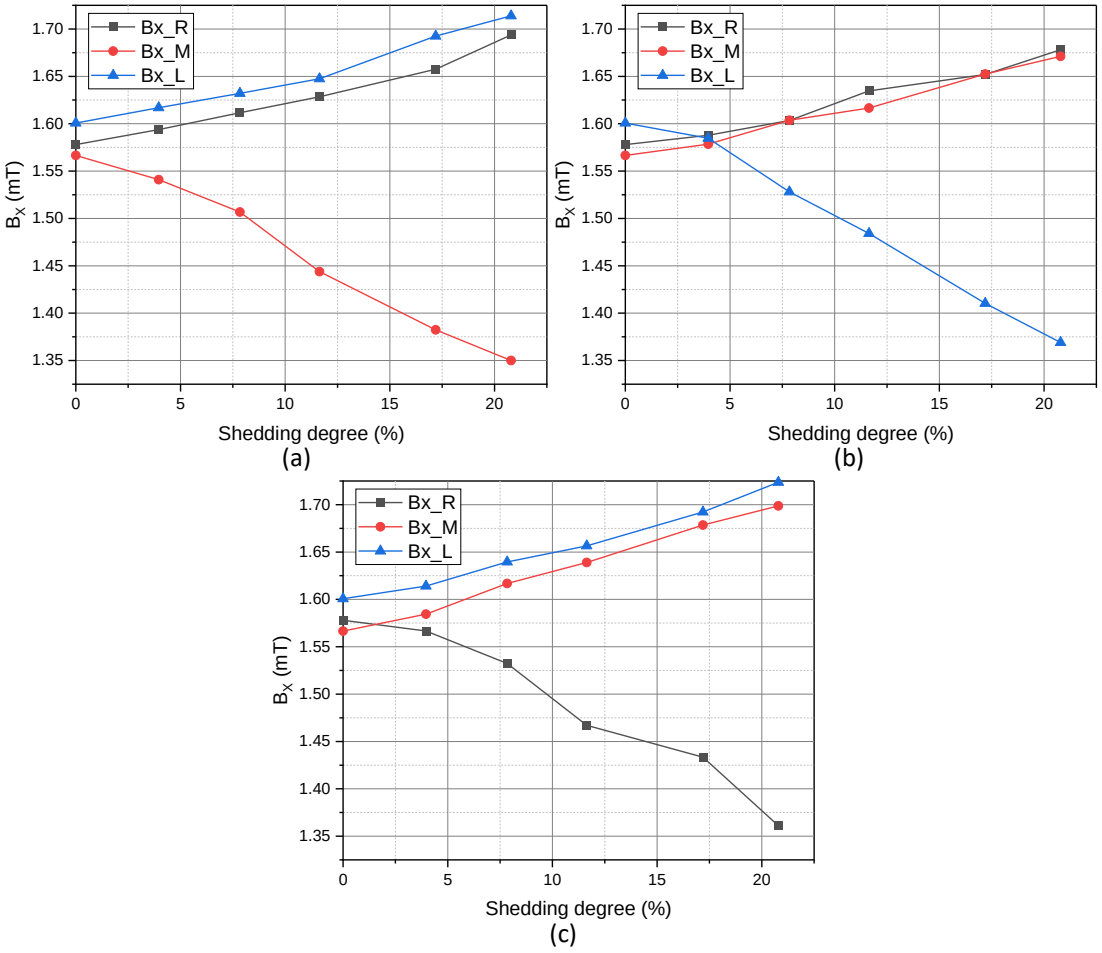


Figure 3-20 B_X distribution with different shedding degree. (a) Middle chip solder fatigue, (b) Left chip solder fatigue, (c) Right chip solder fatigue.

Compared with T_j and T_c, B_X also exhibits better selectivity because it is not influenced by temperature as the following tables indicate. There is no change for the distribution of B_X because the difference between the junction temperature of each chip keeps same as the ambient temperature changes. Furthermore, compared with other precursors used for condition monitoring, such as the turn-off time [118] and gate-emitter pre-threshold voltage [6], B_X has higher generality

due to applicability for power semiconductor devices other than a transistor [119]. Therefore, B_X is proposed as the precursor for chip solder fatigue in this research.

Table 3-5 The distribution of B_X with different ambient temperature for health module.

Ambient temperature (°C)	B_X_R (mT)	B_X_M (mT)	B_X_L (mT)
20	1.58	1.57	1.60
30	1.58	1.57	1.60
40	1.58	1.57	1.60
50	1.58	1.57	1.60

Table 3-6 The distribution of T_j with different ambient temperature for health module.

Ambient temperature (°C)	T_j_R (°C)	T_j _M (°C)	T_j _L (°C)
20	87.6	90.3	86.0
30	97.0	99.8	95.5
40	106.6	109.3	105.1
50	116.3	119.0	114.8

Table 3-7 The distribution of T_c with different ambient temperature for health module.

Ambient temperature (°C)	T_c_R (°C)	T_c _M (°C)	T_c _L (°C)
20	76.3	79.0	74.7
30	85.6	88.3	84.1
40	95.0	97.8	93.5
50	104.6	107.4	103.2

3.5 Summary

Because of same junction temperature swing which is lower than 80 °C for each chip, the chip solder fatigue appears before the bond wire fatigue, and it is possible for any chip solder to firstly start degradation. For each fatigue scenario, T_j, T_c, P_{loss}, V_{CE}, and I_c that normally extracted as a

precursor for health state assessment are analyzed with the degradation of the chip solder. Both T_j and T_c of each chip increases with different rate as the shedding degree increases. T_j and T_c of health chip rise faster which is caused by rapidly increased P_{loss}. The reasons for the increase of T_j and T_c of aged chip are the thermal coupling effect and the change of heat transfer path while P_{loss} decreases. The different change of P_{loss} for aged chip and health chips is caused by more severe unbalanced current sharing as chip solder fatigues and junction temperature increases. The current through the aged chip becomes lower for increased resistance of the chip solder and the silicon chip. V_{CE} of the module increases as chip solder fatigue because of increased junction temperature. However, there is little difference of the change of V_{CE} in different scenarios. Thus, only T_j, T_c, P_{loss}, and I_c are suitable to be used as precursor for health state assessment and degradation localization of the multi-chip IGBT module.

The relative sensitivity of T_j, T_c, P_{loss}, and I_c with chip solder degradation are compared. I_c is difficult to test by tradition measurement method though it has highest relative sensitivity with chip solder fatigue. The relationship between the current and magnetic field has been dug up and gradually applied in sensor technologies. Magnetic flux density is proposed for condition monitoring instead of I_c for easy achieved contactless measurement. The electro-thermal-magnetic model is established to generate magnetic flux density. The magnetic flux density B_X indicates higher relative sensitivity than I_c, and it is not be influenced by other parameters, like temperature. In addition, B_X is not only applicable in the condition monitoring of transistor, but also suitable for other power semiconductor device like diode. Based on the higher relative sensitivity and better selectivity and generality, magnetic flux density instead of collector current is proposed as a new precursor in this research.

Chapter 4 Health State Assessment Model

As shown earlier, obtaining the health state according to failure precursor before a catastrophic failure happens is important to improve the reliability of the converter and avoid further system downtime. Existing studies estimate the health state of device based on residuals between sensed measurement of a single precursor and the baseline value from a model using statistic techniques [22, 49, 83, 95, 120, 121]. When the health state is determined by multiple precursor parameters or the relationship between the precursor and the ageing degree is complicated, the analytical method is difficult to satisfy the need [2, 122, 123]. In addition, the analytical method always requires large residual with small disturbances, noise and modeling errors to ensure the accurate result [2, 123]. Thus, data-driven techniques such as neural networks (NNs) can be an alternative tool to solve the relationship between the precursor parameters and the health state. The date-drive techniques directly extract the relationship from historic information or monitored data without prior knowledge.

The previous chapters have demonstrated that comprehensive consideration of magnetic flux density as a precursor for chip solder fatigue, and the distribution of B_X can more effectively characterize the fatigue degree of IGBT modules and identify different scenarios of chip solder fatigue of the multi-chip IGBT module. The change of the distribution of B_X is nonlinear as fatigue degree increases. Therefore, a health state evaluation model based on back-propagation (BP) neural network for the IGBT module is established by introducing the above precursor parameters. It is of great significance for improving the reliability assessment of multi-chip power module and power electronic system.

4.1 The Structure of BP Algorithm

BP neural network was first proposed by Rumelhant and McClelland, which is the most common type of supervised artificial neural network [67]. It is a multi-layer feedforward network including forward propagation of input information and back propagation of calculated output error [68]. The basic structure of the network mainly includes input layer, hidden layer, and output layer [68]. The input signals of the system are transmitted to the neurons of the hidden layer through the neurons of the input layer, and then to the neurons of the output layer. The neurons in different layers are connected by synaptic weights, and bias are added in both the input layer and the output layer [68]. The relationship between the input layer and the output layer is learned through adjusting the weights and bias of each neuron in the network during training [67]. The network training is performed by using a nonlinear differentiable function to complete the adjustment of the weights [124]. When a forward propagation process is completed, if the difference between the actual output and the expected value exceeds the predetermined accuracy threshold, the network turns to the error backward propagation process, adjusting the weights and thresholds of each layer according to the gradient descent of error until the network output reaches the expected value [124, 125].

Because BP neural network has strong nonlinear processing ability and good self-learning, self-adapting, robustness, and generalization ability, it has been widely used in pattern recognition [125, 126]. Therefore, this research uses BP neural network to analyze the relationship between the electromagnetic parameters and the health state of the multi-chip IGBT module.

The key steps of BP neural network construction normally include:

1) Initialization of BP neural network structure. The node number of the input layer is determined by the number of features of input data, and the node number output layer size depends on the number of classification classes of output data. The node number of the

hidden layer is flexible, which affects the robustness of the neural network [127]. To get better performance, the node number of the hidden layer can be calculated by Hecht–Nelson method [127] or empirical formula [68]:

$$l = 2n + 1 \tag{19}$$

$$l = \sqrt{n + m} + a \tag{20}$$

where l is the number of hidden layer nodes, n is the number of input neurons, m is the number of output neurons, a is the regulating constant, usually between 0 and 10.

2) Initialization of BP neural network parameters. The weights and thresholds of the network can be randomly initialized. In addition, the row data need to be normalized to [-1, 1] to avoid a large network error between the data due to large differences in magnitude, which affects the calculation accuracy and convergence efficiency [68]. The normalization equation is [127]:

$$X' = \{X'_i\} = 2 \times \frac{X_i - X_{imin}}{X_{imax} - X_{imin}} - 1, \qquad i = 1,2,\ldots,n \tag{21}$$

where X_{imin} and X_{imax} are the minimum and maximum value of input array, and X_i denotes the real value of each vector.

3) Calculation of the network forward transmission process. For input arrays of training data $\{X_i\}$, the hidden layer output H and output layer output O in the forward process are [126]:

$$H_j = f_1\left(\sum_{i=1}^{n} \omega_{ij}\, x_i - a_j\right), \qquad j = 1, 2, \ldots, l \tag{22}$$

$$O_k = f_2\left(\sum_{j=1}^{l} H_j\, \omega_{jk} - b_k\right), \qquad k = 1, 2, \ldots, m \tag{23}$$

where a_j is the threshold value of the hidden layer, b_k is the threshold value of the output layer, f_1 is the transfer function of the hidden layer, f_2 is the transfer function of the output layer, ω_{ij} is the weight from input layer to hidden layer, and ω_{jk} is the weight from hidden layer to output layer.

4) Calculation of error between the output value of neural network and the expectation output value. Normally, mean square error (MSE) function is used cost function to minimize the error between the output value of neural network and the expectation output value [2, 127, 128]. However, the reduction of the error can be extremely slow when the estimated error decreases with training, which results in a long learning time. To get rid of this problem, the MSE are replaced by entropy error function such as cross-entropy function as a cost function, especially for classification purposes [129-133].

   For network with sigmoid activation function f(s) = 1/(1 + exp(-s)), following cross-entropy error function to be minimized[133]:

$$E_k = -[Y_k \ln(O_k) + (1 - Y_k) \ln(1 - O_k)] \tag{24}$$

   where Y_k is the target value, and E_k is the error between the target value and output value.

5) Weights and bias are updated as [133]:

$$\Delta\omega_{jk} = -\eta \frac{\partial E}{\partial \omega_{jk}} = \eta(Y_k - O_k)H_j \tag{25}$$

$$\Delta b_k = -\eta \frac{\partial E}{\partial b_k} = \eta(Y_k - O_k) \tag{26}$$

$$\Delta\omega_{ij} = -\eta \frac{\partial E}{\partial \omega_{ij}} = \eta \sum_{k=1}^{m} (Y_k - O_k)\omega_{jk}(H_j(1 - H_j))x_i \tag{27}$$

$$\Delta a_j = -\eta \frac{\partial E}{\partial a_j} = \eta \sum_{k=1}^{m} (Y_k - O_k)\omega_{jk}(H_j(1 - H_j)) \quad (28)$$

where η is the learning rate.

6) Training iterations. If the calculation accuracy is not satisfied within the number of training iterations, steps 3)~5) are repeated until the accuracy meets the requirements according to selected training algorithm. There are different training algorithms such as batch gradient descent method, scaled conjugate gradient, and resilient backpropagation method [124].

4.2 Health Evaluation Model Based on BP Neural Network

The health state evaluation of existing IGBT modules mainly focus on the baseplate solder fatigue and bond wire fatigue. The chip solder fatigue is rarely analyzed especially for multi-chip parallel IGBT module. The thesis proposes magnetic flux density distribution to realize the health state assessment of the module and identify the location of the fatigue. When using the above parameter to evaluate the health state of the module, it must be compared under the same operating condition. The magnetic flux density is determined by current, and temperature has no influence on it, which are verified in last chapter. Therefore, the operating condition of conduction current and magnetic flux density measured for each chip are considered when constructing the BP neural network. Thus, the number of nodes in the input layer of the BP neural network model n = 4.

With the consideration of the degradation progress of the module, the health state of the module is divided into five stages. According to [122], the corresponding range of change of thermal resistance of each stage and its treatment are shown in Table 4-1. To achieve the localization of chip solder fatigue, there are three scenarios for each aging stages. Thus, the total number of classes is 13, and they are represented by number from 0 to 12. The number of nodes of the output layer m = 13.

Table 4-1 Division of health state stages and corresponding treatment [122].

Increment of thermal resistance	Health state stages	Location	Representation	Treatment
0	Healthy	/	0	Normal operation
Less than 5%	Slight aging	M	1	Normal operation
		L	2	
		R	3	
5%–10%	Moderate aging	M	4	Regular maintenance
		L	5	
		R	6	
10%–15%	Serious aging	M	7	Frequent inspection and maintenance
		L	8	
		R	9	
15%–20%	Severe aging	M	10	Replacement
		L	11	
		R	12	

The number of hidden layer nodes (l) directly affects the calculation accuracy and efficiency. To ensure the performance of the model, it is necessary to select the appropriate number of hidden layer neurons. According to formula (20), the range of l is from 5 to 15. The performance of BP neural network with different number of hidden layer nodes are compared to determine the best one.

The standard training algorithm in the BP neural network has poor practical application due to slow learning rate and easy to fall into local minimum [127]. In response to this problem, series of improved algorithms have been proposed, such as the momentum gradient method, Levenberg-Marquardt (L-M) method, batch gradient descent method, scaled conjugate gradient, and resilient backpropagation method.

Among different improved algorithms, scaled conjugate gradient performs same speed as the Levenberg-Marquardt (LM) on function approximation but faster in large networks [134]. It is more robust than resilient backpropagation for error reduction using same speed in resolving

pattern recognition problems [134]. Thus, scaled conjugate gradient is selected as the training algorithm in this research. The active functions normally applied in BP neural network with scaled conjugate gradient algorithm are sigmoid function in hidden layer and softmax function in output layer for classification purpose [134-136]. Softmax function is always pairing with cross-entropy error function for improved classification accuracy [137]. The equation of softmax function and its cross-entropy error is shown as follows [135]:

$$f(s) = \frac{\exp(s_q)}{\sum_{p=1}^{P} \exp(s_p)}, \qquad q = 1, 2, \ldots, P \tag{29}$$

$$E = -\sum_{k=1}^{m} Y_k \ln(O_k) \tag{30}$$

In summary, the health state assessment model of the IGBT module based on BP neural network established in this research is shown in Figure 4-1. The conduction current and the magnetic flux density of each chip are used as input parameters of the neural network, and normalized preprocessing is performed to reduce errors. The scaled conjugate gradient algorithm is used to train the training data to obtain the knowledge model between the health state stages and the input parameters. The model is validated by the validation data, and then the test data is evaluated.

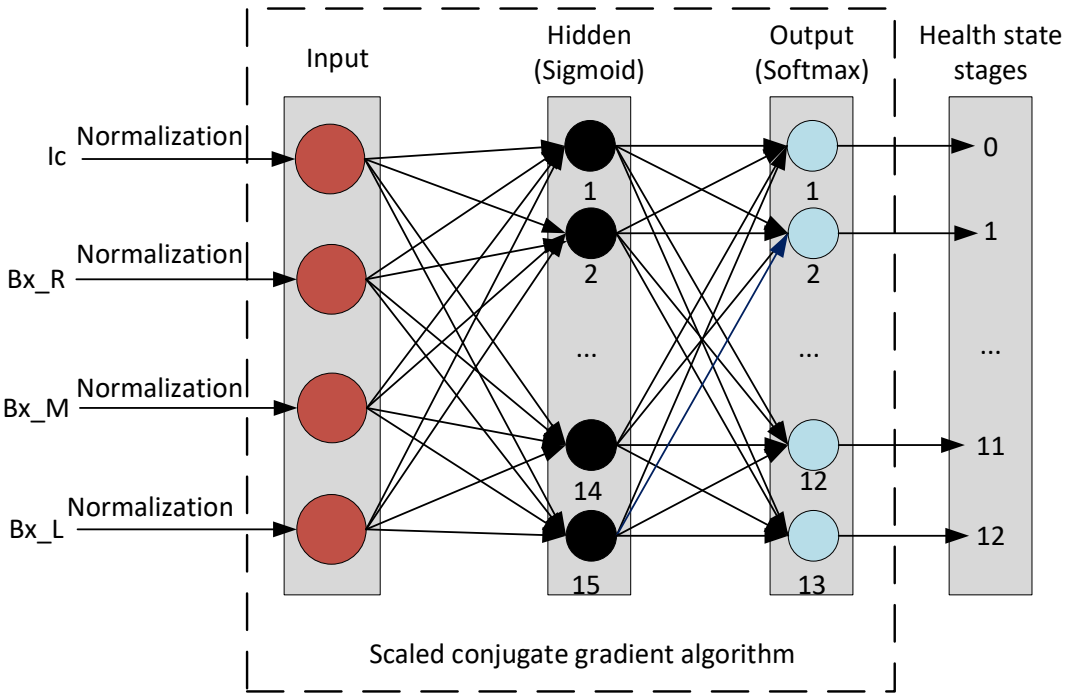


Figure 4-1 Structure of the health state assessment model based on BP neural network.

4.3 Validity Analysis of the Health Evaluation Model

Because the range of operating current is from 150A to 300A, 1054 sets of sample data were extracted from the simulation when the operating current changes from 150A to 300A with an increment of 5A, and the shedding degree changes from 0% to 21% that the corresponding thermal resistance changes from 0% to 20% in each scenario. A total of 738 sets of data are used for training, and the rest data are evenly divided into validation set and test set. The purpose of verification is to ensure the generalization of the network that training is ended before over-fitting, and test is conducted to verify that the generalization of the network is completely independent of training results [134]. The model is set to stop when the cross-entropy error of the training is smaller than 0.0001, the generalization stops improving that there is no drop of the cross-entropy error of the validation data after 6 iterations, or the maximum number of iteration 1000 is reached.

The lowest 87.8% and the highest 99.8% accuracies were obtained in 5 and 15 hidden neurons. When the number of the hidden layer nodes is 13, the model has the best performance with highest 99.8% accuracy. The network with 13 neurons in the hidden layer stops training at maximum epoch of 225 iterations with maximum training time of 2 seconds by reaching maximum 6 validation checks. Figure 4-2 shows the network generates the lowest validation error of 0.0028686 at epoch 219. The curves also indicate good generation ability of the network due to similar value of cross-entropy of train, validation, and test for each epoch. The quality of the network is examined by confusion matrixes shown as follows (Figure 4-3 ~Figure 4-6), and the classification accuracy in training, validation, testing, and overall performance is 99.9%, 99.4%, 100%, and 99.8%, respectively. In addition, the Receiver Operating Characteristic (ROC) which examines the ratio between sensitivity and specificity is used to evaluate classification quality [136]. As Figure 4-7 shows, ROC characteristics of the training, validation, test, and overall performance ROC characteristics all processes a position close to the theoretical descriptive direction with full correct identification (100.00%). Thus, the neural network model with 13 neurons in the hidden layer works well for health state identification.

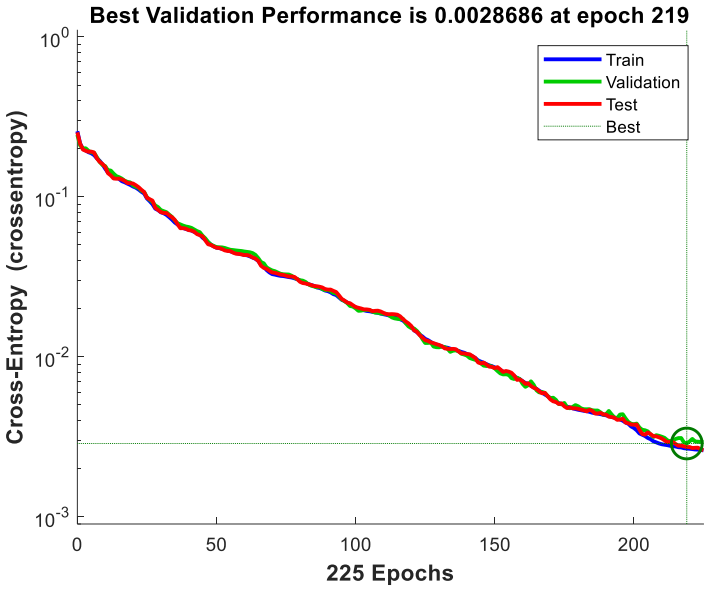


Figure 4-2 Change of cross-entropy for the neural network.

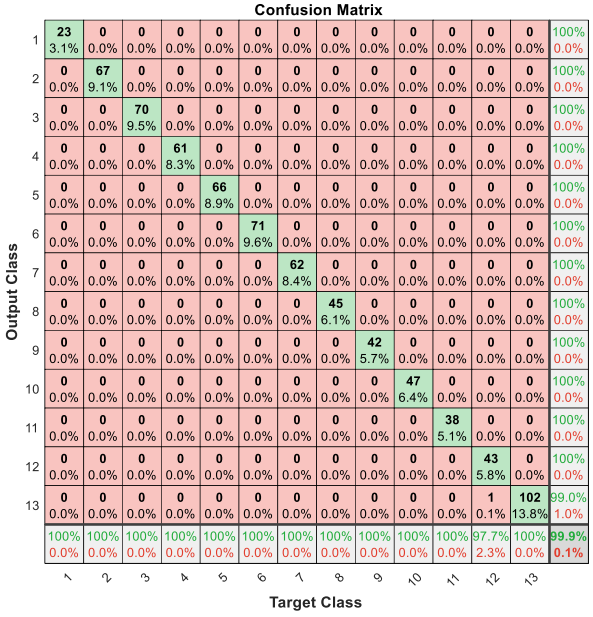


Figure 4-3 Classification accuracy in training.

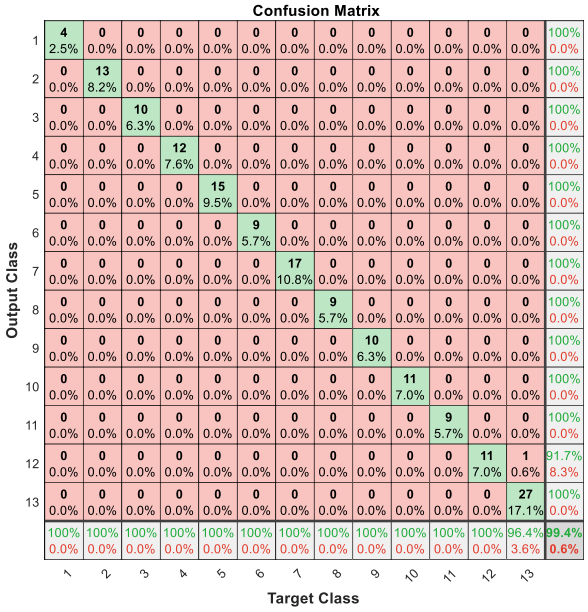


Figure 4-4 Classification accuracy in validation.

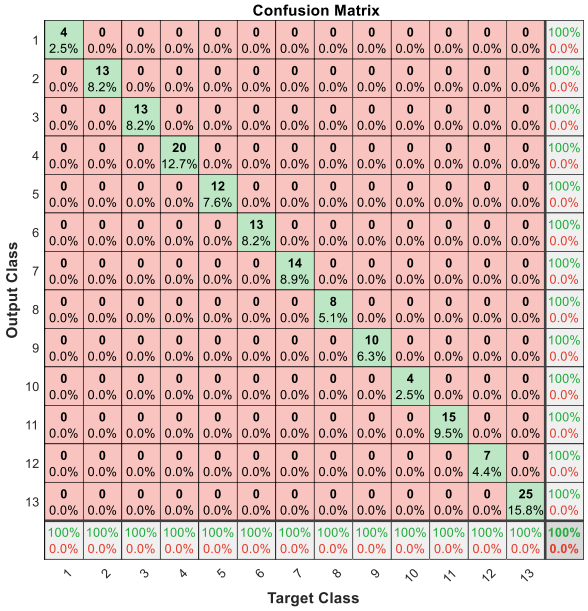


Figure 4-5 Classification accuracy in testing.

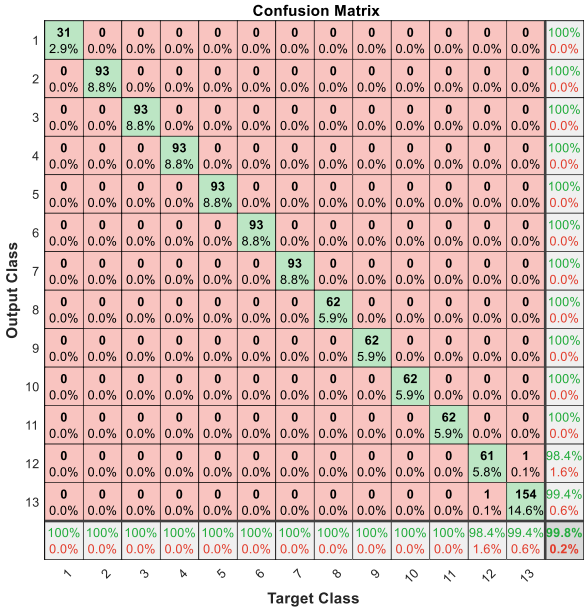


Figure 4-6 Overall classification accuracy of the model.

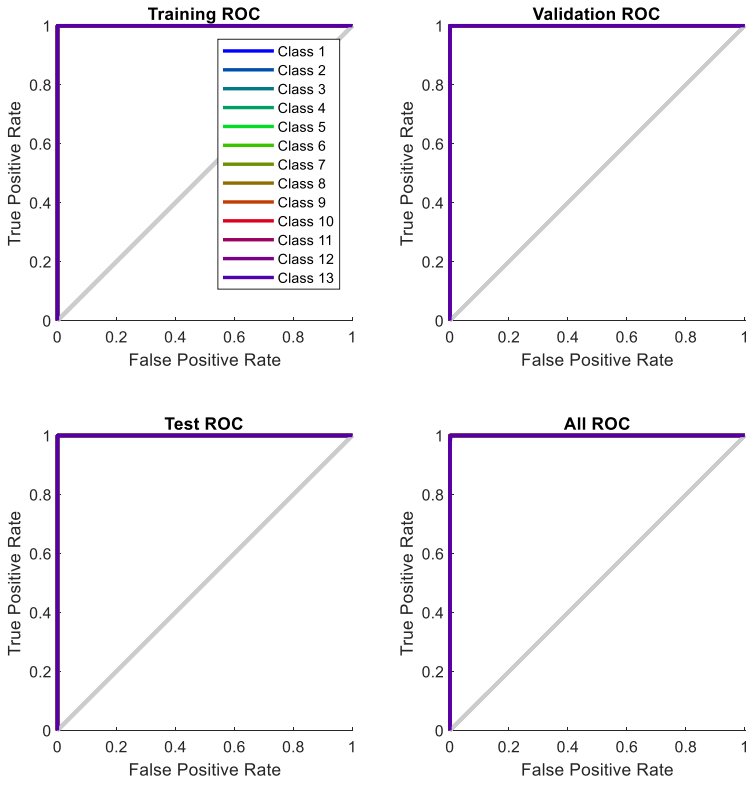


Figure 4-7 ROC curves about the model for health state identification.

The performance of network with different algorithms are shown in Table 4-2. It can be found that the calculation speed and classification accuracy of the standard BP algorithm are obviously inferior to other algorithms. The calculation efficiency of the resilient backpropagation algorithm and scaled conjugate gradient algorithm is significantly improved. The accuracy of the LM algorithm and scaled conjugate gradient algorithm is significantly higher than that of other algorithms. The scaled conjugate gradient algorithm owns great balance between accuracy and calculation speed. Therefore, it is reasonable to choose the scale conjugate gradient as the training algorithm.

Table 4-2 The performance of network with different algorithms.

Training algorithms	Gradient Descent	L-M method	Resilient Backpropagation	Scaled Conjugate Gradient
Iterations	350282	119	410	225
Time	3664s	5s	1s	2s
Accuracy	73.1%	97.1%	96.5%	99.8%

4.4 Summary

Because the relationship between distribution of B_X and corresponding operating current, and fatigue degree is nonlinear, data-drive method instead of model-based method is more suitable to use for health state assessment model. Error backpropagation neural network is the most common type of supervised artificial neural network which normally used in pattern recognition and multi-classes classification for strong nonlinear processing ability and good self-learning, self-adapting, robustness and generalization ability. A health state assessment model based on error backpropagation neural network is proposed to improve the reliability of the module and power electronic system in this chapter.

The structure of the model includes an input layer, a hidden layer, and an output layer. The input layer has 4 nodes for load current and B_X above each chip. The output layer has 13 nodes for 13 classes. The classes include one healthy stage and four aging stages the multi-chip IGBT module. Each aging stage has three possible fatigue scenarios to localize the fatigue and provide corresponding treatment. The number of neurons in the hidden layer is determined according to difference performance of the network with different hidden layer nodes. It can be found that the network with 13 hidden layer nodes has the highest classification accuracy and highly sensitive and specify value with 100.00% correct identification when scaled conjugate gradient is selected as training algorithm.

Compared with other algorithms such as the L-M method and resilient backpropagation method, high calculation efficiency and highest classification accuracy of the scaled conjugate gradient algorithm is also verified in this chapter. It ensures that the health condition assessment model has high speed and accuracy.

Chapter 5 Conclusions and Future Work

5.1 Conclusions

This thesis has identified research gaps in the application of health condition monitoring to multichip IGBT power modules. Consequently, a new failure precursor parameter for identifying the health state of the multi-chip IGBT module has been proposed in this thesis. Multi-chip IGBT modules comprise several IGBT chips within the power module. The increased complexity of multi-chip IGBT power module construction, uneven lay-out of chips, and high-power operating conditions affect the reliability of multi-chip IGBT module.

An Infineon FF450R17ME4 IGBT power modules with 1700 V rated voltage and 450A rated current normally used in wind turbine converter system was used for simulation and experimentation in this thesis. The IGBT power module comprises 6 IGBT chips and 6 anti-parallel diode chips. It is common to have IGBT chips with anti-parallel diode chips within the power module. This research focusses on the health condition of the IGBT chips and ignores the effect of the diode chips because IGBT chips are more susceptible to failures compared with diode chips. IGBT chips experience higher thermal stress compared with diodes due to higher turn-on and turn-off power dissipation, and IGBT chips own a more complex semiconductor structure compared with diodes which makes IGBT chip less reliable.

The selection of failure precursor parameters relies on the knowledge of failure mechanism and external characteristic performance during the degradation. The knowledge of failure mechanism and external characteristic performance for multi-chip IGBT still need to be enhanced though they are clear for IGBT module with single or two IGBT chips. This thesis has recommended electro-thermal finite element model to analyze failure mechanism and external

performance because it can accurately obtain external characteristic performance with consideration of the temperature dependence of electrical resistivity of IGBT chips, thermal coupling effect within the module, and real heat transfer process between the module and the operating environment. An 3D FEM has been built according to actual physic structure and materials of the IGBT module. The electrical resistivity of IGBT chips has been extracted from output characteristic curve, and the resistivity variation of the chip with temperature has been described by linear fitting. All the surface has been set as thermal isolation except the bottom surface of the baseplate to simulate actual heat transfer condition. The chips and bond wires are the main heat source because of through current. The validity of the model has been firstly verified by calibrating the output characteristic curve and transient thermal impedance curve from datasheet. All the simulated curves have showed good consistency with original curves and all errors has been within 5%. Furthermore, the case temperature distribution obtained from the electro-thermal FEM has been closed to the measurement results of the experiment with maximum error 4.07%. Thus, the external characteristic performance got from the electro-thermal FEM is accurate and reliable.

Because chip solder fatigue normally appears earlier than bond wire fatigue at low temperature swings, this research focuses on early aging monitoring of IGBT modules with the chip solder degradation. The junction temperature distribution of the IGBT module at low output frequency of wind turbine has been obtained from the electro-thermal FEM, which has showed the same temperature swings but different steady-state temperature for each chip. The junction temperature of the middle chip is higher than the other two chips in upper leg structure at health state because of thermal effect. It is possible for any chip to age first due to different manufacture quality when the temperature fluctuation is the same.

An increased junction temperature, large change of temperature distribution, and more serious imbalanced current sharing has been found during a single chip solder aging. Temperature of health chip has raised faster as the fatigue degree increases because of rapidly increased P_{loss}. When the chip solder aging appears, the heat transfer path of the aged chip changes and the junction temperature rises, and then the resistance of the chip increases for positive temperature coefficient. The current through the aged chip becomes lower than before due to increased resistance of the chip solder and the chip, and current through other health chips increases. Thus, P_{loss} of health chips increases and the junction temperature of them also increases. As the junction temperature of the module increases, V_{CE} of the module increases. The increased junction temperature can accelerate the fatigue of the module such as bond wire fatigue, and the increase current for health chip increases the electrical stress which can cause failure of the chips.

According to the change of thermal and electrical parameters with chip solder fatigue, the sensitivity of normal used fatigue sensitive parameters (FSPs) has been analyzed. V_{CE} and P_{loss} is not suitable for health condition monitoring because V_{CE} keeps the same for different aging scenarios, and P_{loss} relies on the measurement of other parameters. Ic of the aging chip has indicated highest sensitivity compared with T_j and T_c, which is about 15% increase of original value. However, the current distribution of internal components is inaccessible for direct measurements or visual inspection due to the package. According to the electromagnetic theory, magnetic flux density has been proposed instead of I_c as a new precursor for health condition monitoring in this thesis because it can be measured without contact. Magnetic flux density distribution has been extracted by an electro-thermal-magnetic FEM of the multi-chip IGBT module based on the electromagnetic theory. The magnetic flux density has presented even higher sensitivity than I_c with chip solder degradation from simulation results. In addition, the selectivity

of magnetic flux density has been verified by changing ambient temperature. The magnetic flux density has not been changed with ambient temperature because it is only related with the current. The magnetic flux density can be applied not only for IGBTs but also for other components with current through. Therefore, the magnetic flex density has been selected as the precursor due to better sensitivity, selectivity, and generality.

Finally, a health state assessment model based on backpropagation neural network (BPNN) has been established according to the magnetic flux density distribution. To localize and evaluate chip solder degradation, the health state of the IGBT module is determined by the magnetic flux density for each chip and the corresponding operating conduction current. BPNN has good self-learning, self-adapting, robustness and generalization ability to deal with the nonlinear relationship between the four inputs and health state. A three-layer BPNN model has been built to be trained with trained set samples. The input layer has 4 nodes for load current and B_X above each chip, and the output layer has 13 nodes for 1 healthy state and 4 aging states with three aging scenarios of IGBT module. The number of nodes of hidden layer has been determined as 13 for highest classification accuracy. Experimental results have shown that the proposed model is accurate and effective. The healthy status of IGBT module has been effectively recognized with a total recognition rate of 99.8%. Therefore, it can provide enough accurate reference for the maintenance of IGBT modules.

5.2 Future Work

The proposed method performed well under typical application conditions and can be applied to other devices. However, there are still areas that need to be enriched and improved, and follow-up work can be continued from the following aspects:

1) This thesis verified the sensitivity of magnetic flux density from the aspect of simulation, but there might be error caused by noise for actual measurement. The focus of the next step is to provide an accurate measuring technique for the new precursor.
2) The main research object of the thesis was the chip solder layer, and the research on the bond wire lift-off has not been conducted. The fatigue of the solder layer and the bond wire fall off during the aging process generally both exist after a long-term operation. To evaluate the health condition of the module for a long-term operation using magnetic flux density need to be considered in future work.
3) The research was done under the laboratory condition that the operating condition of the IGBT module was keeping on-state condition. Future work is to demonstrate the representativeness and performance of B_X in actual operating condition with the consideration of switching frequency.

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