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DESIGN, CONTROL, AND DEVELOPMENT OF A MULTILEVEL CONVERTER
MEDIUM VOLTAGE AC TO LOW VOLTAGE DC FOR
FLEET ELECTRIC VEHICLE CHARGE STATION

by

Garry Jean-Pierre

A Dissertation Submitted in
Partial Fulfillment of the
Requirements for the Degree of

Doctor of Philosophy
in Engineering

at

The University of Wisconsin-Milwaukee

December 2021

ABSTRACT

DESIGN, CONTROL, AND DEVELOPMENT OF A MULTILEVEL CONVERTER MEDIUM VOLTAGE AC TO LOW VOLTAGE DC FOR FLEET ELECTRIC VEHICLE CHARGE STATION

by

Garry Jean-Pierre

The University of Wisconsin-Milwaukee, 2021

Under the Supervision of Professor Adel Nasiri

There is a shift in the technology of vehicles from gas and diesel engines to electric vehicles (EVs). Approximately ten million EVs were available globally in 2020 and it is projected that number will reach 145 million by 2030. To power the increasing number of EVs, the number of EV charging stations is growing at a significant rate. In order to provide flexibility and longer driving ranges to customers, the trend is to install DC fast charging stations. These chargers demand high power at low voltage, which our existing electrical distribution system cannot accommodate without major upgrades. Currently, bulky transformers are used to step down to a lower voltage level in order to directly connect to the medium voltage (MV) utility grid. This results in lowered efficiency and increased cost and size of the charging system.

This dissertation formulates a solution to this significant problem. The proposed work addresses the development of a control scheme and multilevel converter for MV AC to low voltage DC intended for fleet EV charging stations. This architecture removes the shortcomings of the existing systems and offers modular structure, scalability, galvanic isolation, and high efficiency. This topology is investigated for a 1 MW system connected to the 13.8 kV AC grid to create 1 kV DC for EV charging. A robust control structure is proposed for voltage balancing and current sharing among various stages of the converter. The converter and high frequency transformer (HFT) are also investigated for the DC/DC conversion. In order to mitigate power

losses, root mean squared (RMS) current minimization and power loss minimization controls are evaluated and the power loss minimization method is found to be superior. A three module single-phase prototype using hardware in the loop (HIL) is developed and tested to verify the viability of the system.

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LIST OF TERMS AND ABBREVIATIONS

| | |
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| AFF active front-end | 10 |
| CHB cascaded H-bridge | 39 |
| CHBML cascaded H-bridge multi-level | 38 |
| DAB dual active bridge | 10 |
| DPS dual-phase shift | 44 |
| EPS extended-phase shift | 44 |
| EV electric vehicle | ii |
| EVSE electric vehicle supply equipment | 14 |
| GO global optimization | 95 |
| HFT high frequency transformer | ii |
| HIL hardware in the loop | iii |
| IGSE Improved Generalized Steinmetz Equation | 91 |
| ISOP input series output parallel | 10 |
| LF Lyapunov Function | 39 |
| LM Lagrange Multiplier | 52 |
| LO local optimization | 95 |
| MBD model-based design | 109 |
| MPC model predictive control | 37 |
| MV medium voltage | ii |
| NPC neutral point clamped | 24 |
| PFC power factor correction | 37 |
| PI proportional integral | 38 |
| PLL phase loop lock | 57 |
| PR proportional resonant | 38 |
| PSO particle swarm optimization | 52 |

| | |
|--|-----|
| pu per-unit | 68 |
| PV photovoltaic | 39 |
| PWM pulse width modulation | 38 |
| RMS root mean squared | iii |
| SMC sliding mode control | 39 |
| SPS single-phase shift | 43 |
| SST solid state transformer | 18 |
| THD total harmonic distortion | 24 |
| TPM trapezoidal modulation | 46 |
| TPS triple-phase shift | 46 |
| TRM triangular modulation | 46 |
| XFC extreme fast-charging | 17 |
| ZCS zero current switching | 46 |
| ZVS zero voltage switching | 42 |

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CHAPTER 1

Introduction

1.1 Trends and Motivations

In 2020, ten million electric cars were globally available on the market, according to an April 2021 report from the International Energy Agency [1]. Although the availability of EVs has steadily grown over the last decade, this accelerated growth was 43% higher in 2020 than 2019 [1]. It is estimated that globally the number of EVs will reach nearly 145 million, or 7% of total the vehicles on the road, by 2030, compared to only 11 million in 2020. EV sales will likely reach approximately 15 million in 2025 and surpass 25 million in 2030. This represents 10% and 15%, respectively, of all road vehicle sales [2]. This growth in EV usage is a result of numerous factors, including climate change, improved technology, government policies, and organizational investments.

The impact of global warming has led to an increased interest in promoting EV use. The climate change crisis has necessitated the need for modernization of transportation away from internal combustion engine vehicles. The need for a drastic reduction in the emission of CO_2 has been an impetus for more leaders of industrialized countries to introduce new policies and programs for increasing the development of EVs. Fiscal encouragements, tax privileges, and more stringent emission standards, as summarized in Table 1.1 [3] - [6], are a few of the measures that have been adopted.

Table 1.1 EV support policies as of 2020

| Country / Region | ZEV Requirement | Fuel economy standards |
|------------------|--|---|
| European Union | Voluntary targets: <ul style="list-style-type: none"> • 2025–2029 = 15% • 2030 = 35% | 95 g CO ₂ /km or 4.1 L/100 km (2021, petrol, NEDC) |
| Canada | British Columbia: Mandated ZEV sale targets: <ul style="list-style-type: none"> • 2025 = 10% • 2030 = 30%, • 2040 = 100% Québec EV credits: <ul style="list-style-type: none"> • 2020 = 9.5% • 2025 = 22% | 114 g CO ₂ /km or 5.4 L/100 km (2021, CAFE) |
| China | EV credits: <ul style="list-style-type: none"> • 2021-2023 = 14-18% | 117 g CO ₂ /km or 5.0 L/100 km (2020, NEDC) |
| United States | California EV credits: <ul style="list-style-type: none"> • 2025 = 22% | 114 g CO ₂ /km or 5.4 L/100 km (2021, CAFE) |

Many of these policies have contributed to a decrease in the total cost of EV ownership, which has been a major driver in the increased demand for EVs. In response to this rising demand, the number of vehicle manufacturers producing EVs has also risen, as have the available styles and models. Fig. 1.1 [7] shows data from the U.S. Department of Energy demonstrating the growth trend in EVs by comparing 2016 and 2021 available models, engine sizes, driving range in miles, and manufacturers.

| Manufacturer | 2016 | | 2021 | | |
|-------------------------|------------------|------------------|--|-------------------------|-------------------|
| | Model | Engine size (KW) | Model | Engine size (KW) | Range /miles |
| Audi | | | e-tron Sportback --- e-tron | 141 / 172 --- 141 / 172 | 218 --- 222 |
| BMW | i3 | 125 | i3 --- i3s | 125 --- 135 | 153 |
| Chevrolet | Spark | 104 | Bolt EV | 150 | 259 |
| Fiat | 500e | 83 | | | |
| Ford | Focus | 107 | Mustang Mach-E AWD --- California Route 1 | 198 --- 216 | 211 / 230 --- 305 |
| Ford | | | Mustang Mach-E AWD Extended | 209 / 216 | 270 / 300 |
| Hyundai | | | Ioniq Electric --- Kona Electric | 100 --- 150 | 170 --- 258 |
| Jaguar | | | I-PACE EV400 | | 234 |
| Kandi | | | K27 | 20 | 59 |
| Kia | | | Niro Electric | 150 | 239 |
| Mercedes-Benz | B250e | 132 | | | |
| Mini | | | Cooper SE Hardtop 2 door | 135 | 110 |
| Mitsubishi | i-MiEV | 49 | | | |
| Nissan | Leaf | 80 | Leaf (40 kWh battery pack) | 110 | 149 |
| Nissan | | | Leaf SV/SL (62 kWh battery pack) | 160 | 215 |
| Nissan | | | Leaf (62 kWh battery pack) | 160 | 226 |
| Polestar Automotive USA | | | Polestar 2 | | 233 |
| Porsche | | | Taycan 4S Perf Battery --- Taycan Perf Battery | 194/280 --- 240 | 199 --- 200 |
| Porsche | | | Taycan Turbo S --- Taycan Turbo | | 201 --- 212 |
| Porsche | | | Taycan Perf Battery Plus --- Taycan 4S Perf Battery Plus | 280 --- 210 / 250 | 225 --- 227 |
| smart | fortwo | 55 | | | |
| Tesla | Model S | 285 | Model S Performance (19" Wheels) --- Model S Long Range | 149 / 276 --- 179 / 186 | 387 --- 405 |
| Tesla | Model X AWD 90D | 193/193 | Model Y Standard Range RWD | 209 | 244 |
| Tesla | Model X AWD P90D | 193/375 | Model 3 Standard Range Plus RWD | 198 | 263 |
| Tesla | Model S AWD | 350/285 | Model Y Performance AWD | 133 / 179 | 303 |
| Tesla | | | Model 3 Performance AWD | 131 / 190 | 315 |
| Tesla | | | Model Y Long Range AWD | 69 / 201 | 326 |
| Tesla | | | Model X Performance (20" Wheels) | 151 / 273 | 341 |
| Tesla | | | Model S Plaid (21" Wheels) | 250 (X3) | 348 |
| Tesla | | | Model 3 Long Range AWD | 131 / 190 | 353 |
| Tesla | | | Model X Long Range Plus | 180 / 189 | 371 |
| Volkswagen | e-Golf | 85 | ID.4 1st --- ID.4 Pro S --- ID.4 Pro | 150 | 250 --- 260 |
| Volvo | | | XC40 Recharge | | 208 |

Fig. 1.1 EV growth comparison for 2016 and 2021

The average driving range of new EVs is increasing at a fast pace and contributing to the appeal of EVs to consumers. The average range of EVs went up from around 60 miles in 2011 to over 250 miles in 2020 [8]. Fig. 1.2 shows driving ranges for some of the top selling EVs currently on the market, with the top performing EV having a range of 400 miles. Most EVs now have the capability to accommodate many travel plans on a single charge.

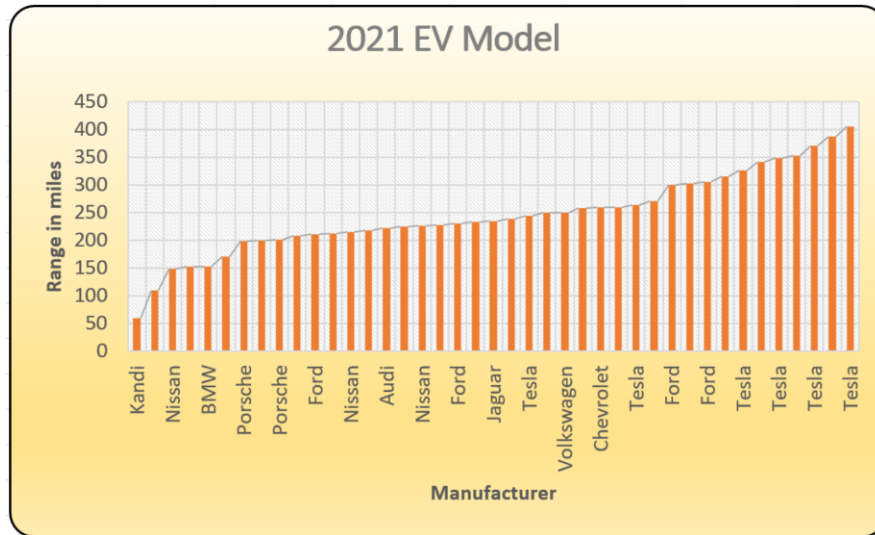


Fig. 1.2 Average range of current EV models

Major organizations around the globe are contributing to the fast transition to electric mobility by adapting fleets to EVs and investing in charging stations. While most of the available chargers are installed at home and work, deployment of publicly accessible chargers will be crucial as EVs are being adopted by both major organizations and the general population. Convenient and inexpensive publicly available chargers are necessary to meet the increasing demand for EVs. To address this, governments have proposed multiple measures, such as direct investment and incentives, in order to meet the demand for EV charging infrastructure development and installation.

To meet the electrification demand of the projected increased number of EVs on the road, more convenient and accessible charging points will be required. With an estimated 9.5 million already in use, privately owned home chargers are the most readily available option for EV owners [2]. Charging stations available to employees at their places of work are becoming more common and can help address the increased demand for EV charge points. However, this requires buy-in and investment from companies. By 2030, the number of private home and workplace chargers are projected to reach approximately 105 million [2]. To meet

long distance travel and accommodate home and workplaces without charging points, publicly available chargers must become more readily available if EVs are to become the norm. It is projected that by 2030, the number of publicly available chargers will reach 14 million level 1 chargers and 2.3 million fast chargers [2].

Fig. 1.3 [9] presents the growth of public and private EV charging infrastructure in the United States since 2011. Both the number of EV supply equipment ports and number of EV charging station locations have steadily increased. The number of charging stations nearly doubled from 2015 to 2019, and in 2020, it grew by 18%.

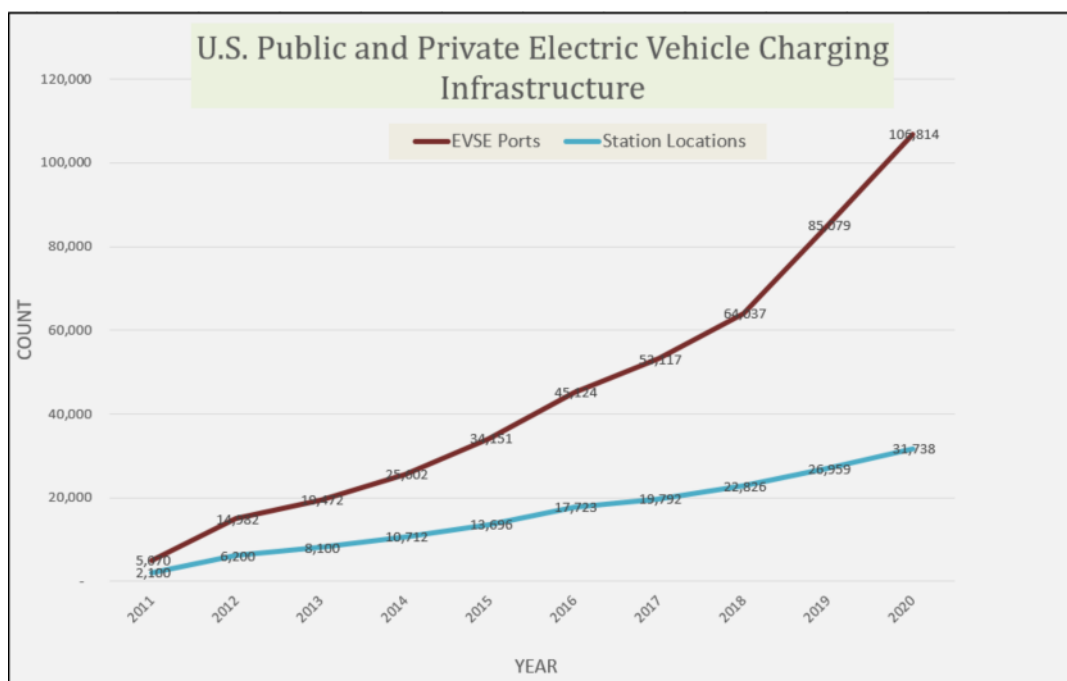


Fig. 1.3 Growth of EV charging infrastructure

Fig. 1.4 [10] shows the trend of U.S. public and private alternative fueling stations by fuel type from 1992 to 2020. Since 2011, there has been over a ten fold increase in the number of EV charging stations. In the recently passed H.R.3684 - Infrastructure Investment and Jobs Act, the U.S. government has committed to building 500,000 charging stations by 2030 [11]. The availability of charging infrastructure that is able to compete with the gasoline refueling

experience by providing short charge times is a necessary step in the complete transition to EV.

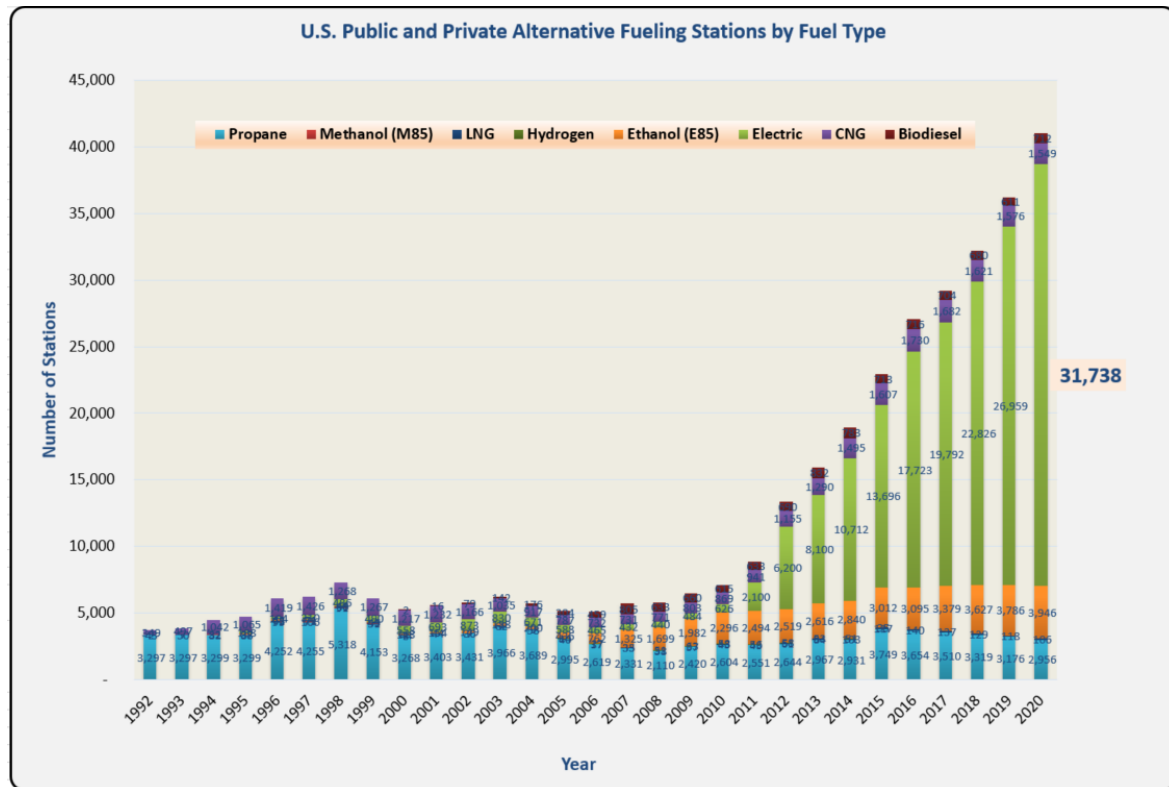


Fig. 1.4 Growth of alternative fueling stations

1.2 Challenges and Opportunities

Reducing energy utilization globally in the transportation branch is crucial for achieving sustainability and gaining independence from fossil fuel resources. Recently, the increase of EV charging capability is serving as an enabler to reach this energy independence goal. However, despite the advancement in charging technology, there are still barriers to achieve a refueling experience comparable in time to that of the internal combustion engine vehicle. Achieving a charge time of 10 minutes or less while increasing the EVs range to greater than 400 miles requires major developments and improvements of the energy density of the cell within battery technology. Some of these developments and improvements are currently underway and being utilized by some EV manufacturers, as can be seen in Fig. 1.2. Although progress is underway,

many challenges and opportunities exist in bringing this technology to maturity.

Enhancing the thickness of the battery electrodes is a successful method of increasing the energy density of a cell. However, thicker electrodes result in longer charge times. Thus, thinner electrodes are more applicable for ultra fast charging. This necessitates the use of more cells to achieve the desired energy density, resulting in increased battery system total cost.

To achieve ultra fast charging in less than 10 minutes, charging architectures must be capable of supplying up to 400 kW, and EVs must be suitable to accept the high level of electrical charge. This presents numerous challenges. The required high current can have significant impacts on the components of the vehicle's electrical system. To mitigate this, a recent strategy has been focusing on doubling the battery voltage, which also affects the rating of the onboard power electronic converter and the motor drive systems. The increased voltage level also affects the system configuration, requiring a more sophisticated thermal management system.

Successful adoption of 400 kW ultra fast chargers requires coordination among all collaborators, including grid utility operators, EV corporations, battery designers, fast charger companies, governments, cybersecurity experts, and standard governing groups. Considerations for voltage level and power demands for ultra fast chargers, connectors, installation locations, and price of electricity can influence the implementation of ultra fast chargers. Therefore, many keys opportunities for successful implementation of EV ultra fast chargers exist:

Electrical Design

- Analysis of effects from increasing battery voltages on different parameters, including cost, weight, and volume of the EV-capable fast charger
- Investigation into insulation coordination requirements to meet the high current and voltage design
- Study of trade offs and impacts of fast charge rate on battery life, EV range, and charge

time

Semiconductor Devices and Electric Drives

- Development of connectors and semiconductor modules for high power and voltage application for the automotive industry
- Magnetic, motor, and insulation design methods to accommodate high power and voltage systems
- Thermal consideration for the overall system

Interoperability and Network Protection

- Research and implementation of secure communication between EVs and chargers for reliable transportation
- Evaluation of various charging protocols to understand their limits in fast charger application
- Establishment of common standards to ensure both new and older EVs are able to connect with any fast charging network

[12]

1.3 Research Objectives and Contributions

Transitioning from gas and diesel engine vehicles to EVs has become a global trend. Approximately ten million EVs were available globally in 2020 and it is projected that number will reach 145 million by 2030 [2]. Accordingly, the number of EV charging stations is growing at a significant rate to meet the demand. The trend is to install DC fast charging stations to provide

flexibility and longer driving ranges to customers. These chargers demand high power at low voltage, which the existing electrical distribution system cannot accommodate without major upgrades. Currently, in order to directly connect to the MV utility grid, bulky transformers are used to step down to a lower voltage level, thus lowering efficiency and increasing cost and size.

This dissertation formulates a solution to this significant problem. The proposed work addresses the development of a control scheme and multilevel converter for MV AC to low voltage DC intended for fleet EV charging stations. This architecture removes the shortcomings of the existing system and offers modular structure, scalability, galvanic isolation, and high efficiency. This topology was investigated for a 1 MW system connected to the 13.8 kV AC grid to create 1 kV DC for EV charging. A robust control structure was proposed for voltage balancing and current sharing among various stages of the converter. The converter and HFT were also investigated for the DC/DC conversion. In order to mitigate power losses, RMS current minimization and power loss minimization controls were evaluated and power loss minimization was found to be superior. A three module single-phase prototype was developed and tested to verify the viability of the system.

1.4 Dissertation organization

This study is structured in 7 chapters. This first chapter presents the trends and motivation for this work, the challenges and opportunities in achieving full implementation of fast charger technology, and the scientific contributions of this dissertation.

The second chapter is focused on different charging technologies that are currently trending for EV charging. A brief overview is presented of currently used charging methods, including wireless and conductive charging, and the battery swapping method. This chapter ends with a

discussion of slow to fast chargers.

In the third chapter, power converters that are suitable for EV fast charging are discussed. An overview of fast charger architectures is presented, followed by discussion of different power converter topologies. This chapter ends with the presentation of the topology selection for this work.

The fourth chapter includes a literature review of the selected topology. Discussion includes system and components design, existing control methods for active front-end (AFE) AC-DC and dual active bridge (DAB) DC-DC topologies, and optimization schemes for the DAB converters.

The mathematical derivation and control analysis for this work are presented in chapter five. The first section presents the proposed controller derivation for the AFE side. The analysis of the proposed controller of the AFE is introduced in the second section. The third section contains the loss analysis of the AFE. The fourth section presents mathematical derivations and the analysis of the second stage of this system, the input series output parallel (ISOP) DAB converter. The operating regions for the DAB, analytical expressions for the RMS currents based on the operating regions, optimization strategy, and control structure are also discussed in the fourth section. Section five of this chapter presents the mathematical expression for the loss characterization of the DAB converter. The optimization techniques are presented in section six. Section seven contains the HFT design and optimization.

Chapter six of this work presents the simulation and experimental results and the validation approach. In the first section, the model based design approach is presented, followed by the simulation results for both the AC-DC and DC-DC stages in section two. The third section discusses the overall system loss analysis. Sections four and five present the HIL setup and obtained results for both stages of the system.

Finally, the seventh chapter gathers the conclusions drawn from the research work developed in this dissertation and proposes areas for future work.

CHAPTER 2

Charging Technologies

2.1 Overview

The recent research, development, and commercialization of EVs is an important step toward the goal of creating sustainable, smart cities with little to no pollution. New standards for EV manufacturers will require them to overcome many challenges, including the development of a high performance battery and a suitable EV charger, while keeping vehicle costs to a minimum.

The increased consumer demand for EVs has generated a thriving market for fast and convenient charging station services. Currently, EV charging methods are primarily carried out by three well-known charging technologies, including at home charging, workplace charging, and public charging stations. These charging technologies are categorized as conductive charging and can be divided into three levels, depending on their power ratings and charging time capabilities. The conductive charging method is suitable for all power levels.

The inductive charging method is another method used for low power transfer, but is less suitable for high power and fast charging capability. Before gaining feasibility for mainstream charging, this method has numerous hurdles to overcome, including low efficiency, coil misalignment, high power transfer capability, and communication latency.

The battery swapping method is primarily applicable for public transportation, such as buses and taxis. This method can be beneficial for grid operators, but battery usage and large

scale battery swapping station deployment remain obstacles to overcome. This chapter presents an overview of the different charging methods, the currently available standards, and the different charging levels currently available.

2.2 Charging Methods

The growing use of EVs presents challenges to the electric power grid. Plug-in EVs introduced a new set of non linear load demands which the power grid needs to be able provide. Therefore, it is paramount to develop new charging methods and technologies to alleviate this burden and to efficiently integrate EVs into the power system network. Charging methods have been classified into three main categories: wireless charging, conductive charging, and battery swapping. The most common method is conductive charging, which provides energy to EVs via a direct wired connection from the electric grid. Wireless charging, also known as inductive charging, uses magnetic fields to provide energy to the EVs. The battery swapping technique involves replacement of a discharged EV battery with one that is fully charged. Fig. 2.1 shows the breakdown of the different charging methods.

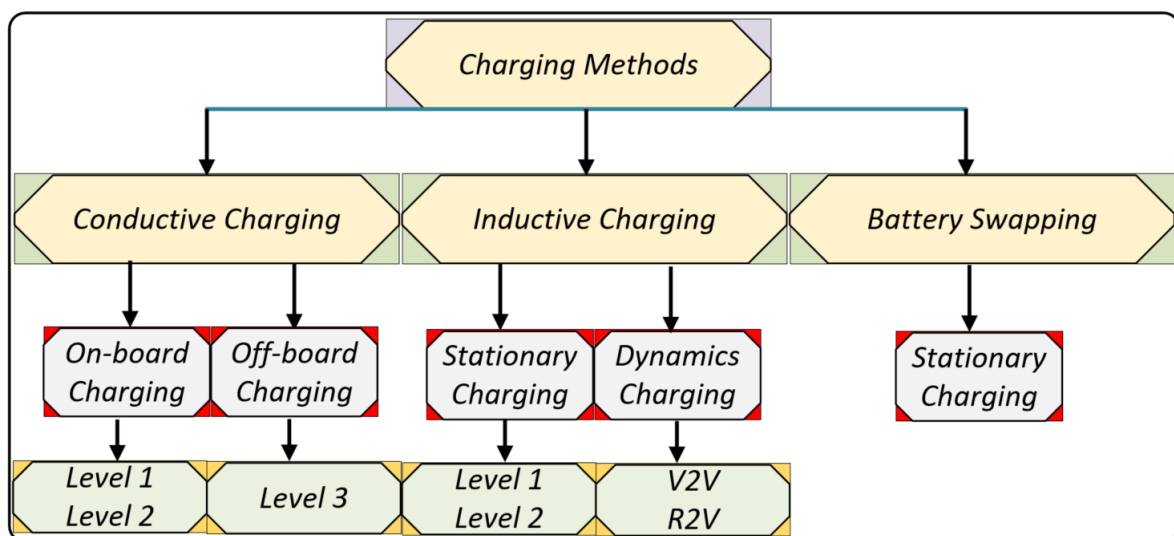


Fig. 2.1 EV charging methods

2.2.1 Wireless Charging

Wireless charging technology is a direct result of electromagnetic induction theory. This charging method removes the need for a wired connection between the charging station and the vehicle. Wireless charging requires the use of two coils: one placed at the surface of the charging station for transmitting energy and the other inside the EV for receiving energy. This transmission can occur either while the EV is stationary or dynamic. Dynamic wireless charging was developed to enable cars to charge while driving, resulting in an increased battery range. There are two methods to accomplish this. Road-to-vehicle charging is achieved by placing charging coils on the road for transmitting energy to the battery during motion [13] and [14]. This is denoted as R2V in Fig. 2.1. The other method is known as vehicle-to-vehicle charging. This method for charging via a designated charging vehicle is under investigation and is presented in [15]. It is denoted as V2V in Fig. 2.1.

Although inductive power transfer is convenient for consumers, there are drawbacks. During wireless power transfer, the efficiency is comparatively low, the required air gap range is narrow, and there are limitations on the power that can be transferred [16]. Coil misalignment and communication latency between the transmitter and receiver can contribute to inefficient power transfer [14] - [18].

There are numerous published standards for charging EVs using wireless power transfer. The SAE J2954 created worldwide standards for both charging EVs and electric vehicle supply equipment (EVSE) using wireless power transfer technology. These standards allow light duty EVs and infrastructure to operate safely at up to 11kW with an air gap of 250 mm, and to achieve an efficiency of up to 94%. They also establish an 82.8 dBuA/m EMI limit recommendation for the operating frequency range of 79.00 to 90.00 kHz [19].

SAE J2954/1 is the charging standard for light-duty vehicles. Based on the charging power

level, this standard is divided into numerous subcategories. WPT1 is established for 3.7 KVA maximum power transfer supplied by a 120V AC source. WPT2 is dedicated for a power level of 7.7 kW supplied by 240 V AC source. WPT3 presents a step up of WPT2 to 11.1 kW. WPT4 is established for a power level of 22 kW supplied by a 240 V three-phase AC source [19]. SAE J2954/2 is being developed for power levels in the range of greater than 22 kW to 150 kW, which is applicable for heavy duty vehicles supplied by 208V AC three-phase, 480V AC three-phase, or MV. SAE J2847/6 provides guidance on communication for wireless power transfer between light-duty plug-in EVs and wireless EV charging stations [19].

2.2.2 Battery Swapping

In order to achieve a charging time approximately equal to the internal combustion engine refueling time, battery swapping stations have incrementally gained attention by EV owners. Aside from faster refueling, these battery swapping stations may provide other advantages, including convenience, improvement of the battery recovery rate, increased battery utilization ratio, and participation in power regulation [20]. This method can be advantageous to the utility grid by reducing the load stress on the grid through optimization of the timing of battery charging. Battery swapping operators can take advantage of the integration of renewable energy sources to the system for planning charging times, which can result in decreased carbon emissions and improvement in the efficiency and stability of power grid [20] - [22].

2.2.3 Conductive Charging

The conductive charging method utilizes a direct connection between the vehicle and charger via a cable or connector. This is currently the basic and most popular infrastructure for EV charging stations. This method can be classified as on-board charging or off-board charging, depending on the power level. These power levels are discussed in greater detail in the Charging

Levels section below. In contrast to the other charging methods discussed, conductive charging provides higher efficiency, faster charging time, and greater availability around the world. Conductive charging allows vehicle-to-grid interaction, which can assist in maintaining the voltage level of the grid, reducing loading stress on the power system, and providing real power support and reactive power compensation [23].

2.3 Charging Levels

EV chargers can be classified as either on-board or off-board. On-board chargers are mainly used as home chargers and only provide charging power under 100kW [24]. The main disadvantage of these EV chargers is their long charging time. The off-board chargers, which are typically DC system based, have the capability to fully charge an EV battery in ten minutes or less. However, in order to have a practical ultra-fast EV charger located in a rural area, a strong grid is required. Typically, the ultra-fast EV charger is composed of a filter, an AC-DC rectification, a power factor correction, and a DC-DC converter into which the power factor correction may be integrated. Three standard charging levels are used to charge EVs. Level 1 and level 2 stations, which utilize lower charging power and require longer charge time, are the most common. These are typically installed in homes, offices, or public places. Level 3 chargers, also known as fast charging stations, provide more power at a faster rate and are typically installed in public places.

2.3.1 Level 1

Level 1 chargers are an on-board battery charging technology which was developed primarily for residential charging. For this type of charging level, only a 120V single-phase connection is required and the EV can be connected directly to the AC outlet. All power conversions are

integrated into the EV for the AC-DC conversion. Users typically charge their EV overnight, which is the ideal time for reducing stress on the power grid. This charging method is slow and can provide approximately a 40 mile range for 8 hours of charge. The majority of plug-in EVs are integrated with a Level 1 connector, which is a standard NEMA connector for the outlet side, and an SAE J1772 standard connector for plugging into the charge port of the car [25].

2.3.2 Level 2

Level 2 chargers are another type of on-board battery charging technology. This type of charger was developed primarily for commercial battery charging and utilizes the three-phase 208V/240V connection system. These chargers can also be used in residential spaces, however, they require installation of additional 40A electrical circuit equipment. In contrast to level 1 chargers, level 2 chargers provide faster charging rates up to 80A and 19.2 kW. When they are used in residential spaces, they operate at a lower power rating of 30A and 7.2 kW. The increased power transfer rate equals a shorter time for charging the EV. Level 2 chargers can provide approximately 10 to 20 miles of range for each hour of charge, compared to the 2 to 5 miles of range level 1 chargers achieve each hour of charge [25]. Similar to level 1 charging technology, the J1772 connector can be used for level 2 as charging equipment.

2.3.3 Level 3

The increasing number of EVs has created a need for more suitable charging infrastructure with shorter charging times. The prominent extreme fast-charging (XFC) technology offers a charge time comparable to the time needed to refuel a traditional combustion engine vehicle. The state-of-the-art DC fast-charging stations are connected to the three-phase 480V low voltage distribution feeder up to 13 kV MV power grid. This connection is usually achieved with the use of a bulky low frequency transformer, which increases the size and cost of the system. To

mitigate the need for this bulky low frequency transformer, power electronics-based solid state transformers (SSTs) have been introduced to directly interface the MV grid. This configuration provides numerous advantages, including more control flexibility, lower footprint, better current control, and higher efficiency [26].

The level 3 charger is divided into three subcategories based on the power level. The most widely available is the 50kW 480V fast charging station, which is capable of providing approximately a 2.92 mile range per minute of charge. The second category includes the range of greater than 50kW and less than 300 kW. The Tesla Supercharger falls in this category. It is rated at 480V and 140kW and is capable of providing a range of 8.17 miles per minute of charge. The last category is ultra-fast charging, which operates at 800V and 400kW. For each minute of charge, the user can travel up to 23.3 miles [24].

To prevent mismatch, various organizations have established standard protocols and connectors for DC fast charging systems. There are currently five standards for DC fast charging structures, as seen in Table 2.1. The IEC 62196-3 establishes the standard for connector configuration [27]. Tesla, Inc. has also developed its own proprietary system which is only used for Tesla cars. In ultra-fast chargers, two main considerations exist for supplying power to the EVs; the corresponding EV battery must be rated for the charger and the connector must be able to carry the high current. From Table 2.1, it can be seen that the CHAdeMO standard has the highest rated current and thus, has the highest power capability. Multiple EV charging standards are used globally for EV charging infrastructure. In the U.S, the IEEE and SAE standards are used, in Japan and Europe the CHAdeMO standard is used, and in China the GB/T standards are utilized.

Table 2.1 DC fast charger standards

| | | | | | |
|---------------|---|-----------------------------|--|---------------------------|-------|
| Standard | CHAdemo IEEE 2030.1.1 IEC 62196-3 | GB/T 20234.3 IEC 62196-3 | CCS Type 1 SAE J1772 IEC 62196-3 | CCS Type 2 IEC 62196-3 | Tesla |
| Configuration | AA | BB | EE | FF | |
| Power (kW) | 400 | 120 | 150 | 175 | 135 |
| Voltage (V) | 1000 | 1000 | 600 | 1000 | 410 |
| Current (A) | 400 | 250 | 200 | 200 | 330 |

To fully integrate EVs to the market, remarkable advancements have been made in battery performance and range, and charging time reduction. Level 3 ultra-fast chargers have been developed utilizing these advancements and offering numerous advantages. XFCs can alleviate the need for level 1 and 2 chargers for home charging and reduce stress associated with unplanned long distance travel. The high power charging and discharging rates can provide more practical regenerative braking due to its capability to accelerate or decelerate faster than gas power vehicles. Additionally, a longer battery range translates directly to more traveling at a lower cost. A well structured analysis was carried out in [28] comparing the travel time of gas power vehicles to different level 3 EV chargers and is presented in Fig. 2.2 [28]. It can be seen that the travel time for a long distance road trip for a 400kW XFC EV and an internal combustion engine vehicle is approximately the same.

Level 1 and 2 on-board chargers use 120V and 240V AC input and can provide a maximum output power of 1.9 kW and 19.2 kW, respectively. As a result of their low power capability, these chargers are more applicable for overnight or workday charging. The limited power ranges of level 1 and 2 chargers have activated the need for a faster and more convenient charg-

ing method. This has led to the development of DC fast chargers, which can typically provide output power in the range of 50 kW to 400 kW.

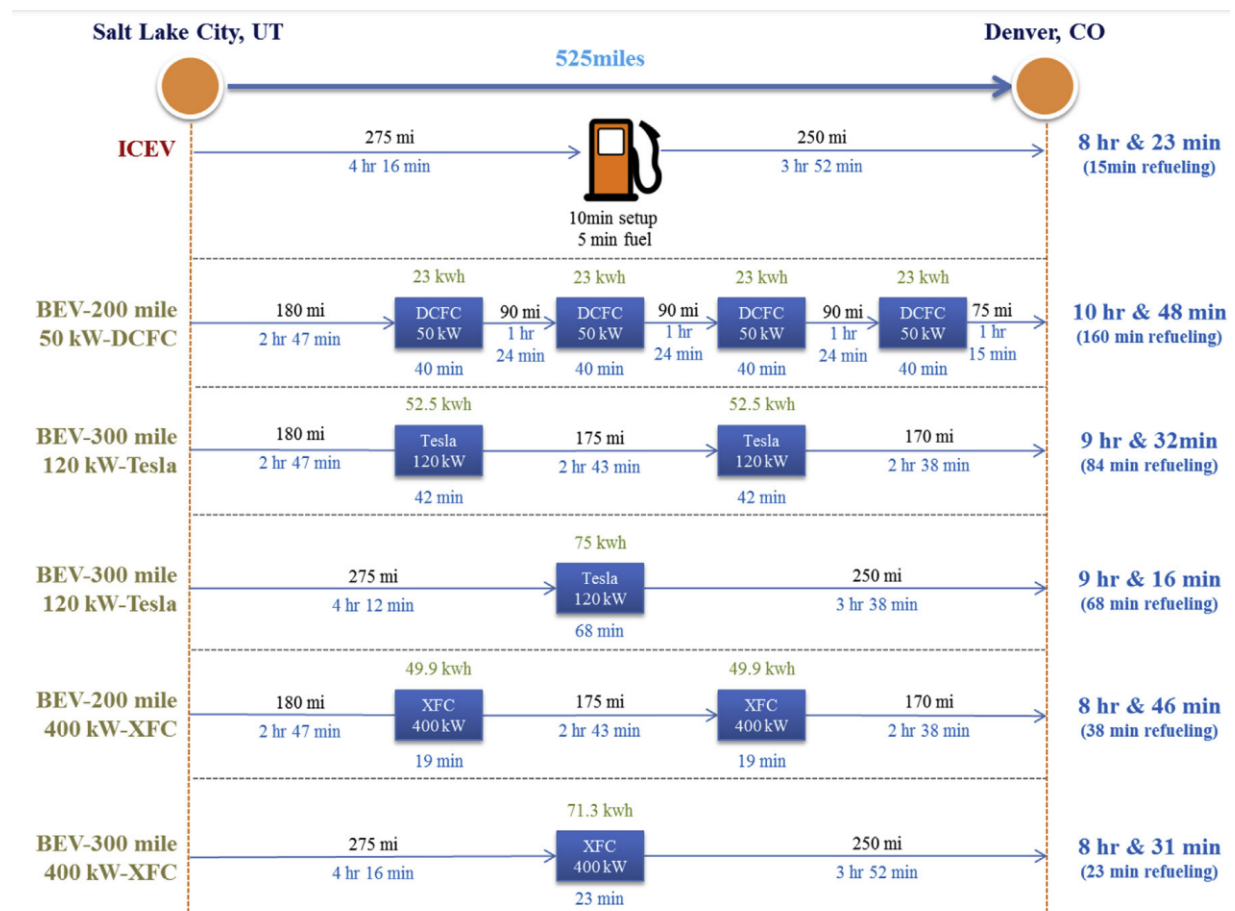


Fig. 2.2 Intercity travel from Salt Lake City to Denver

CHAPTER 3

Power Converter Topologies for EV Fast Charging

The development of faster and more efficient charging infrastructure is necessary to accommodate the growing demand for EVs. XFC technology is one method that has been employed to address this need. Utilizing this technology, EVs are able to charge in a time comparable to the time needed to refuel a gas powered vehicle. These state-of-the-art DC fast charging stations are connected from the three-phase 480V low voltage distribution feeder up to the 13 kV MV power grid. Bulky low frequency transformers traditionally have been used to step down the MV to low voltage, increasing the size and cost of the system. Power electronics-based SSTs have been introduced to overcome the cost, inefficiency, footprint, and size of the system and can enable direct interface to the MV grid. The use of SSTs also allows for improved control flexibility and better current control.

3.1 Fast Charger Station Architectures

AC bus and DC bus configurations are the two possibilities for EV charging station architecture [29]. The AC bus architecture utilizes the secondary side of the medium to low voltage step-down transformer, to which the loads and renewable energy systems are connected to the bus through multiple AC-DC converter stages. Conversely, the DC bus uses one AC-DC stage to establish a common DC bus for loads and renewable energy systems. Fig. 3.1 and Fig. 3.2

show these two common architectures.

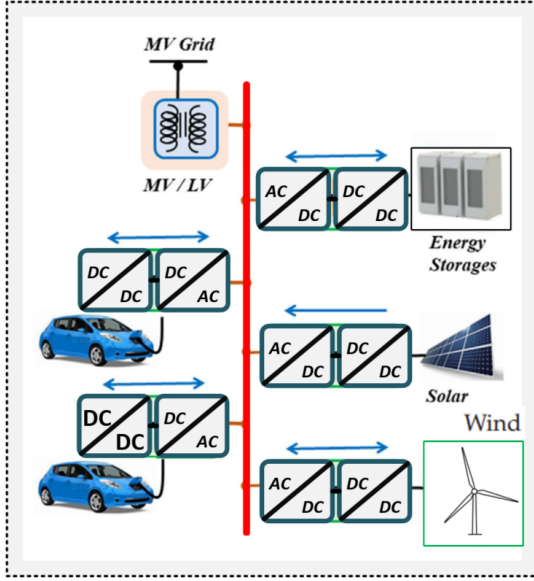


Fig. 3.1 AC connected architecture

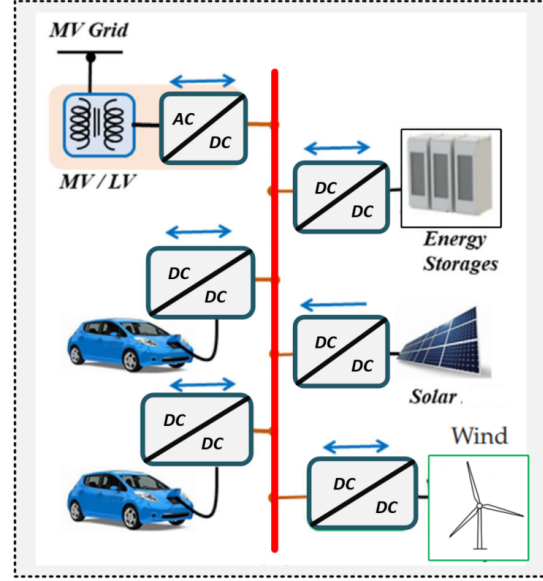


Fig. 3.2 DC connected architecture

Each architecture has both benefits and disadvantages. The AC system requires more AC-DC conversion stages, while the DC system uses only one stage for AC-DC conversion. More conversion stages are directly related to higher power losses and more complex control systems. However, the protection scheme for the AC system is less complex than that of the DC system. The AC bus configuration provides low power nodes, which is beneficial in terms of implementation and availability of both power and protection devices. However, due to its multiple conversion nodes, the power factor of the system can potentially degrade and affect the grid voltage. The DC bus architecture requires only one AC-DC converter at the front end stage to provide a common DC bus. This configuration provides a more compact and efficient technique for connecting the energy storage and renewable resources. The removal of the AC-DC stage decreases the footprint and increases the efficiency of the system in comparison to that of the AC bus configuration. According to [30], elimination of the reactive power control in the DC bus configuration helps decrease the control complexity. Despite its many benefits, DC protection and metering represent some of the challenges of the DC bus system.

3.2 Power Converter Topologies

Several isolated power converter topologies suitable for SST applications are presented in the state-of-the-art. They can be classified into non-modular and modular AC-DC converter structures for connecting to the MV grid and providing low DC voltage output. Four converter configurations are possible for non-modular topology. These are based on the number of conversion stages and are depicted in Fig. 3.3 - 3.6. Multiple SST-based EV charging stations are derived from modular structures to ensure scalability, higher efficiency, higher power density, and lower foot print.

3.2.1 Non-modular AC-DC Converters

The conventional two-level or three-level three-phase AC-DC converters have been well established in low voltage applications. However, they are not capable of sharing AC voltage for forming multiple modules. In order to interface the MV grid, extend the voltage blocking capability, and increase the power level, semiconductor devices can be connected in series. Fig. 3.3 - Fig. 3.5 depict the general three-phase arrangement for non-modular AC-DC converters with galvanic isolation. However, these configurations can be bulky due to the increased number of power devices, passive components, and gate drivers at the AC-DC stage needed to meet the voltage requirement. The recent development of SiC MOSFETs that are capable of blocking voltages up to 15 kV have enabled the use of single module converter topologies to be directly connected to the MV grid. Fig. 3.6 shows an example configuration for a two-stage single module. This type of configuration can significantly decrease the topology and control complexity of the system and increase the reliability and efficiency of the converter. For a two-stage three-phase power conversion system, such as the configurations of Fig. 3.3 and Fig. 3.5, a non-isolated AC-DC converter using multiple power devices connected in series to form a

multilevel converter can be used to connect to the MV grid.

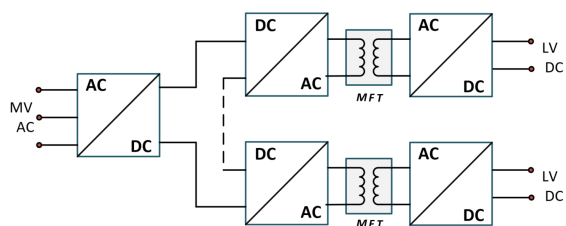


Fig. 3.3 Two-stage isolated AC-DC system with LV DC outputs

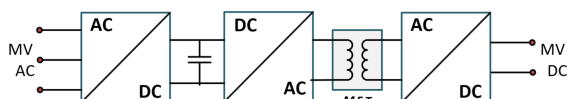


Fig. 3.5 Two-stage isolated AC-DC system with MV DC output

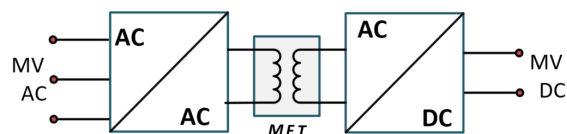


Fig. 3.4 Single-stage isolated AC-DC system with MV DC output

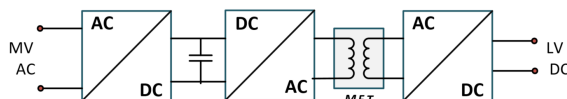


Fig. 3.6 Two-stage single phase isolated AC-DC system with LV DC output

3.2.2 Two-Stage Topologies

3.2.2.1 AC-DC Converters

Three of the widely used multilevel AC-DC converters for MV integration are the neutral point clamped (NPC) converters, presented in Fig. 3.7 and Fig. 3.8 [31] -[34], the multilevel diode-clamped converter, as seen in Fig. 3.9, and the flying capacitor multilevel converter, as seen in Fig. 3.10 [35] - [39]. These converter configurations enable the use of low voltage devices connected in series in each leg to achieve multilevel voltage for reducing dv/dt and current total harmonic distortion (THD). Additionally, NPC converters have the capability of creating a bipolar DC bus [40] and [41]. This capability was explored in [42] and [43] for implementing chargers with a bipolar DC bus. Implementation of a bipolar DC-DC bus generates the opportunity for partial power converters to be used at the DC-DC stage.

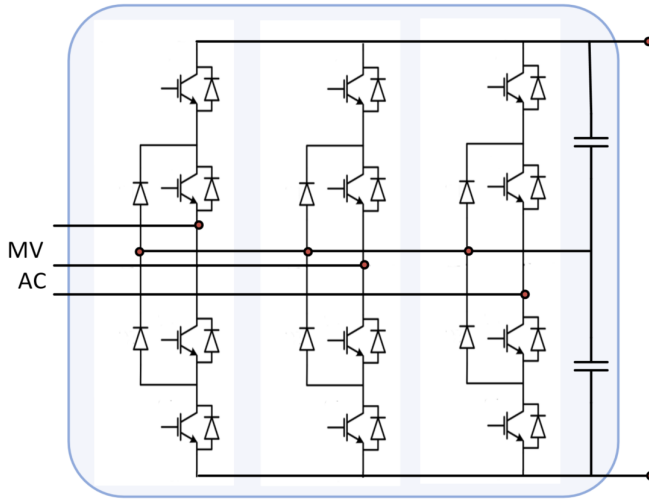


Fig. 3.7 NPC converter

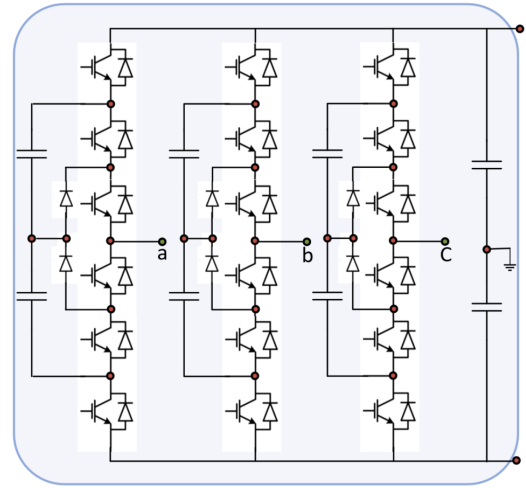


Fig. 3.8 Multilevel NPC converter

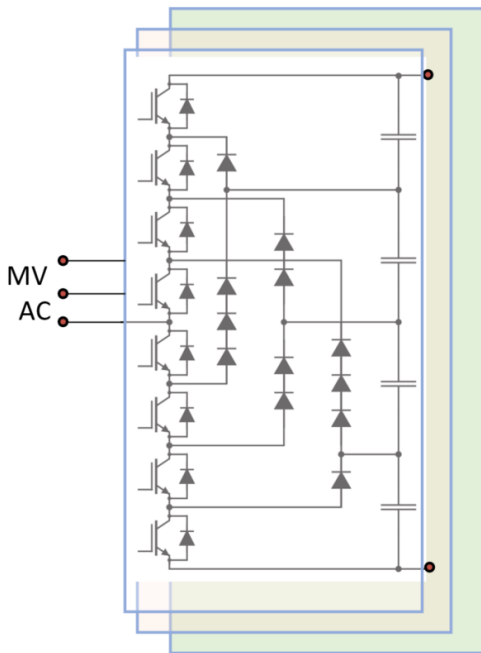


Fig. 3.9 Five-level diode-clamped converter

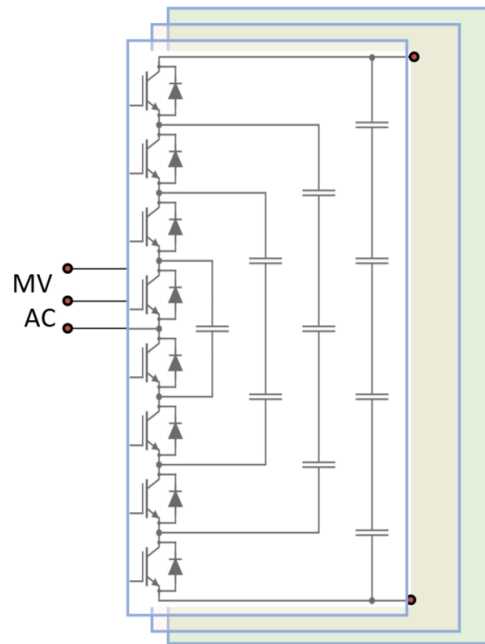


Fig. 3.10 Five-level flying capacitor

The recent breakthrough in high voltage SiC MOSFETs which are capable of blocking voltages in the range of 3.3 to 15 kV have facilitated the direct integration of power electronics to the MV grid by using single module converters, as seen in Fig. 3.6. These advances have significantly decreased the complexity of the multilevel systems and increased the system reliability and efficiency. A single 10 kW module based SST was presented in [44] and [45]. This

converter was designed and implemented for interfacing the 3.6 kV MV AC to generate 6 kV DC bus voltage. The AC-DC rectifier was designed using a single H-bridge with an LCL filter to provide better grid current attenuation. The isolated DC-DC stage was designed as a dual active half-bridge converter using 13 kV SiC MOSFETs on the primary side of the transformer to provide 400 V on the secondary side using low voltage power devices. Fig. 3.11 shows the configuration of this single module converter. Another single module based SST was presented in [46] and [47] for interfacing the 3.8 kV MV grid to provide 400 V DC output bus voltage. The AC-DC full bridge rectifier provides an intermediate DC link of 7 kV bus. Similar to [44] and [45], an LCL filter was used to filter out the grid current, resulting in a reduction in THD. However, extra passive components were added between the legs of the full bridge rectifier in order to achieve higher switching frequency in the range of 35 to 75 kHz. In contrast to the converter presented in [44] and [45], the isolated DC-DC stage was built using an LLC resonant converter with a half-bridge high voltage SiC MOSFET on the primary side of the transformer. Fig. 3.12, shows the configuration of this single module converter.

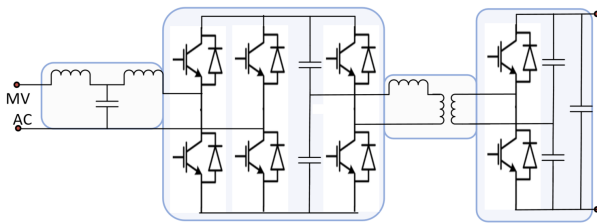


Fig. 3.11 3.6 kV 10 kW XFC

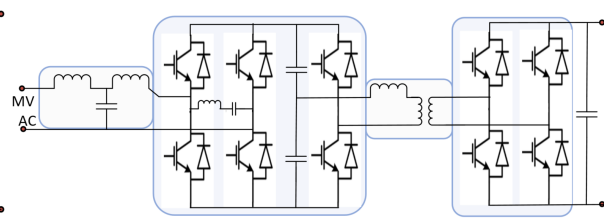


Fig. 3.12 3.8 kV 25 kW XFC

3.2.2.2 Isolated DC-DC Converters

In addition to the AC-DC stage, an isolated DC-DC conversion is added to achieve both galvanic isolation and low or medium DC voltage on the output. The two most used topologies for this application are DAB and resonant converters. Due to their capability to be used in either buck or boost operation modes and operate at high power density and high efficiency, these

converter topologies are used for EV charging applications [43].

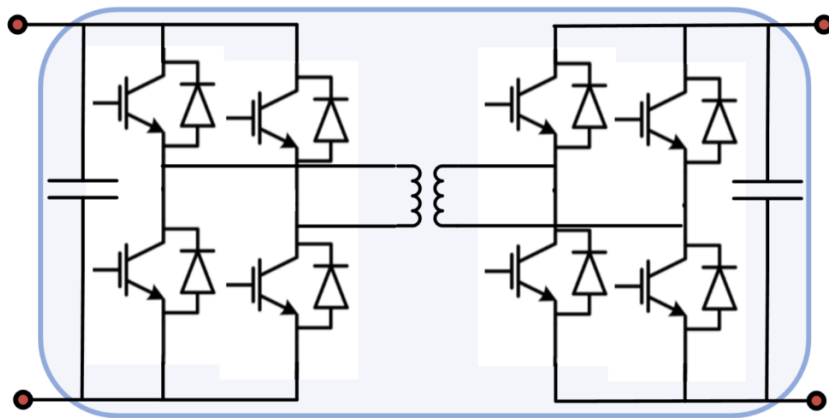


Fig. 3.13 Single-phase level DAB

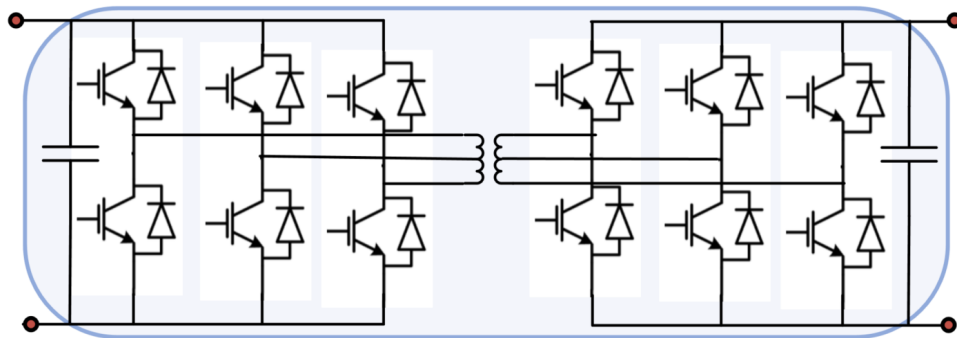


Fig. 3.14 Three-phase DAB

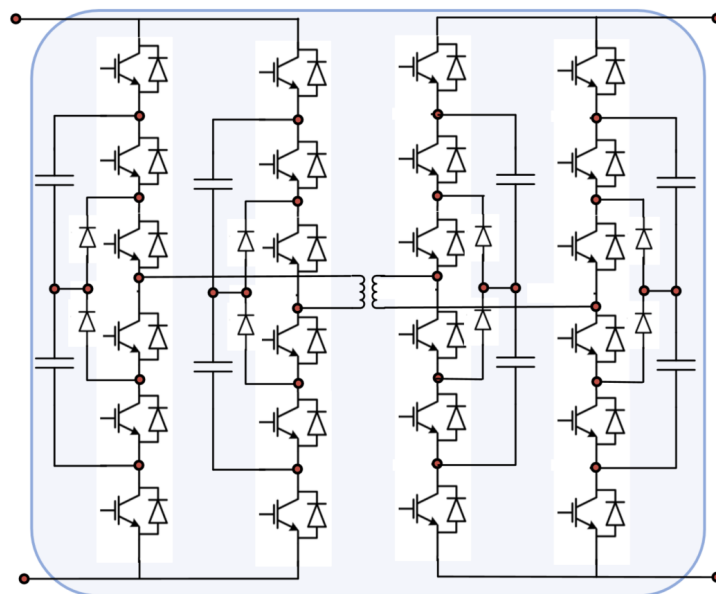


Fig. 3.15 Multilevel DAB

The most well-known topologies are shown in Fig. 3.13 - Fig. 3.15. Fig. 3.13 presents a single-phase level DAB, the most popular DAB used in power conversion. Fig. 3.14 shows a three-phase DAB converter with a three-phase transformer [48] - [51]. Fig. 3.15 represents a generalized view of a multilevel DAB which can be scaled up, as presented in [52]. Multilevel DAB DC-DC converter topologies are becoming increasingly popular in medium and high voltage applications. Among the existing multilevel topology families, the NPC configurations are the most favorable in terms of efficiency and power density. DAB converters employing three-level NPC legs on one side of the transformer to two-level on the other side of the transformer are presented in [53] and [54]. Three-level to three-level DAB converters are presented in [55] and [56].

3.2.3 Single-Stage Topologies

In addition to the two-stage power conversion methodology, single-stage approaches are also used. They can be configured as two-level or multilevel AC input. Fig. 3.4 shows the generalized idea of a single-stage power conversion with integrated HFT to provide galvanic isolation. This system can also be designed to operate in a bidirectional fashion. The single-stage AC-DC configurations are generally identified by the omission of the inner DC link voltage. As in a two-stage module, the single-stage AC-DC energy conversion must be able to satisfy all the desired functionalities, including power factor correction, galvanic isolation, THD reduction, and output DC voltage control. As a result, this configuration has the potential of providing higher efficiency, lower footprint for higher power density, and increased reliability [57] and [58]. In the literature, various single-stage AC-DC converter structures were presented. In [59], an isolated single-stage AC-DC converter with bidirectional power flow capability was presented. This converter was built using a cycloconverter on the primary side and a full bridge voltage

source converter on the secondary side of the HFT. A three-phase AC-DC DAB converter was introduced in [60] - [62]. This converter configuration contains a cycloconverter on the primary side and full bridge on the secondary DC side, as seen in Fig. 3.16. Another single-stage configuration, which can be seen in Fig. 3.17, was presented in [63] for unidirectional operation and in [64] for bidirectional operation. The configuration consists of a combined three-phase T-type and half-bridge on the primary side and a full bridge converter on the secondary DC side.

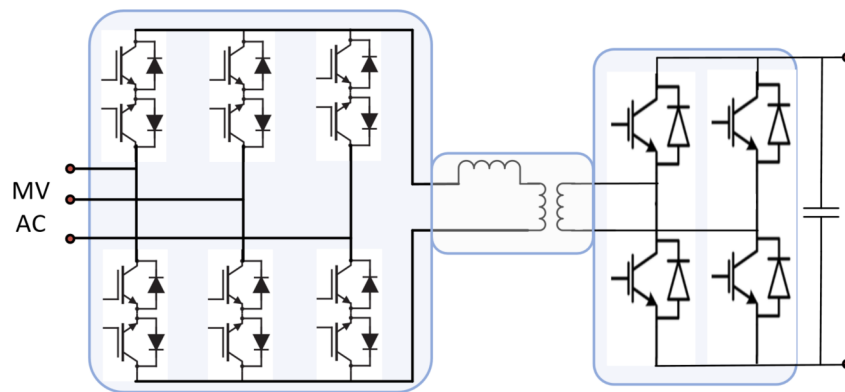


Fig. 3.16 Three-phase AC-DC DAB

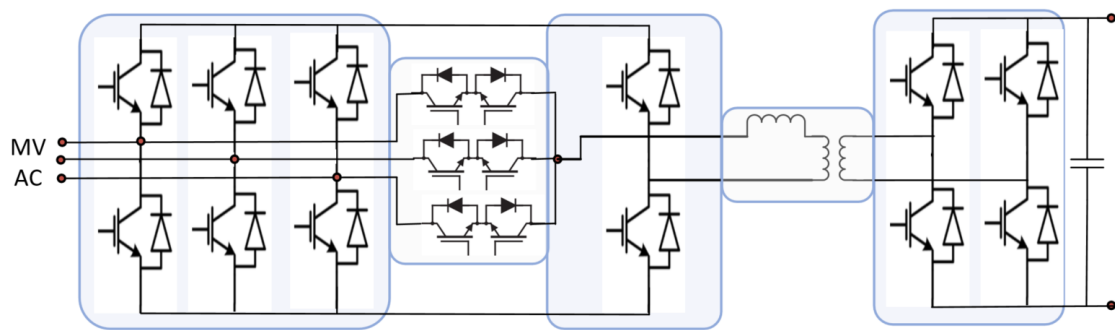


Fig. 3.17 Three-phase boost-type isolated pulse width modulation converter

3.2.4 Modular AC-DC Topologies

One disadvantage of traditional three-phase AC-DC converter configurations is the inability to be configured in series to achieve distribution of the phase voltage between each module. To

solve this issue, phase modular AC-DC converters have been proposed. These structures use multiple converter modules that are series connected and can be scaled based on the desired voltage and power level. Fig. 3.18 shows an example system configuration. As the name implies, the modular AC-DC converter is formed by stacking identical modules as building blocks to achieve the desired voltage and power levels. While many modular AC-DC converters have been implemented and presented in the literature, only the systems that were designed primarily for fast charger technologies are reviewed in this section.

The typical arrangement for interfacing the MV grid is a series input connected for increasing the voltage blocking capability and parallel output connected for providing higher current capability at the desired DC voltage output. Several modular architectures have been presented in prior art for fast charging stations, each with different characteristics in terms of configuration, voltage level, and power capability.

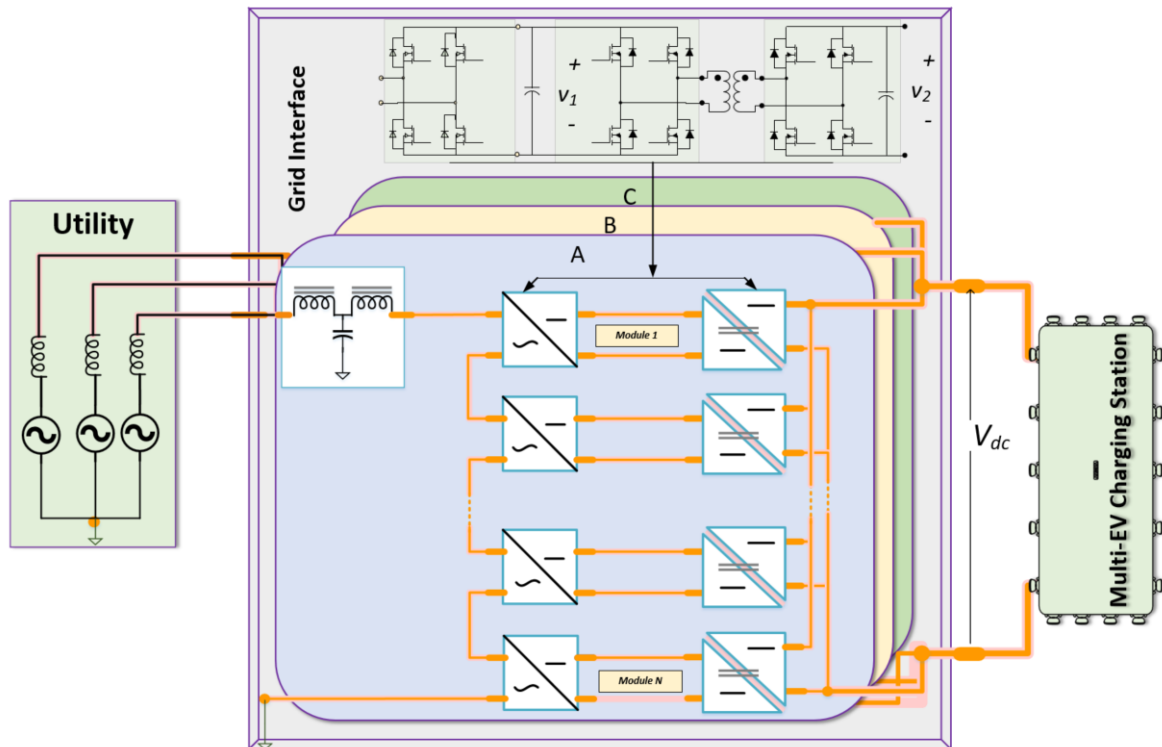


Fig. 3.18 General modular converter configuration

In [65], a three-level boost converter is adopted for DC fast charger technology. This model is based on the MV SST application and utilizes an AC-DC three-level boost configuration and a half-bridge LLC converter for the DC-DC stage. Fig. 3.19 shows the system configuration. In [66], investigators at Delta Electronics proposed a three-phase based SST rated for 400 kW 4.8 kV, or 13.2 kV for fast charger connected applications. The proposed converter is presented in Fig. 3.20. This system is designed to connect to the MV 4.8 kV line-to-neutral system for three series connected modules or 13.2 kV for nine modules. A full bridge three-level NPC type converter is used for the rectification stage in order to reduce stress on the passive resonant components and an isolated LLC resonant DC-DC converter is used for the output stage. This system is also designed for interfacing energy storage or renewable resources through its fixed 1 kV DC output. The reported efficiency for one module is 97.3% at rated condition.

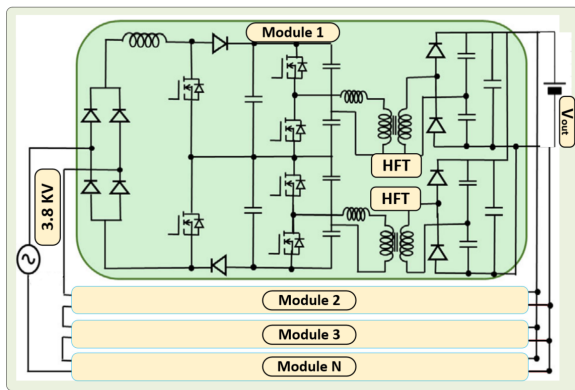


Fig. 3.19 3.8 kV 16 kW EV XFC

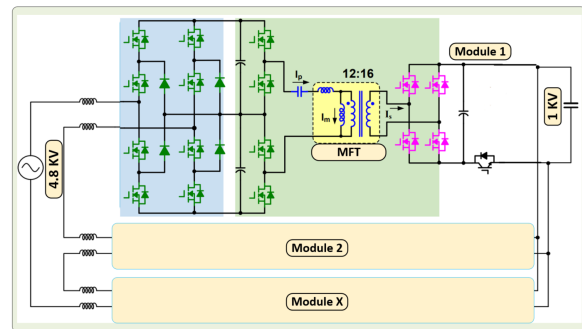


Fig. 3.20 400-kw/1000-v/400-A

A modular multiport system was proposed in [67] with an integrated battery storage unit for fast charger applications. The converter is presented in Fig. 3.21 and contains a full bridge AC-DC rectification stage, an integrated bidirectional buck boost converter for battery storage, and a dual half-bridge DC-DC converter at the output stage. A scaled down version of this system was built to operate at 140 V AC.

A five-level AC-DC configuration was proposed in [68] and [69]. This converter topology is derived from the multilevel NPC structure. The rectifier stage consists of a diode bridge with

the additional three-level boost converter for the AFE stage. The output DC-DC stage is built using one three-level NPC bridge connected to the primary side of the HFT. [68] has reported an efficiency of 98.6% for the maximum power density of $6.6kW/dm^3$. This configuration is shown in Fig. 3.22.

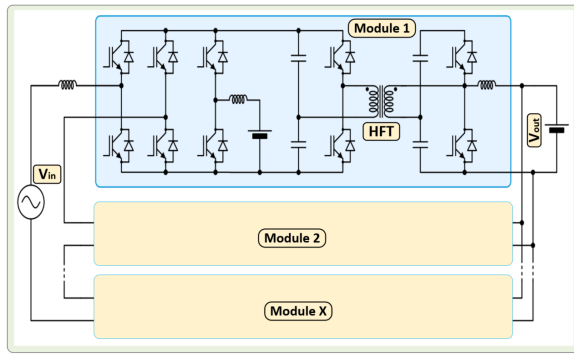


Fig. 3.21 Modular multiport fast charger

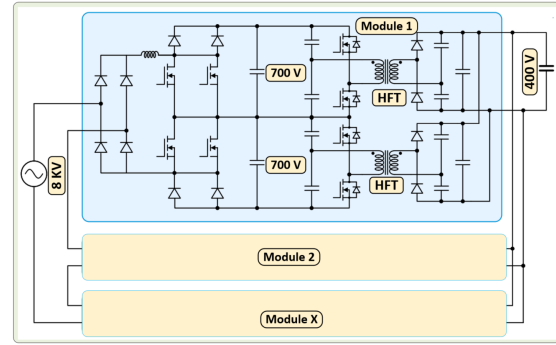


Fig. 3.22 Five-level modular structure for fast charger

[70] proposed a series connected MV converter for fast charging stations. The AC-DC stage consists of three modules connected in series at the 2.4 kV side, while the DC-DC stage is connected in parallel for providing 450 V to the energy storage unit. For achieving rectification, power factor correction, and 1250 V total DC bus, the AC-DC is configured by a unidirectional NPC converter. The DC-DC stage is formed by two ISOP connections of the full bridge converters. For a reported operation of 38 kW, the efficiency of the converter was 96%. Fig. 3.23 shows this converter configuration.

A different fast charger configuration was proposed in [71] for interfacing the MV grid, utilizing three modules connected in series at the 2.4 kV side. This configuration was aimed at minimizing the forward voltage drop on the diodes, maintaining unity input power factor when supplying reactive power, and increasing the overall system efficiency. The DC-DC stage is built using a half-bridge NPC converter for reducing the footprint of the system. Fig. 3.24 shows this converter configuration.

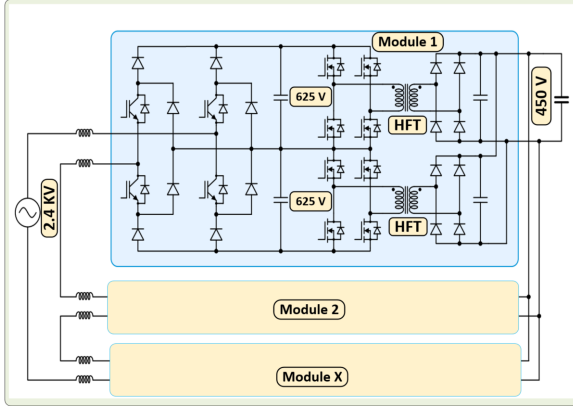


Fig. 3.23 MV fast charger

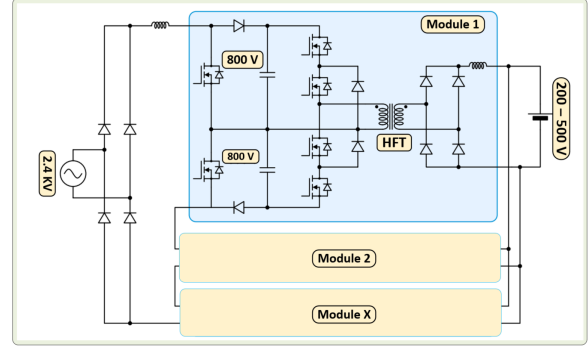


Fig. 3.24 Proposed MV fast charger

The ISOP design of power converters has enabled direct connection to the MV grid using low voltage power devices. This design provides the ability to stack multiple modules for achieving high power technology for EV fast charging stations. By stacking modules together, a multilevel voltage waveform is generated, resulting in decreased THD and a reduction in filter component size. However, the increased number of components and higher control complexity for equal power and voltage sharing among the modules can affect the reliability of the system.

3.3 Topology selection

Based on the different topologies presented in the state-of-the-art for interfacing the MV grid and with the goal of achieving low DC output voltage, a modular system configuration for fleet charging stations was selected and will be described in this section.

The two-stage multilevel ISOP structure was selected for this research project for numerous reasons. It is able to meet the requirements of connecting to MV AC using the currently widely available power MOSFETs and provide galvanic isolation between the load and the input source. Additionally, it can achieve bidirectional power flow and obtain phase modularity and scalability to meet different power and voltage levels. The multilevel topology allows the use of low blocking voltage switching devices with low on-state resistance, which results in de-

creased conduction losses and the ability to operate at a higher switching frequency. Multilevel configuration is useful in decreasing the current and voltage harmonics, which directly result in the use of smaller filter components, thus reducing the system footprint. Modular structure for multilevel systems is obtained by series cascading multiple modules to meet the AC voltage requirements. This is beneficial, as the system can be scaled for different voltage levels and power ratings, and is more manageable in the case of a module failure. Lastly, one of the main requirements for MV AC-DC systems for fleet charging is the integration of galvanic isolation between the AC grid and the DC-side loads, which can be achieved by the ISOP parallel DAB converter.

CHAPTER 4

Cascaded AC-DC AFE Converter and ISOP DAB Converter

AC-DC converters with bidirectional power flow capability have been attractive in both industry and academia. Three-phase voltage source converters and multilevel NPC converters with LCL filter based AFE converter topologies are one of the widely used candidates that can operate with high power factor in a bidirectional power flow manner. The EV charger must isolate the battery and the power grid to prevent any ground fault impact on either side. In order to achieve galvanic isolation between the grid and the EV battery, the system can be configured as the following: a line frequency transformer, an AC-DC rectification stage, and a non-isolated DC-DC converter, which can be a buck converter, a boost converter or an interleaved converter design. Using an HFT embedded into the isolated DC-DC converter stage is another option. Phase shifted full bridge converters and resonant converters are the most common topologies used for unidirectional isolated DC-DC converter stages. For bidirectional isolated DC-DC converter topologies, DAB converters and bidirectional resonant converters are the most commonly used. For higher power applications, DAB and resonant topologies can be connected in series and/or parallel [72].

Fig. 4.1 shows the configuration of the three-phase fast charging system design based on the SST concept. The topology consists of a cascaded multi-level AFE rectifier and a modular ISOP DAB DC–DC converter with HFTs.

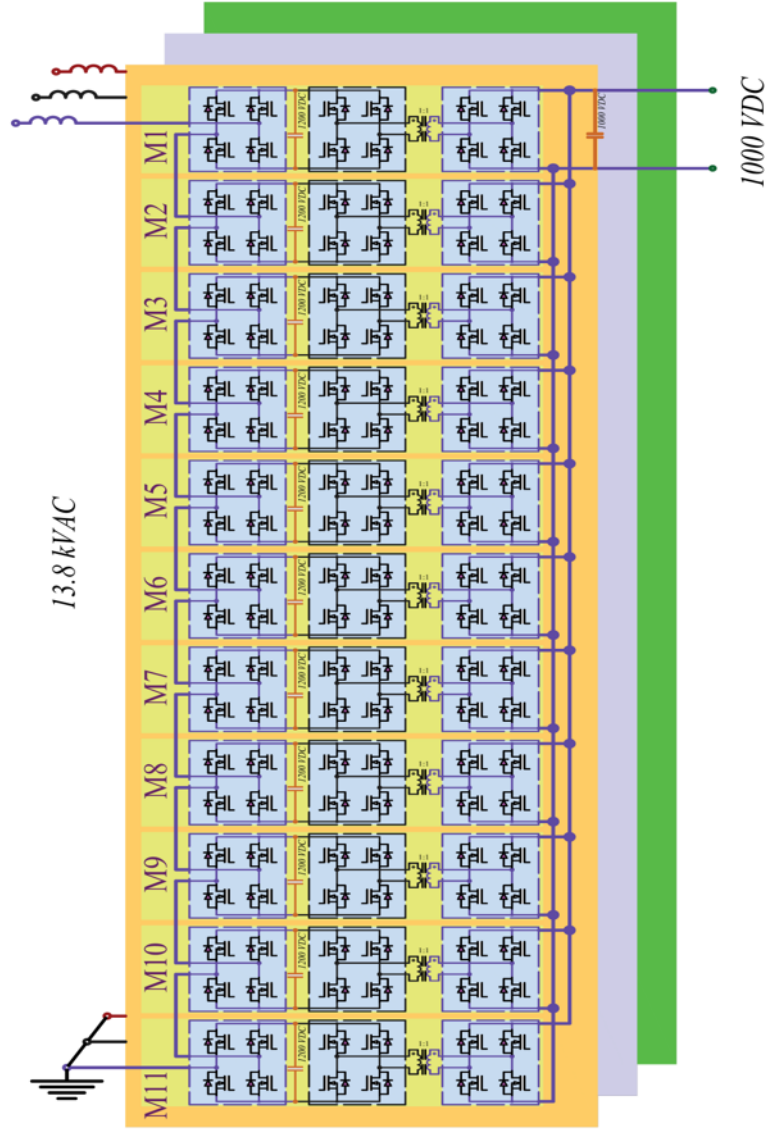


Fig. 4.1 The SST converter architecture

A scaled down version of this system is considered for analysis and verification. The scaled down converter is connected to the utility grid through an LCL filter, which is used to provide filtering and reduce the THD. The AFE establishes the DC link interface for the ISOP DAB converter. The input AC current and DC link voltage controllers are designed to maintain high power quality and low THD performance. The isolated ISOP DAB DC-DC converter establishes the output DC bus for the battery based energy storage unit or EVs and provides compact, integrated, and galvanic isolated connections for the loads. To study the optimum

performance of the system, the governing equations of the scaled down single-phase SST are obtained to implement the control and analyze both the AC and RMS currents of the DAB. These equations are presented in Chapter 5.

4.1 Cascaded H-Bridge AFE

The two main purposes of the AC-DC rectification stage with power factor correction (PFC) are to regulate the DC voltage and provide high power factor. The control scheme includes a voltage outer loop and a current inner loop. A three-phase voltage source control based rectifier is widely used in industry due to its bidirectional power flow, low voltage distortion, near unity power factor, and DC voltage control capabilities [73]. However, this method needs two line-voltage sensors, two phase-current sensors, and a DC-link voltage sensor, resulting in a high total cost.

Sensorless control methods, such as direct power control model predictive control (MPC), have been proposed to decrease the cost and increase the robustness during disturbances [74] – [77]. Although active and passive methods can be used for PFC, the passive methods have a larger size, volume, and weight, and a limited PFC performance. This is especially true for variable load conditions [78]. Conversely, active PFC methods can control DC voltage and offer a high power factor over a wide operating range. For unidirectional power flow, a diode rectifier is connected to a boost, buck, or buck-boost converter. The main disadvantage of these PFCs is high power loss. The bridgeless PFC can address this issue by reducing the number of semiconductor components in the line current path [79]. However, the bridgeless PFC has higher common mode noise.

For a high/medium voltage AC to low voltage DC system, the cascaded multilevel converter is widely used. One of the main challenges in this topology is to balance the floating

capacitor output voltage for stable operation of the whole system. Several methods, including self-balancing control [80], zero/negative sequence voltage injection [81], selective harmonic elimination by pulse width modulation (PWM) [82], selective harmonic elimination by MPC [83], and space voltage vector adjustment [84], have been presented to address this issue. There are advantages and disadvantages to each method and different considerations, such as complexity, dynamic performance, effect on switching frequency, applicability, and computation burden, that must be taken into account when selecting or proposing a new method.

4.1.1 AFE Control

The cascaded H-bridge multi-level (CHBML)-AFE converter controller generally contains an output DC bus voltage control, a grid voltage synchronization entity, and a utility current regulator. Control designs and methods to address output DC bus voltage control and utility current regulation in CHBML-AFEs have been presented in literature.

4.1.1.1 Grid Current Control

Numerous control designs have been introduced to regulate the utility current. The deadbeat current regulator was implemented in [85] to reduce the current error at each consecutive sampling period. Even though this method offers a fast transient response, it is sensitive to variation in system parameters [86] and [87]. A method based finite MPC was presented in [88] to reduce computation complexity and improve the steady-state performance of the current. In order to regulate both the voltage and the current of the system, cascaded proportional integral (PI) controllers were utilized in [89]. Hysteresis current control strategies were proposed and studied in [90] and [91] to reduce the current harmonics of the grid. Although the hysteresis strategies are simple, the main drawbacks are high current total harmonic spectrum and variable switching frequency. The proportional resonant (PR) current regulator was analyzed in [92] for tracking

sinusoidal signal and in [93] for observing the change in photovoltaic (PV) irradiation. The predictive current regulator was implemented in [94] and [95] to decrease switching frequency. A harmonic current rejection PWM regulator method was used in [96] to decrease the harmonics.

The sliding mode control (SMC) method has been successfully employed for regulating power converters due to these benefits: improved performance against parameter variations and external disturbances, rapid dynamic transient response, and simplicity of implementation [97] and [98]. SMC was also used in [99] and [100] to guarantee a constant DC bus voltage and realize unity power factor in boost CHBML-AFE structures. However, SMC presents a couple of drawbacks: problems with variable switching frequency and the occurrence of steady-state errors in the voltage output. A weak dynamic response of the SMC when a load transient occurs is due to the frequent sliding gain in the sliding surface function. This prevents the convergence of the tracking errors to zero in finite time. In order to mitigate the issue of constant sliding, the rotating sliding line was introduced in [101] to provide improvement to the dynamic response. The Lyapunov Function (LF) based control method was successfully applied to regulate DC-DC converters [102], three-phase AC-DC converters [103], single- and three-phase shunt active power filters [104] and [105], and single-phase grid-connected inverters [106]. Outstanding dynamic response and global stability under large signal transients are achieved through the use of the LF technique.

4.1.1.2 Module Voltage Control

Voltage balancing is the one of the main challenges in the implementation of this topology. Voltage balancing control can be carried out either by a cascaded H-bridge (CHB) [107] and [108] or a CHB and a DC-DC converter [109] and [110]. Although the first approach is more flexible, the time response is lower due to the use of a PI controller and the lower switching

4.1.2 LCL Filter Design

In grid-connected inverters and AFE circuits, an effective filter is required in order to decrease the ripple of the output current and current harmonics injected from the grid. To this end, an L-filter, which is a first order filter, was introduced. Disadvantages of this filter include poor harmonic attenuation and dynamic performance, high voltage drops across the inductor, and bulkiness [116]. The higher-order filters, such as LCL, LCL-LC, LLCL, and trap-filter, present excellent performance with compact size. Due to its simplicity and high performance, the LCL filter has attracted high attention in both academia and industry.

The power quality indices dictate the component size of the LCL filter. The inverter and grid side inductors and the capacitor size are determined based on the desired output current ripple, the attenuation capability at high frequencies, and the maximum generated reactive power at fundamental frequency [117]. When designing the LCL filter, resonance poses a challenge, as it can harm the system. Either a control method or passive and active damping methods utilizing resistor/resistors can attenuate this issue and increase system robustness and stability [118]. The design process is iterative and requires consideration of the resonant frequency, voltage drop, maximum output current ripple, minimization of the THD, and damping method [119]- [121]. Among the methods proposed, [120] was chosen for the LCL filter design for this work, as it offers a systematic design methodology that meets industrial requirements and limits THD to a specific value. Performance details of this filter are included in Chapter 5.

4.2 DC-DC DAB Converter

The DAB converter, as seen in Fig. 4.3, incorporates two voltage sourced active bridges linked by an HFT and additional external series inductors on either the primary or secondary side of the transformer. This converter was first presented in [122] for achieving high efficiency, high

power density, and isolated DC–DC conversions while maintaining ultra fast dynamic response and the capability of operating in buck-boost mode. It also provides bidirectional power flow. Due to the capability of the DAB converter to auto-adjust the power flow in both directions, operate under wide voltage gain ratios, and achieve zero voltage switching (ZVS), it has been widely used in many applications, including energy storage systems, micro-grids, SSTs, power electronic traction transformers, and on-board chargers for EVs [122].

The HFT is one of the major components of the DAB converter. It provides the galvanic isolation between the MV grid and the battery or the loads. In the case of a battery acting as a load on the DAB output, the isolated configuration can help avoid the high insulation voltage on the battery side. While DAB is a popular technology, there are many challenges to overcome. The high circulating current, which is analogous to reactive power in power system applications, does not participate in the power transfer of the converter. It is simply a heat source that affects the conduction and copper losses and eventually decreases the efficiency of the converter. Loss of ZVS is another issue that impacts the switching loss of the DAB [123]. Numerous modulation methods have been proposed in order to improve the performance of DAB converters. They can mainly be categorized into three techniques based on the degree of control freedom. The next sections describe each modulation technique and their advantages.

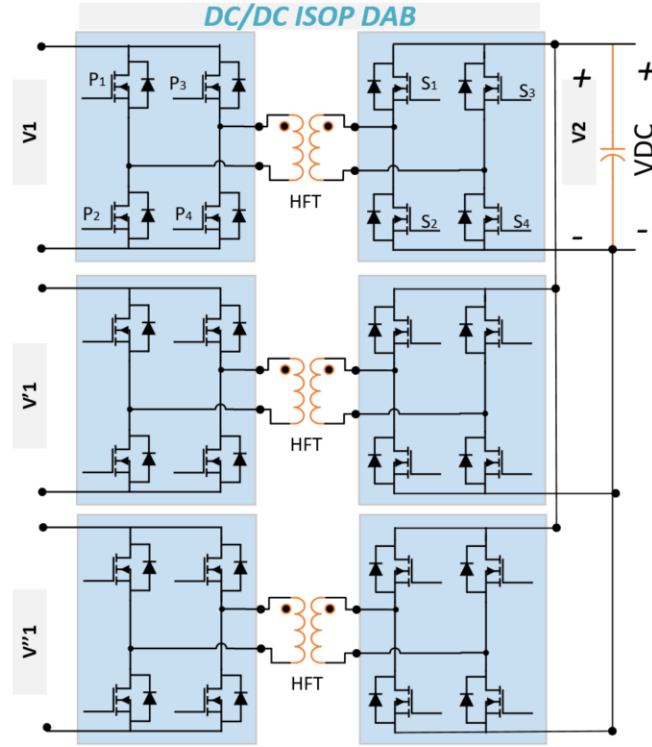


Fig. 4.3 DAB converter configured as ISOP

4.2.1 Single-Phase Shift Modulation

The simplest and most common method of regulating the DAB is single-phase shift (SPS), which uses only one degree of control freedom to regulate the output power flow of the DAB [124]- [129]. In SPS control, the switch pairs in both full bridges are gated to obtain phase shifted square waveformss with a 50% duty cycle ratio. Only the phase shift among the bridges is controlled. Adjusting the phase shift between the primary and the secondary voltage results in the leakage inductor of the transformer changing to enable power flow direction and magnitude [130]. Particularly in the case of a rated power transfer and a square waveform voltage amplitude ratio at unity, this modulation scheme is instrumental in achieving soft-switching. The SPS method utilizes $D_1 = D_2 = 0.5$, thus contains only ϕ as the degree of control freedom. Fig. 4.4 shows the primary and secondary voltages and the leakage inductor of the transformer.

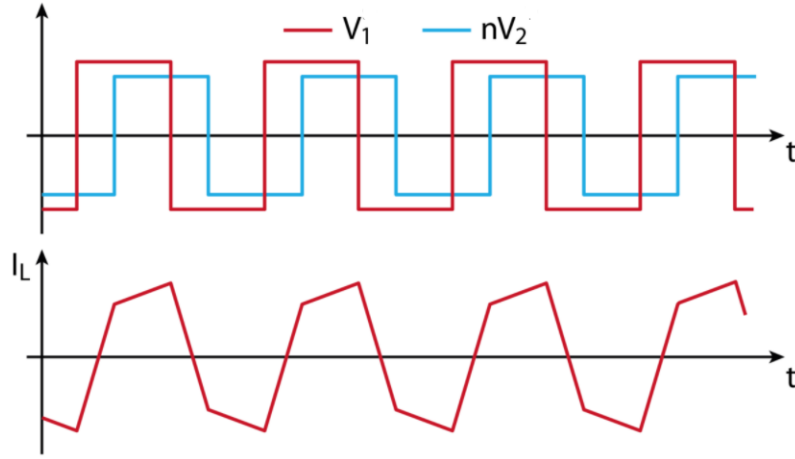


Fig. 4.4 DAB primary and secondary voltages and inductor current waveforms

Using the SPS method, the expression for power transfer between the primary and secondary sides of the transformer can be formulated in (4.1) and has a maximum power transfer when $\phi = 0.25$.

$$P = \frac{2nV_1V_2}{f_s L_{leak}} \phi(1 - 2\phi) \quad (4.1)$$

This method presents the advantage of being simple, as it has only one control variable and can achieve the highest power flow. However, drawbacks of SPS include high RMS current, back flow power, limited operating range, and limited ZVS range for unequal voltage on the primary and secondary sides of the transformer [131] - [138]. Due to the presence of high RMS current, which leads to high conduction and switching losses, phase shift modulation is not applicable for high efficiency applications.

4.2.2 Extended-Phase Shift and Dual-Phase Shift

To increase the control flexibility of the DAB, extended-phase shift (EPS) [132], [136], [137] and [139] and dual-phase shift (DPS) [131] and [140] modulation schemes have been studied. In the EPS method, the switch pairs in one full bridge are switched with an inner phase shift ratio. This enables the AC output voltage of one bridge to be a three-level waveform, while the

other is a two-level 50% square waveform [137]. Both methods contain two control variables. In the EPS method, the duty ratio of one full bridge is considered in addition to the phase shift, while in the DPS method, both full bridges use an inner equal phase shift ratio in addition to the phase shift. Comparatively, while both methods maintain the same operating conditions of the two bridges even while the converter changes power flow direction, the implementation of the DPS is easier than the EPS method. Fig. 4.5 and Fig. 4.6 show the generated primary and secondary voltage and inductor current waveforms of these two methods. Assuming P_1 leads S_1 , the power equation for the EPS method can be formulated, as in (4.2) and (4.3) for the DPS method.

$$P = \frac{NV_1V_2}{4f_sL_{leak}} \left(D_{EP1}(1 - D_{EP1} - 2D_{E2}) + 2D_{E2}(1 - D_{E2}) \right) \quad (4.2)$$

$$P = \frac{NV_1V_2}{2f_sL_{leak}} \begin{cases} \left(\frac{-1}{2}D_{D1}^2 + D_{D2}(1 - D_{D2}) \right), D_{D2} \geq D_{D1} \\ D_{D2}(1 - D_{D1} - \frac{1}{2}D_{D2}), D_{D2} < D_{D1} \end{cases} \quad (4.3)$$

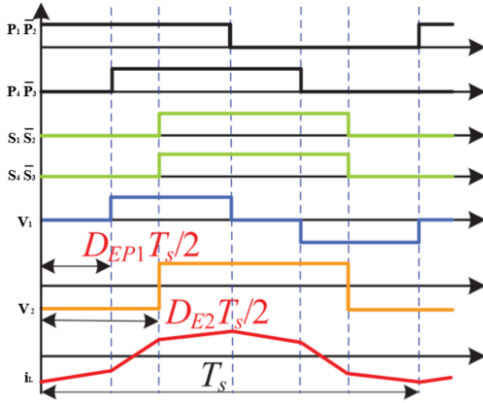


Fig. 4.5 DAB voltage and inductor current waveforms under EPS modulation

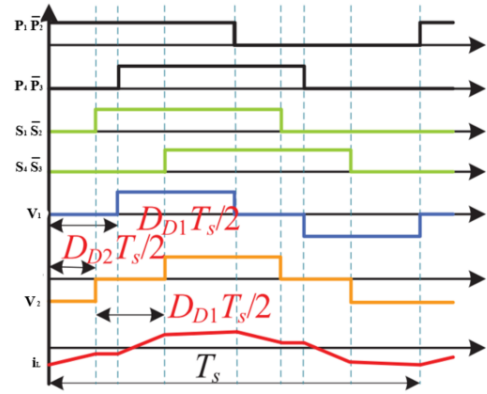


Fig. 4.6 DAB voltage and inductor current waveforms DPS modulation

The EPS method can decrease the conduction losses and circulating energy at medium power transferred. However, for low power transfer, it becomes less effective [132]. Comparison between the SPS and DPS modulation schemes show the DPS can be employed to minimize

the current stress, increase the ZVS operation range, and decrease the nonactive power of the DAB converter [141] - [143]. The EPS method is also able to achieve these benefits [144] - [146].

4.2.3 Triple-Phase Shift: Triangular and Trapezoidal Modulations

Triple-phase shift (TPS) is a unified three degree of freedom control technique which is utilized for optimizing the efficiency of different operating zones and modes of the DAB. Both triangular modulation (TRM) and trapezoidal modulation (TPM) techniques are subcategories of the TPS method. In triangular modulation [147]- [150], both the primary and the secondary converters generate three-level switched voltage waveforms using three degree of freedom control variables. Similarly, the trapezoidal modulation method [151]- [155] regulates the duty ratios of the two full bridges and the phase shift ratio independently to generate the three-level voltage waveforms. The generated voltages and inductor current based on these modulation techniques can be seen in Fig. 4.7 and Fig. 4.8. Although these two methods are similar in terms of control variables used to regulate the power, their generated waveforms are different, as seen in Fig. 4.7 and Fig. 4.8. In TRM, the control is implemented in a way that the voltage turn-ons are aligned and the secondary voltage is turned off when the inductor current equals zero. In this case, the secondary H-bridge always switches under zero current switching (ZCS). To overcome the limited maximum power transferred by the TRM modulation technique, TPM can be used. Using this method can help the primary and secondary H-bridges achieve ZCS two times per period. It can be noticed that the SPS, EPS, DPS, TPM, and TRM controls are all special cases of TPS. The same power flow can be obtained with different phase shift and duty cycle values. In TRM, to achieve ZCS on the secondary voltage, the condition should be $(V_1 - nV_2)D_1 = nV_2(D_2 - D_1) \Rightarrow V_1D_1 = nV - 2D_2$, meaning that power transfer is not

feasible when $V_1 = nV_2$. The max power transfer for TRM can be formulated as (4.4).

$$P_{TRM-max} = \frac{N^2 V_2^2 (V_1 - NV_2)}{4f_s L_{leak} V_1} \quad (4.4)$$

Chapter 5 contains the derivations for formulating the average power transfer and RMS current for different operating points under the TPS method. The power transfer for one region is presented in (4.5).

$$P_{TPS} = \frac{V_1 V_2}{8LF} (-(D_1^2 + D_2^2) - 2 + 2(D_1 + D_2) + \phi(2 - \phi)) \quad (4.5)$$

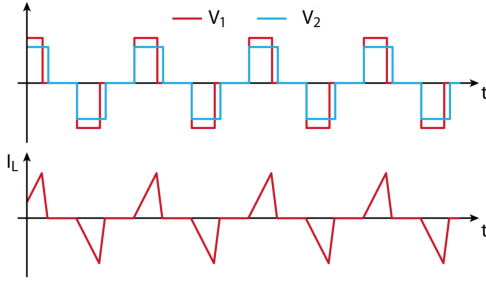


Fig. 4.7 DAB voltage and inductor current waveforms under TRM modulation

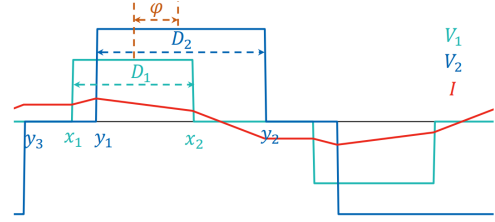


Fig. 4.8 DAB voltage and inductor current waveforms under TPS modulation

4.3 DAB Converter Optimization Methods

Although the DAB converter has many positive characteristics, some limitations exist. Variations in the performance of the DAB converter depend upon the operating range. At low power operation, its performance degenerates significantly. To maximize the performance of the DAB, efficiency optimization has been a focal point of study. Numerous techniques have been presented to achieve the optimum operation and highest efficiency. Generally, there are five techniques used: RMS current minimization, peak current stress reduction, reactive power loss minimization, ZVS range optimization, and total power loss minimization.

DAB converters have gained much interest for their ease of achieving soft-switching, ability to transfer power in both directions, and simple symmetric structure. Nevertheless, a high circulating current issue exists when the voltage amplitude of the DAB is not based on the unity turn ratio of the transformer. Thus, the soft-switching range is affected, especially at light loads [156] - [157]. This section presents control methods and solutions from the literature which are used to optimize the soft-switching range in a DAB.

The ZVS range can be obtained by assuming that the main components of the DAB, such as power MOSFETs and transformers, are ideal devices if the parasitic capacitance and the magnetizing inductance of the transformer are neglected. Based on this stipulation, ZVS can be achieved when the current passes through the anti-parallel diodes during turn on [158]. This is shown in Fig. 4.9, which demonstrates that the converter tends to lose ZVS at lighter loads

$$\phi_b < \phi_a.$$

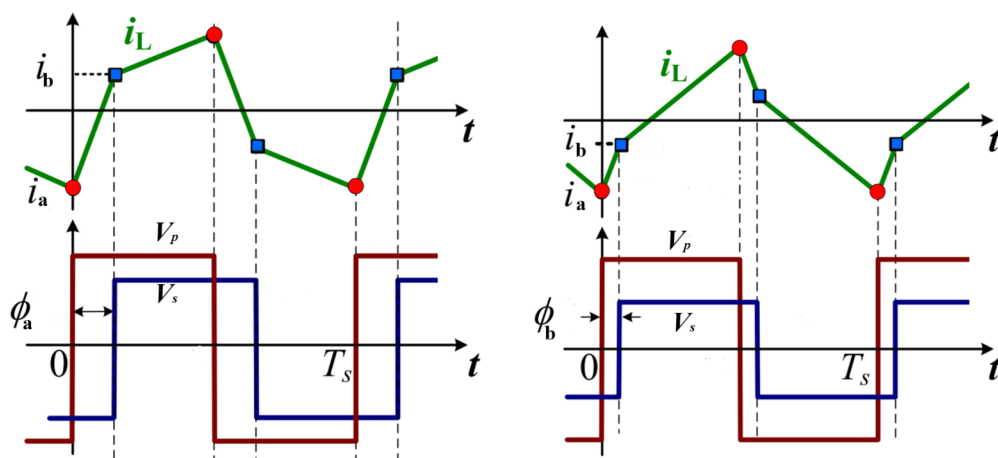


Fig. 4.9 ZVS condition under SPS method

Targeting low load efficiency improvement of high-frequency DAB when operating under SPS [159] presents a method to achieve full load range ZVS. This method utilizes the magnetizing inductance of the transformer to obtain ZVS for all power switches while operating under wide voltage ratio between the primary and secondary sides of the transformer. For this

technique, the turns ratio, magnetizing inductance, and leakage inductance are the considered variables for the optimization process. The overall approach can be seen in Fig. 4.10 [159], where K_l is the leakage and magnetizing ratio and G is the voltage ratio.

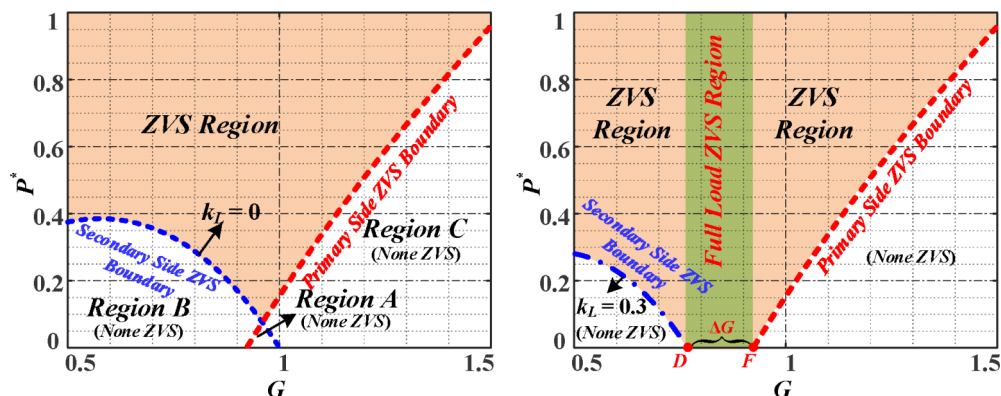


Fig. 4.10 ZVS range improvement under SPS method

In renewable energy application, the DAB converter must be able to operate under wide voltage ratios and wide power ranges due to the intermittent availability of the energy sources and the variable characteristic of the loads or battery charging [160] and [161]. As the DAB is typically regulated using the phase shift control scheme, ZVS can be achieved for a particular voltage and power mode. This increases the likelihood of the converter working under high circulating current at light loads [158]. To mitigate this issue and expand the ZVS range, new converter configurations and more advanced control methods were proposed. The current fed DAB converter, first proposed in [162], has gained much attention for energy storage and PV applications to naturally achieve ZVS condition. To further expand the ZVS range, [163] proposed an extra auxiliary inductor added to the HFT in order to achieve ZVS over the entire operating range. In order to achieve ZVS on all switches, a variable inductor can be used for the HFT, as presented in [164] and [165], a switch controlled inductor can be added in parallel, as in [166] and [167], or an additional control voltage source can be used, as presented in [168] - [171], depending on the power level. Asymmetrical PWM was proposed in [172] to obtain

ZVS and ZCS performance while operating under wide power range.

The increasing demand for high efficiency, especially at light-load conditions, high power capability and high switching frequency, have made DAB the preferred converter configuration. Achieving high efficiency while operating at non-rated conditions or low power level can be cumbersome. Therefore, some trade offs are made when designing the DAB converters. In the literature, the most common strategy is the modification of the control method employed to regulate the converter [173] and [174]. Other researchers have addressed the need for efficiency improvement by reconfiguring the DAB converter. Such techniques include increasing the tap of the transformer, using variable inductors, and adding or rearranging the switches [175] - [177].

In regards to control modifications, many optimized phase shift methods were proposed. However, deriving the governing equations for an analytical approach of the efficiency can be challenging. [178] used the traditional phase shift method for two DABs connecting as input and output parallel to increase the efficiency during certain operation regions of the converter. This was achieved by dictating which converter should be operational. It is well documented that the traditional phase shift method is optimal at unity voltage ratio and rated power. However, when operating away from the unity voltage ratio and rated power, the SPS method is no longer the modulation of choice. [179] proposed a hybrid EPS modulation plus direct power control to improve the efficiency and dynamic performance of the DAB converter, while [180] proposed a linearized modulation technique based on the EPS method to minimize the conduction loss of the DAB. In [181], a broader optimization approach based on both EPS and DPS was proposed to improve the performance and efficiency of DAB converters.

Multiple modulation techniques have been presented to improve upon the shortcomings of SPS. In [136] and [137], a PWM method is introduced to generate three-level PWM voltage in

order to drive each H-bridge to improve the RMS and peak currents and total efficiency. The EPS control technique was studied in [137] to enable the DAB converters to operate under soft-switching, and in [182] to minimize the reactive power loss and naturally obtain ZVS. The DPS method was proposed in [183] to improve the efficiency of the DAB converter and in [184] to obtain the minimum RMS current. While the EPS and DPS methods can significantly improve the DAB performance, it is worth noting that they do not provide a global optimization solution to efficiency improvement.

The TPS control technique has been widely used to obtain a more general solution for improving the efficiency the DAB converter at different power ratings. The TPS method is the unified form of the EPS, DPS, SPS, TRM, and TPM modulation schemes. In [185]- [191], TPS was used to achieve minimum current stress, in [192] to obtain the minimum reactive power flow in the DAB converter, and in [193] - [195] for minimizing the RMS current of the inductor.

Other researchers have studied more advanced TPS based modulation techniques. [196] proposed a TPS based nondominated sorting genetic algorithm 2 for an AC-DC and DAB converter in order to minimize the conduction, dead band, and switching losses of the DAB. With a goal of reducing conduction and switching losses, [197] proposed a TPS based piece wise analytical approach to derive the final hybrid closed-loop control. [198] presented a multiobjective efficiency optimization approach to extend the power range of the DAB converter using a TPS based genetic algorithm to obtain closed-form expressions for the control variables. Taking into consideration only the input and output voltages, the transformer turn ratio, and the leakage inductance, [199] proposed a TPS based perturb-and-observe tracking method to improve light loads efficiency. A numerical approach based on the conduction and switching losses of the power devices, the copper and core losses of the inductor and transformer, and the gate driver loss of the DAB converter, was presented and analyzed in [200]. Although this method

addresses the major losses in the DAB, the reported optimized efficiency was only 93.5%.

Owing to the supplementary control degree of freedom of the TPS control, formulation of the analytical expression for the optimal modulation variable is cumbersome. To formulate a closed-form expression, the Lagrange Multiplier (LM) method was used in [134] to calculate the optimal control variables for minimum peak current stress. [201] used the Karush-Kuhn-Tucker algorithm to formulate the closed-form solutions for the global optimal control variables. The global optimal condition was presented in [194] to obtain the global solution for the minimum RMS current. A randomized optimization algorithm was introduced in [202] for obtaining the minimum current stress.

Artificial intelligence has also been applied to obtain the optimal TPS control variables. Reinforcement learning was introduced in [203] and deep deterministic policy gradient in [204] for formulating the efficiency optimization and minimum reactive power, respectively. Particle swarm optimization (PSO) is another method which has been widely used for numerical analysis. In this work, it is used, along with the LM method, to obtain numerical values for the TPS method.

CHAPTER 5

Control Derivation and Analysis of the System

5.1 AFE Control Derivation

The CHBML-AFE converter controller generally contains an output DC bus voltage control, a grid voltage synchronization entity, and a utility current regulator. Control designs and methods to address output DC bus voltage control and utility current regulation in CHBML-AFEs have been presented in literature. Based on the excellent features of the LF based regulator method discussed in Chapter 4, this work presents an LF based current control method for the CHBML-AFE. The standard LF strategy is modified with an added capacitor voltage feedback loop, leading to inhibition of the LCL filter resonance. Additionally, the PR control strategy generates the inverter side current reference, resulting in the suppression of the filter component value dependency and the steady-state error. Global asymptotic stability can be ensured through calculation of the appropriate gain values. In addition, the transient performance of the system is improved as a direct result of the capacitor voltage feedback. The proposed control scheme utilizes a PI regulator for the DC voltage control. The use of an additional DC voltage balancing controller, which was introduced in [205], helps to prevent unbalanced DC voltage conditions.

A single-phase CHBML-AFE is presented in Fig. 5.1 Three identical cascaded single-phase H-bridge cells form the converter structure. Three separate DC bus voltages, V_{o1} , V_{o2} and V_{o3} , are obtained. The H-bridge input terminals are connected in parallel to the utility grid,

denoted as V_g , via the LCL filter. The LCL filter is comprised of the filter capacitor, C_f , and the impedances, Z_2 and Z_1 , where L_2 and r_2 are the series combination of Z_2 , and L_1 and r_1 are the series combination of Z_1 . The equations describing the CHBML-AFE can be written as (5.1) – (5.6). Equation (5.7) represents the switching function, in which U_o and Δu are defined as the steady-state and unsettled values of u , respectively.

$$\frac{L_2 di_2}{dt} + r_2 i_2 = v_g - v_{cf} \quad (5.1)$$

$$\frac{L_1 di_1}{dt} + r_1 i_1 = v_{cf} - (V_{H1} + V_{H2} + V_{H3}) \quad (5.2)$$

$$\frac{C_f dv_{cf}}{dt} = i_c = i_2 - i_1 \quad (5.3)$$

$$V_{H1} = uV_{01}$$

$$V_{H2} = uV_{02} \quad (5.4)$$

$$V_{H3} = uV_{03}$$

$$V_{01} = V_{02} = V_{03} = V_d \quad (5.5)$$

$$v_g = V_g \sin(\omega t) \quad (5.6)$$

$$u = U_o + \Delta u \quad (5.7)$$

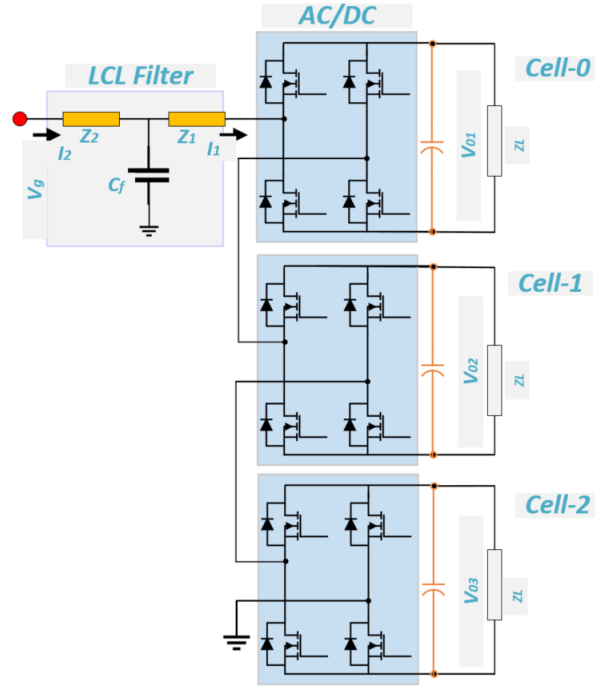


Fig. 5.1 The cascaded H-bridge active rectifier

5.1.1 LF Based Current Control Scheme

To study the stability of the CHBML-AFE converter around its equilibrium point of operation, the LF based controller has been utilized. The direct formulation of LF states that the state variables are at the stability point when the supplied energy from the power source equals the total energy consumed by the load and AFE components. The state variables can be formulated, as in (5.8) - (5.10), where i_1^* , i_2^* and V_{cf}^* are the references for i_1 , i_2 and V_{cf} .

$$x_1 = i_1 - i_1^* \quad (5.8)$$

$$x_2 = i_2 - i_2^* \quad (5.9)$$

$$x_3 = V_{cf} - V_{cf}^* \quad (5.10)$$

From this stipulation, an energy based function can be developed to evaluate the stability of

the system [206], [207] and [208]. As formulated in Lyapunov's direct method, the equilibrium point is universally asymptotically stable if $V(x)$ meets the following criterion for all $x \neq 0$:

$$\begin{aligned} V(0) &= 0 \\ V(x) &> 0 \\ V(x) &\rightarrow \infty \\ \frac{dV}{dt} &> 0 \end{aligned} \tag{5.11}$$

The subsequent LF can be obtained from the stored energy in the inductors and capacitor:

$$V(x) = \Delta E_{L1} + \Delta E_{L2} + \Delta E_c = \frac{1}{2}L_1x_1^2 + \frac{1}{2}L_2x_2^2 + \frac{1}{2}Cx_3^2 \tag{5.12}$$

From (5.12) it can be concluded that $V(0) = 0$ and $V(x) > 0$ for all $x \neq 0$, and $V(x) \rightarrow \infty$ as $\|x\| \rightarrow \infty$. The time derivative of (5.12) is formulated to test the former statement and the universal stability of the CHBML-AFE at its stable point. The time derivative of the LF is formulated in (5.13):

$$\frac{dV(x)}{dt} = x_1L_1\frac{dx_1}{dt} + x_2L_2\frac{dx_2}{dt} + x_3C_f\frac{dx_3}{dt} \tag{5.13}$$

By substituting equations (5.8) – (5.10) into (5.13), this equation can be rearranged, as below:

$$\frac{dV(x)}{dt} = -3V_dx_1\Delta U - r_1x_1^2 - r_2x_2^2 \tag{5.14}$$

Here, $\frac{dV(x)}{dt} < 0$ if the disturbed input regulator is chosen as:

$$\Delta U = K_\alpha V_dx_1 \tag{5.15}$$

where $K_\alpha > 0$ and is a real constant. The ultimate formulation of the control input is presented in the following equation:

$$u = U_0 + \Delta U = \frac{1}{3V_d} \left(L'_1 \frac{di_1^*}{dt} + r'_1 i_1^* + V_{cf}^* \right) + K_\alpha V_d x_1 \quad (5.16)$$

where L'_1, L'_2, r'_1, r'_2 and C'_f represents the estimated values of filter components L_1, L_2, r_1, r_2 and C_f , respectively. Multiplying the voltage regulator output and the unit sine wave, generated by the phase loop lock (PLL) to be synchronized to the grid voltage, produces the $i_2^*(t)$ function in (5.13) and (5.14). Once the $i_2^*(t)$ is generated, $v_{cf}^*(t)$ and $i_1^*(t)$ are obtained, as in (5.17) and (5.18), respectively.

$$v_{cf}^* = V_g - L'_2 \frac{di_2^*}{dt} - r'_2 i_2^* \quad (5.17)$$

$$i_1^* = i_2^* - i_c^* = i_2^* - C'_f \frac{dV_g}{dt} + L'_1 C'_f \frac{d^2 i_2^*}{dt^2} + r'_2 C'_f \frac{di_2^*}{dt} \quad (5.18)$$

The control law in (5.16) yields a globally asymptotically stable operation. Yet, the damping produced is not effective in decreasing the oscillations which result from the complex conjugate poles of the LCL filter. In order to overcome this problem, the traditional LF based control law is adjusted with a capacitor voltage error x_3 feedback loop. This modification is presented in (5.19):

$$\Delta U = K_\alpha V_d x_1 - K_\beta x_3 \quad (5.19)$$

Substituting (5.19) into (5.14) gives:

$$\frac{dV(x)}{dt} = -3K_\alpha x_1^2 V_d^2 - r_1 x_1^2 - r_2 x_2^2 + 3K_\beta V_d x_1 x_3 \quad (5.20)$$

By considering the perfect match between the real and estimated values of the LCL filter com-

ponents, the negative definiteness of $\frac{dV(x)}{dt}$ is ensured if the following inequality is met:

$$K_\beta < \left(K_\alpha V_d - \frac{r_1}{3V_d} - \frac{r_2 x_2^2}{3V_d x_1^2} \right) \frac{x_1}{x_3} \quad (5.21)$$

Both the inverter current and capacitor voltage feedback are included in the ultimate control law, as demonstrated below:

$$u = \frac{1}{3V_d} \left(L_1' \frac{di_1^*}{dt} + r_1' i_1^* + V_{cf}^* \right) + K_\alpha V_d x_1 - K_\beta x_3 \quad (5.22)$$

5.1.2 Reference Inverter Current Generation Using PR Controller

Under disturbances away from the operating point, the closed-loop control is global asymptotically stable using the formulation obtained in (5.22). However, obtaining i_1^* and v_{cf}^* signals is crucial for the proposed control. Even though these signals can be obtained by using (5.17) and (5.18), generating i_1^* can be cumbersome and requires second order differentiation. Therefore, in this study, the PR control technique is used to generate the inverter reference current i_1^* . The dependency on the LCL filter parameters and the requirement for second order differentiation can be mitigated through the use of a PR regulator. It is well established that the PR regulator provides excellent tracking for AC signals along with an infinite gain at ω in order that the utility current will follow its reference without any error in steady-state operation. Although this idea is sound in theory, infinite gain is impossible in a practical system. Thus, in real world applications, the succeeding non-ideal transfer function equation, given in (5.24), is utilized [209]. Equations (5.23) and (5.24) are the responses of the ideal and the non-ideal PR controller, respectively.

$$G(s) = \frac{Y(s)}{E(s)} = K_p + \frac{2K_r s}{s^2 + 2\omega_c s + \omega^2} \quad (5.23)$$

$$G_{pr}(s) = \frac{Y(s)}{E(s)} = K_p + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega^2} \quad (5.24)$$

In (5.23) and (5.24), K_p is the proportional gain while K_r is the resonant gain. ω is the resonant frequency and ω_c is the cutoff frequency. The PR regulator output represents the inverter current reference and can be formulated using the Laplace Domain, as in (5.25).

$$I_1^*(s) = [I_2^*(s) - I_2(s)]G_{pr}(s) \quad (5.25)$$

The magnitude and phase plots of the ideal versus the non-ideal PR regulators, when $K_p = 10.83$, $K_r = 1080.33$, $\omega = 100\pi \frac{rad}{s}$, and $\omega_c = 1 \frac{rad}{s}$, are shown in Fig. 5.2. It can be noted that the gain of the magnitude response of the non-ideal PR is significantly decreased, thus providing better performance.

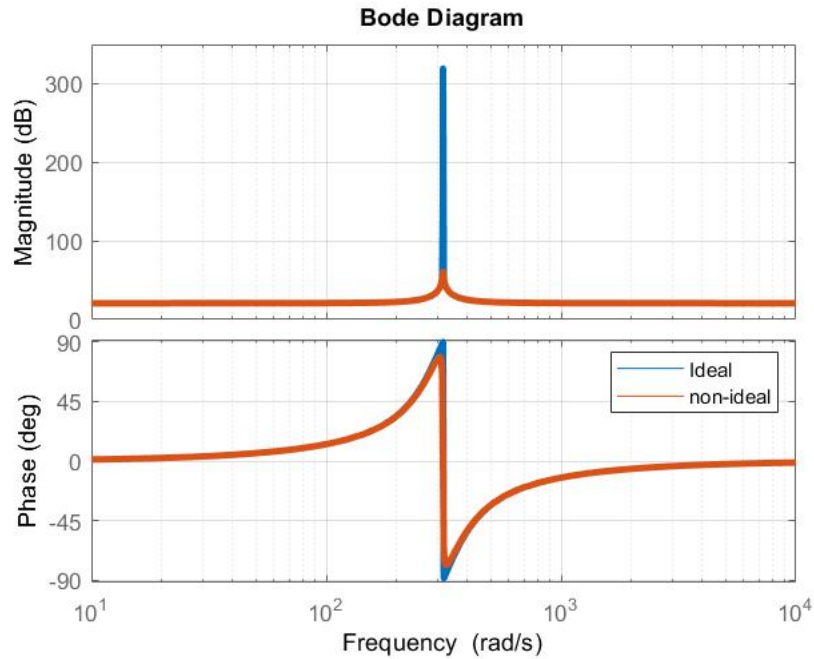


Fig. 5.2 The Bode diagram of the ideal and non-ideal PR

5.2 AFE Control Analysis

5.2.1 Analysis of the Grid Current Transfer Function

A closed-loop transfer function that links the reference to the measured grid utility is formulated in the frequency domain, as in (5.26), in order to predict the behavior of this system. To minimize the number of parameters and simplify the obtained transfer function, the filter inductor resistances r_1 and r_2 are omitted. Substituting the final switching control obtained in (5.22) into (5.2) gives rise to the following expression, as formulated in (5.26). It is seen from (5.26) that the presented control scheme is unaffected by changes in C_f .

$$TF(s) = \frac{I_1(s)}{I_1^*(s)} = \frac{bs^3 + es^2 + gs + d\omega^2}{Ds^5 + Fs^4 + Gs^3 + Hs^2 + Ls + M} \quad (5.26)$$

where

$$\begin{aligned} A &= L_1 + L_2(1 + 3K_\beta V_o) & a &= L_2'(1 + 3K_\beta V_0) \\ B &= 2\omega_c L_1'(K_p + K_r) & b &= a + L_1'K_p \\ D &= C_f L_1 L_2 & d &= 3K_p K_\alpha V_o^2 \\ E &= 3K_\alpha v_o^2 C_f L_2 & e &= d + 2\omega_c(b + L_1'K_r) \\ F &= E + 2D\omega_c & f &= 3K_r K_\alpha V_o^2 \\ G &= 2E\omega_c + A + D\omega^2 + L_1'K_p & g &= b\omega^2 + 2\omega_c(d + f) \\ H &= 3K_\alpha V_o^2 + \omega^2 E + 2A\omega_c + B & I &= 6K_\alpha V_o^2 \omega_c + (A + L_1'K_p)\omega^2 \\ J &= 3K_\alpha V_o^2 \omega^2 L = I + d + f & M &= J + d\omega^2 \end{aligned}$$

The characteristic equation can be used to analyze the stability of the closed system. Since

$K_\alpha > 0, K_\beta > 0, K_p > 0$, and $K_r > 0$, it is inferred that the characteristic equation contains only positive constant coefficients. Application of the Routh–Hurwitz stability criterion leads to the following formulations (5.27) - (5.31):

$$FG - DH > 0 \quad (5.27)$$

$$FL - DM > 0 \quad (5.28)$$

$$LF^2 - GFH - DMF + DH^2 > 0 \quad (5.29)$$

$$M > 0 \quad (5.30)$$

$$D^2M^2 - 2DFLM - DGHM + DH^2L + F^2L^2 + FG^2M - FG > 0 \quad (5.31)$$

The closed-loop system is stable when the above conditions (5.27) - (5.31) are satisfied. However, these conditions are not sufficient to determine the desired values of the controller. Determination of the control parameters will be explained in the next section.

5.2.2 Determination of Control Parameters

It can be seen from (5.26) that the transfer function and the characteristic equation are fifth order. Thus, achievement of the optimum values of the controller gains analytically is cumbersome. Before focusing on the optimum parameter determination, effectiveness of the proposed voltage feedback loop was investigated. Fig. 5.3 and Fig. 5.4 show the frequency response of the proposed controller when there is a 10 percent deviation in all three component values of the LCL parameters with and without the capacitor voltage feedback loop, respectively, at the same time. The gains of the PR controller are set to $K_p = 10.833$, $K_r = 1080.33$, $\omega = 100\pi \frac{rad}{s}$, and $\omega_c = 1rad/s$. It can be observed in Fig. 5.3 that although different K_α were used in the

control scheme, which does not contain the added capacitor voltage feedback loop ($K_\beta = 0$), the resonance cannot be damped. However, the desired resonance damping can be obtained when the added capacitor voltage loop is enabled, as depicted in Fig. 5.4. The level of damping is related to the value of K_β . Additionally, when both control methods are used, it can be noted that there is no steady-state error (0 dB magnitude at 60 Hz) or phase shift (0° phase at 60 Hz) in the utility current. This provides evidence of the effectiveness of the PR regulator.

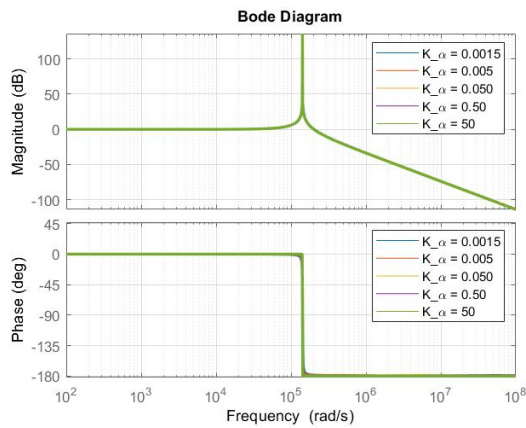


Fig. 5.3 The magnitude and phase responses without the capacitor voltage feedback loop ($K_\beta = 0$)

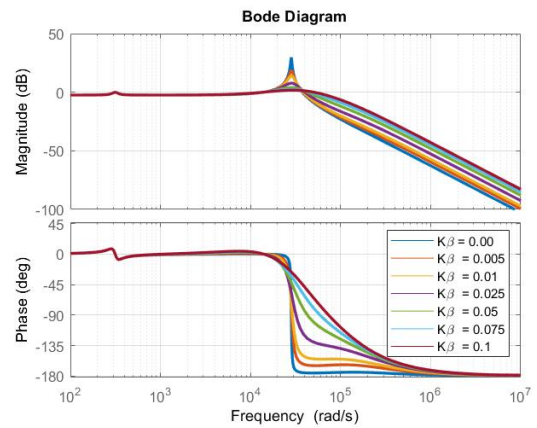


Fig. 5.4 The magnitude and phase responses with the capacitor voltage feedback loop ($K_\alpha = 0.05$ and $K_\beta \neq 0$)

As mentioned above, the PR controller is used to obtain i_1^* from the utility current error ($i_2^* - i_2$). It is worth noting that K_p influences the dynamics of the system, and K_r has an important role in decreasing steady-state error and dictating the bandwidth around the fundamental frequency [209] and [210]. To determine the PR controller gains, K_α and K_β are fixed at $K_\alpha = 0.05$ and $K_\beta = 0.025$. The magnitude and phase responses of the PR controller for different K_p and K_r values are given in Fig. 5.5 and Fig. 5.6. When K_r is increased, there is no change in the magnitude of the resonant peak. However, the bandwidth increases at 60 Hz. Since the gains of a PR regulator can be adjusted in the same manner as a PI regulator, the

technical optimum criterion [210] and [211] can be used to obtain K_p and K_r :

$$K_p = \frac{f_{sw}(L_1 + L_2)}{3} \quad (5.32)$$

$$K_r = \frac{K_p(r_1 + r_2)}{L_1 + L_2} \quad (5.33)$$

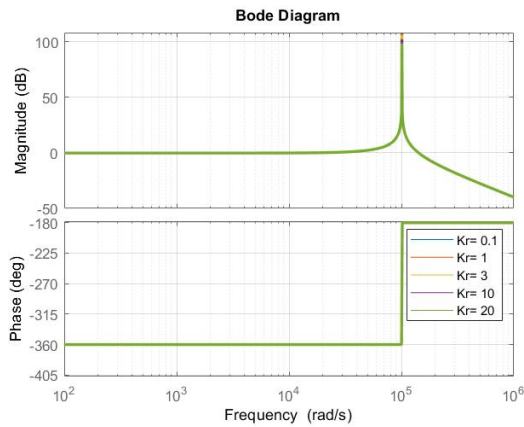


Fig. 5.5 The magnitude and phase responses for $K_r = 10$

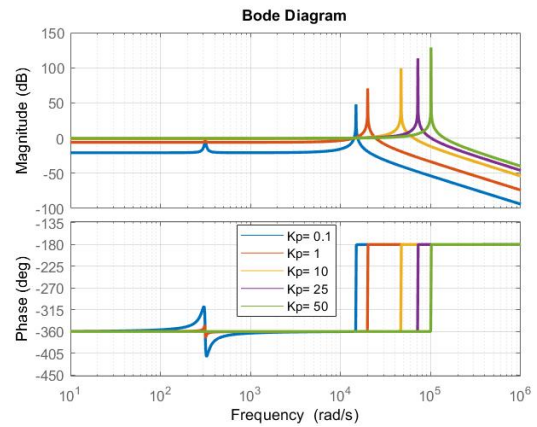


Fig. 5.6 The magnitude and phase responses for $K_p = 1200$

The root locus graphs of the system for different K_α and K_β gains with constant K_p and K_r were obtained to observe the movement of the roots, and are given in Fig. 5.7 and Fig. 5.8, respectively. As previously mentioned, the system is fifth order. However, the LF based controller mainly affects only three of the five poles (a complex conjugate poles pair and one real pole). The dynamic response of the system maintains the global stability. The other complex conjugate poles pair is located near the imaginary axis in the s-plane and is only influenced by the gains of the PR regulator for the purpose of achieving a zero steady-state error in i_2 .

Initially, K_β , K_p and K_r gains are kept constant. Fig. 5.7 represents the movement of the system poles when K_α is varying. The movement of the real pole is not shown in Fig. 5.7, as it is much larger than the real part of the complex conjugate poles. It is seen that the complex conjugate poles move away from the imaginary axis while the real pole (which is

not seen in the figure) moves toward the imaginary axis. Additionally, K_α gains significantly affect the real part of the conjugate poles, but have comparatively less effect on the imaginary parts. Therefore, K_α improves the system dynamics but can provide limited resonance damping effect to suppress the oscillations introduced by the complex conjugate poles of the LCL filter. When K_β is increased from 0 to 0.1, as in Fig. 5.8, the complex conjugate poles move away from the imaginary axis. The damping ratio increases, while the real pole moves toward the imaginary axis. However, the damping ratio is decreased with larger K_β values, as the real pole moves toward zero. This leads to deterioration in the dynamic response and may risk the stability of the system. Therefore, optimum determination of the controller gains greatly affects the performance of the controller. Since the closed-loop transfer function is extremely complex, simulation studies are used to determine the K_α and K_β in order to obtain a fast dynamic response and globally stable system. In this study, controller gains are determined as $K_\alpha = 0.005$ and $K_\beta = 0.025$.

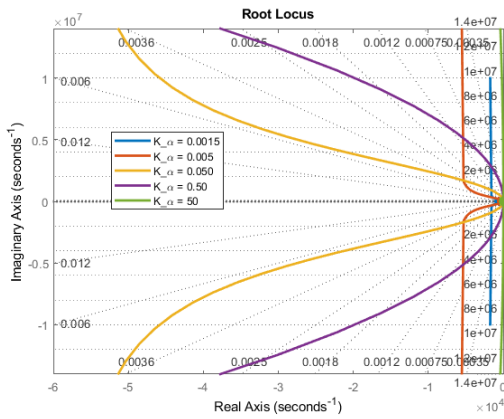


Fig. 5.7 Root locust of the transfer function for different K_α values

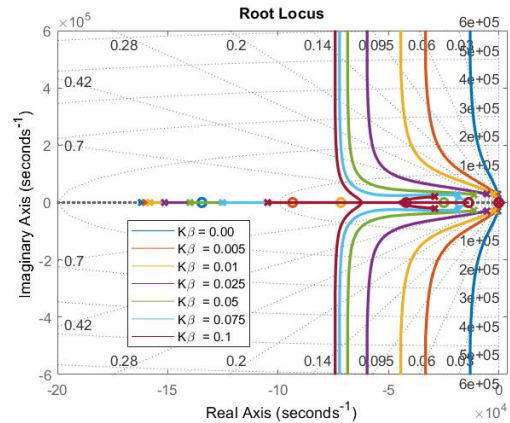


Fig. 5.8 Root locust of the transfer function for different K_β values

5.2.3 Controller Structure

The proposed control scheme is given in Fig. 5.9, which shows the overall controller structure.

Fig. 5.10 demonstrates the detailed diagram of the controller.

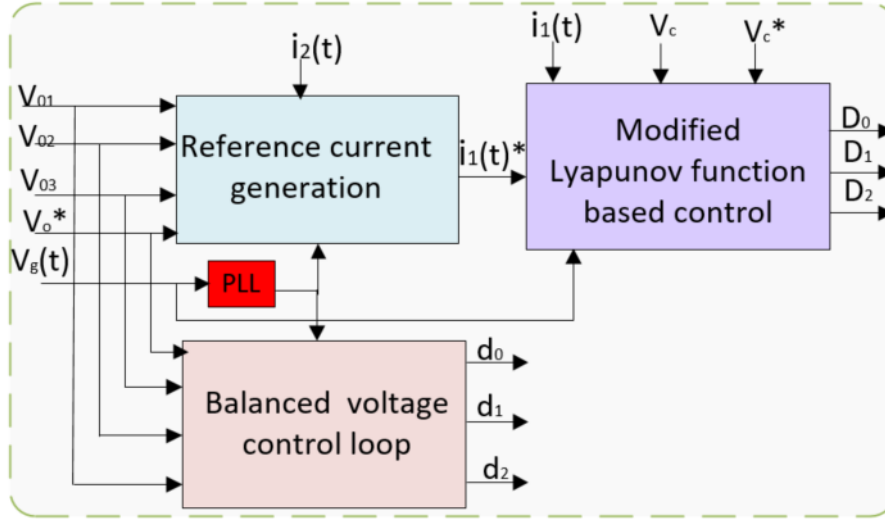


Fig. 5.9 Overall controller block diagram of the proposed controller with capacitor feedback voltage loop and DC bus balancing

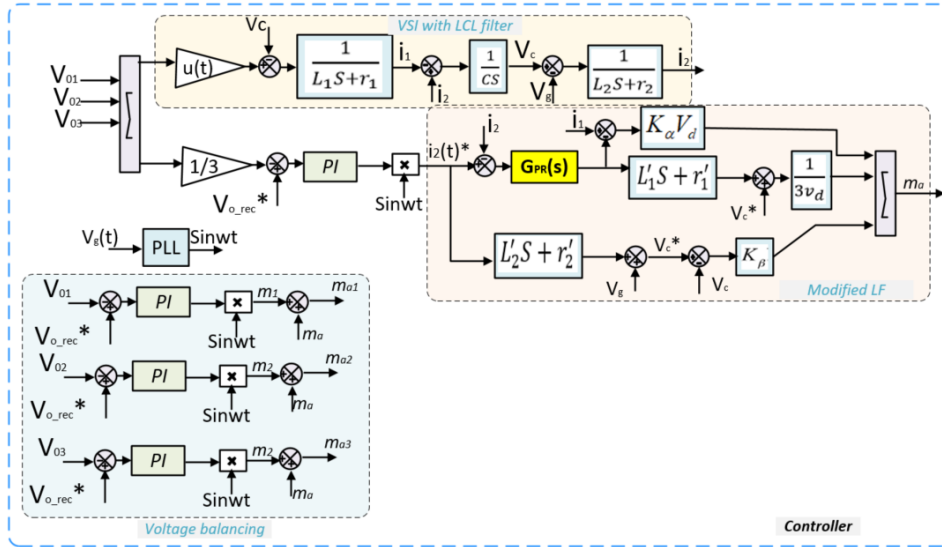


Fig. 5.10 Detailed controller block diagram of the proposed controller with capacitor feedback voltage loop and DC bus balancing

The overall control method contains three main parts: the generation of the grid current reference, the modified LF based method, and the output bus voltage balancing control. The grid reference current is obtained by summing the output voltages and dividing that result by the number of DC buses present in the CHBML-AFE to obtain the average DC voltage value. This average voltage is taken as the reference value and is regulated by the PI controller. By multiplying the output of the PI controller and the unit sine wave, which is synchronized with

the grid voltage and frequency and generated by the PLL unit, the reference signal for the grid current is generated. This reference current is then fed to the PR controller block to produce the final reference for the modified LF. In addition to the LF based control with additional capacitor voltage loop and PR controller, a voltage balance controller is also applied to balance the cell voltages of the CHBML-AFE. The goal of this voltage balance controller is to remove possible unbalanced voltage conditions for situations where mismatched parameters occur or different loads are applied to the cells of CHBML-AFE. The output DC voltage of each cell is controlled by a PI controller. The output of the PI is then multiplied by the reference sine wave (the output of the PLL) to generate the perturbed duty cycles. These are added to the switching control, which is generated by the modified LF block. The relationship between each block is seen in detail in Fig. 5.10.

5.3 AFE Converter Loss Analysis

The CHBML-AFE power losses are formulated based on the conduction and switching losses. Conduction losses in power MOSFETs can be formulated using the MOSFET-approximated drain-source on-state resistance. The conduction loss of the anti-parallel diode is also formulated to obtain the total conduction losses. R_{DS} is the on-state resistance and V_{do} is the diode voltage drop. Taking into consideration the inverter side inductance current oscillation and the switching operation mode, the conduction and switching power losses are obtained, as in (5.34) and (5.35) [212] and [213].

$$P_{con-AFE} = 2N_{cell}(R_{DS}I_{rms}^2 + V_{do}i_{ave}) \quad (5.34)$$

$$P_{sw-AFE} = 2N_{cell}f_s \left(E_{ON}(|i_{ave} - \frac{\Delta i_b}{2}|, V_d) + E_{OFF}(|i_{ave} + \frac{\Delta i_b}{2}|, V_d) + Q_{rr}(|i_{ave} - \frac{\Delta i_b}{2}|, V_d) \cdot V_d \cdot f_{sw} \right) \quad (5.35)$$

E_{on} , E_{OFF} , Q_{rr} , V_d , f_{sw} , and N_{cell} are the turn-on and turn-off energy of the selected semiconductor, the reverse recovery charge of the diode, the capacitor voltage of each cell, the switching frequency, and the number of cells, respectively. Δi_b can be calculated as follows:

$$i_b(u) = \frac{uV_{dc}}{N_{cell}L_b} \left(\frac{1}{N_{cells}} - u \right) \quad (5.36)$$

where L_b is the summation of the grid side and inverter inductances. The maximum current ripple can be found at $u = 0.5/N_{cell}$ as:

$$i_{b,max} = \frac{V_{dc}}{4N_{cell}^2 L_b f_{sw}} \quad (5.37)$$

u is the modulation index obtained from (5.22). Δu_i is the correction from the voltage balancing.

$$u = \frac{1}{N_{cell}V_d} \left(\frac{L_i di_i^*}{dt} + r_i i_i^* + V_{cf}^* \right) + K_\alpha V_d x_1 - K_\beta x_3 + \Delta u_i \quad (5.38)$$

The filter power losses are formulated based on the copper and core losses of the inductors and the ESR loss of the capacitor. (5.39) defines the copper loss:

$$P_{cu-filter} = R_{cu-LCL} \cdot I_{rms}^2 \quad (5.39)$$

where R_{cu-LCL} is the summation of the grid side and inverter winding resistances. The filter core loss of each inductor of the LCL filter is calculated based on the Steinmetz Equation as:

$$P_{core-filter} = K_c f_s w^x \frac{L \Delta i_{pp}}{2 N_L A_e} V_e \quad (5.40)$$

where K_c , x , and y are the parameters of the chosen magnetic material. L , A_e , and V_e are the inductance, the effective cross-section of the air, and the volume of the magnetic core, respectively. N_L is the number of inductor turns. The ESR loss is formulated in (5.41). i_c is derived from (5.3).

$$P_{ESR} = R_{est} i_c^2 \quad (5.41)$$

The total loss of the AC-DC power stage can be computed as the summation of the CHBML-AFE losses and the filter losses, as formulated in (5.42).

$$P_{lossAC-DC} = P_{con-AFE} + P_{sw-AFE} + P_{cu-filter} + P_{core-filter} + P_{ESR} \quad (5.42)$$

5.4 ISOP DAB RMS Current Minimization Derivation

A standard ISOP DAB converter is shown in Fig. 5.11. The ISOP is composed of multiple cells configured through series inputs and parallel outputs. Fig. 5.12 shows the AC side voltage of the first and second bridge voltages, V_1 and V_2 , respectively, and the inductor current, I_L , for one cell of the ISOP. D_1 and D_2 are the duty cycles of the first and second converters, respectively, and ϕ is the phase shift between V_1 and V_2 . All three parameters are defined in per-unit (pu). $D_1 = D_2 = 1$ is the case of the square wave and $\phi = 1$ is 90° phase shift. The simplest method for operation of the DAB is considering $D_1 = D_2 = 1$ and adjusting ϕ to regulate the power. This method covers the entire power capability range of the DAB,

and the RMS current is at the minimum for the same voltage level $V_1 = V_2$. However, when V_1 differs from V_2 , unnecessary RMS current and circulating power both generate losses and heat the converters and transformer. The most general and flexible method of operating the DAB is to vary all three parameters, D_1 , D_2 , and ϕ . Depending on the values of these three variables, V_1 and V_2 waveforms are different, and hence, the calculation is different. To start the calculation of the current and power, all of the possible modes or operation regions should be determined. For the theoretical analysis of both the RMS current and power loss minimization, the following assumptions are made to derive the TPS modulation scheme of a DAB module:

- The magnetizing inductance L_m is large, therefore the magnetizing current can be neglected
- The transformer turns ratio guarantees that the module is always operated in boost mode
- The commutation intervals are negligibly small in comparison to the switching cycle.

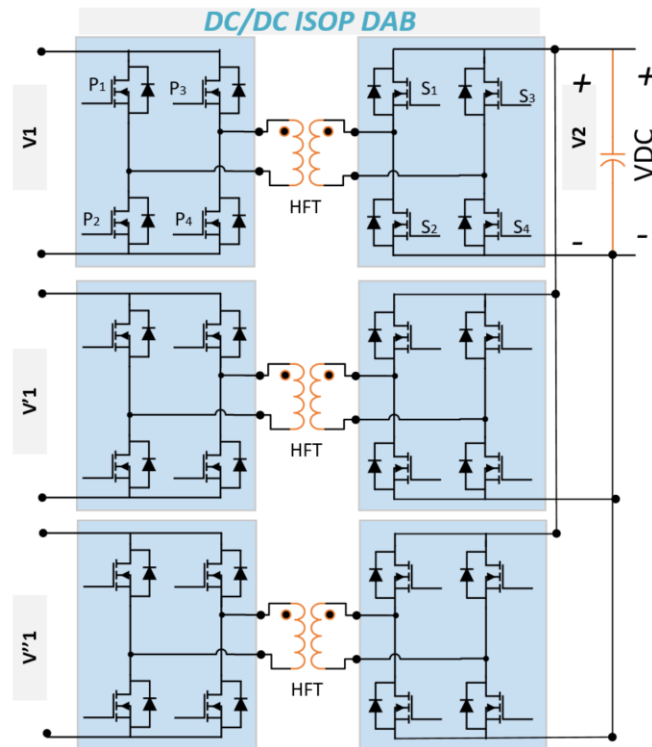


Fig. 5.11 ISOP DAB

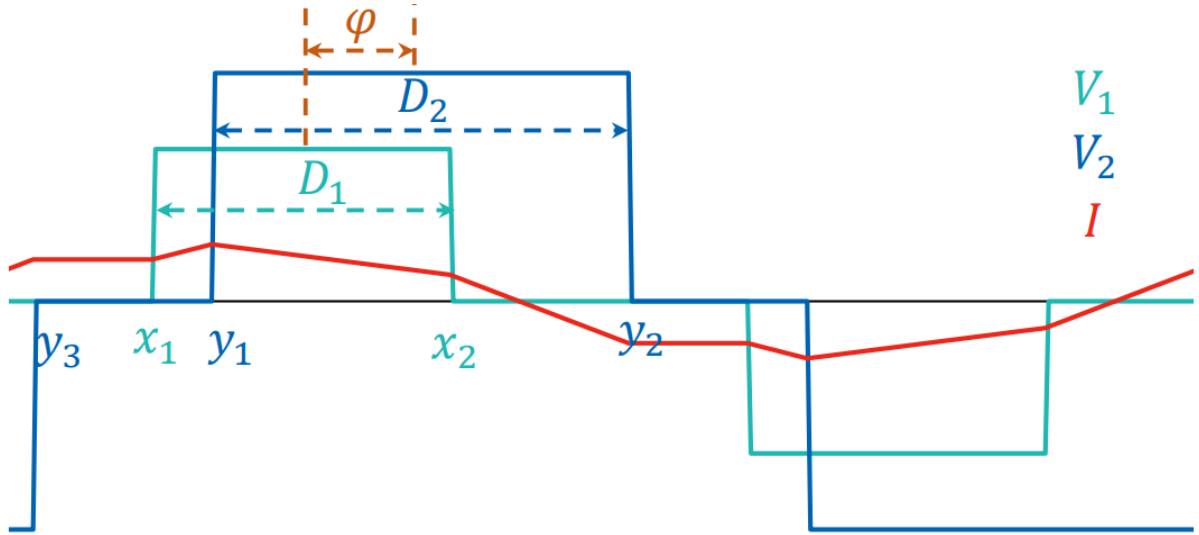


Fig. 5.12 DAB AC voltage and inductor current TPS modulation method

5.4.1 Regions of Operation

In Fig. 5.12, the rising and falling times of V_1 and V_2 are defined as x_1 , x_2 and y_1 and y_2 are the rising and falling times of V_2 . y_3 is the rising up from negative of V_2 .

$$\begin{aligned}
 x_1 &= 1 - D_1 \\
 x_2 &= 1 + D_1 \\
 y_1 &= 1 - D_2 + \phi \\
 y_2 &= 1 + D_2 + \phi \\
 y_3 &= -1 + D_2 + \phi
 \end{aligned} \tag{5.43}$$

When considering the half of the period which contains x_1 and x_2 , there are three areas in which y_1 , y_2 , and y_3 can lay. However, it is impossible to have $y_3 > x_2$, as it is a logical contradiction.

Knowing $y_3 < x_2$ eliminates a set of possibilities which are not feasible.

$$\begin{aligned}
y_3 &> x_2 \\
-1 + D_2 + \phi &> 1 + D_1 \\
-D_1 + D_2 + \phi &> 2 \rightarrow \perp
\end{aligned} \tag{5.44}$$

y_3 and y_1 cannot exist at the same time in half a period. The fact that only y_1 and y_2 or y_3 and y_1 can happen at the same time removes several possible combinations.

$$\begin{aligned}
y_3 &> 0 \\
y_2 &< 2 \\
-1 + D_2 + \phi &> 0 \\
1 + D_2 + \phi &< 2 \\
D_2 + \phi &> 1 \\
D_2 + \phi &< 1 \rightarrow \perp
\end{aligned} \tag{5.45}$$

Unlike the previous impossible combinations which describe a set of possibilities, this combination is a specific case which is a logical contradiction.

$$\begin{aligned}
y_1 &< x_1 \\
y_2 &< x_2 \\
1 - D_2 + \phi &< 1 - D_1 \\
1 + D_2 + \phi &< 1 + D_1 \\
2 + 2\phi &< 2 \rightarrow \phi < 0 \rightarrow \perp
\end{aligned} \tag{5.46}$$

This condition describes another specific impossible case:

$$y_3 > x_1$$

$$y_1 > x_2$$

$$-1 + D_2 + \phi > 1 - D_1 \quad (5.47)$$

$$1 - D_2 + \phi > 1 + D_1$$

$$2\phi > 2 \rightarrow \phi > 1 \rightarrow \perp$$

All of the remaining feasible possible combinations are considered for the derivation of the equations. The names of each region come from the three dimensional regions in which each condition is satisfied. Fig. 5.13 shows one example waveform of each region. Fig. 5.13(a) - Fig. 5.13(e) show the primary and secondary voltages of the transformer, V_1 and V_2 , respectively. Fig. 5.13(f) - Fig. 5.13(j) are the resultant currents passing through the transformer from one converter to another. Fig. 5.13(k) - Fig. 5.13(o) illustrate the instantaneous power sent from the first converter. Fig. 5.13(p) - Fig. 5.13(t) are feasible regions in a 3D space of D_1 , D_2 , and ϕ . Derivation of the “Right” (Orange) region is presented. The other regions are derived similarly. The conditions for this region are described in the following equations. The boundaries of all the regions are listed in Table 5.1.

$$x_1 < y_1 \quad -D_1 + D_2 + \phi < 0 \quad (5.48)$$

$$y_2 < x_2 \quad -D_1 + D_2 + \phi < 0 \quad (5.49)$$

$$-D_1 + D_2 - \phi < 0 \quad 1 + D_2 + \phi < 1 + D_1 \quad (5.50)$$

$$1 - D_1 < 1 - D_2 + \phi \quad (5.51)$$

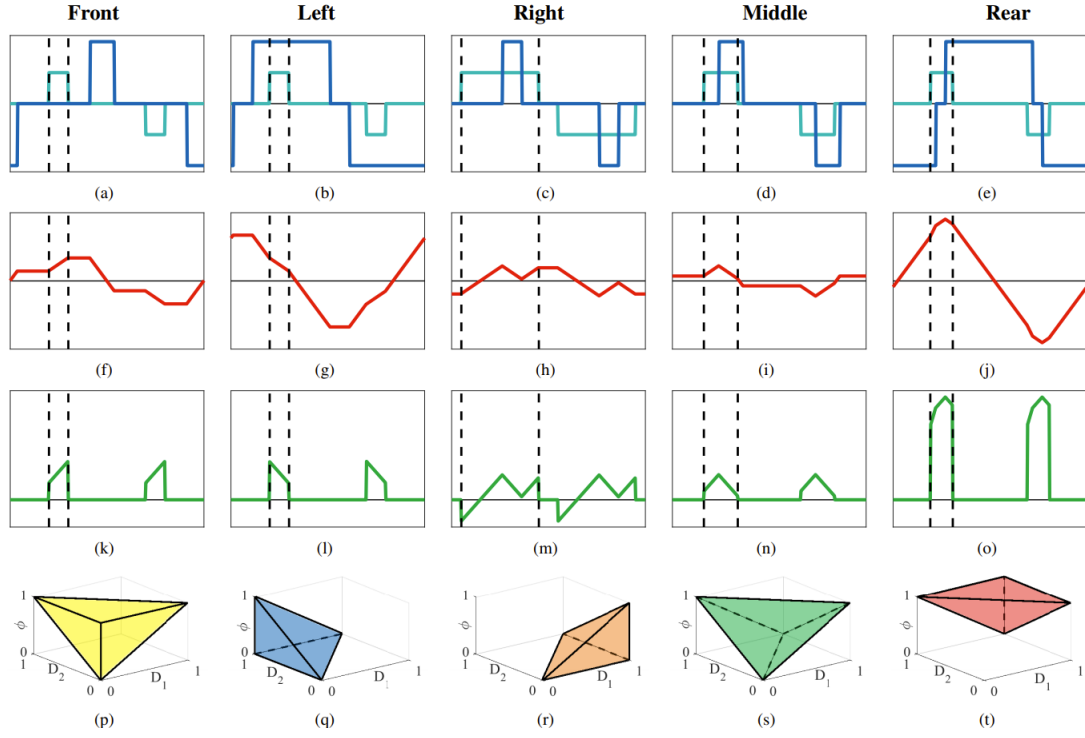


Fig. 5.13 Waveform of various modes of operation: (a) - (e) AC side voltages of the first and second converters; (f) - (j) the current from the first converter to the second; (k) - (o) power flow from the first converter to the second; and (p) - (t) boundaries of regions of the operation

Table 5.1 Boundary Regions

| | |
|--------|--------------------------------|
| Front | $D_1 + D_2 - \phi < 0$ |
| Right | $-D_1 + D_2 + \phi$ |
| Left | $D_1 - D_2 + \phi < 0$ |
| Middle | $0 \leq D_1, D_2, \phi \leq 1$ |
| Rear | $D_1 + D_2 + \phi > 2$ |

5.4.2 RMS Current and Average Power Derivation

The first step in calculating the RMS current and average power is to formulate the instantaneous expressions. The magnetizing current of the transformer is neglected in comparison to the leakage current. The instantaneous current is calculated piecewise for each region of

operation based on (5.52).

$$I_l(t) = I_0 + \frac{1}{L} \int_{Z_a}^{Z_B} (V_1(t) - V_2(t)) dt \quad (5.52)$$

In (5.52), Z_A and Z_B can be 0, x_1 , x_2 , y_1 , y_2 , y_3 , or 2, depending on the region of operation and the piece of the current. The output current may not be vertically symmetrical. However, after the transient, the current is symmetric around the x axis. Hence, the average of the current needs to be calculated and subtracted from the instantaneous current. The average calculation has been done in a piecewise manner in (5.53).

$$I_{ave} = \sum_{i=1}^8 \int_{Z_{ai}}^{Z_{Bi}} I(t) dt \quad (5.53)$$

The average power is calculated piecewise in each region from (5.54), where V_1 and I are variables, depending on the piece in each region. The RMS current is obtained from (5.55).

$$P_{ave} = \frac{1}{8} \sum_{i=1}^8 V_1(t) \int_{Z_{ai}}^{Z_{Bi}} (I(t) - I_{ave}) dt \quad (5.54)$$

$$I_{rms} = \sqrt{\frac{1}{8} \sum_{i=1}^8 \int_{Z_{ai}}^{Z_{Bi}} (I(t) - I_{ave})^2 dt} \quad (5.55)$$

The average power equation for each region is obtained in (5.56). $P_{aveFront}$, $P_{aveRight}$ and, $P_{aveLeft}$ are independent to ϕ , D_1 , and D_2 , respectively, as they could be predicted by examin-

ing Fig. 5.13(a) - Fig. 5.13(c).

$$\begin{aligned}
P_{aveFront} &= \frac{V_1 V_2}{8LF} 2D_1 D_2 \\
P_{aveRight} &= \frac{V_1 V_2}{8LF} 2D_2 \phi \\
P_{aveLeft} &= \frac{V_1 V_2}{8LF} 2D_1 \phi \\
P_{aveMiddle} &= \frac{V_1 V_2}{8LF} \left(\frac{-1}{2} (D_1 - D_2)^2 + \phi (D_1 + D_2 - \frac{1}{2} \phi) \right) \\
P_{aveRear} &= \frac{V_1 V_2}{8LF} \left(-(D_1^2 + D_2^2) - 2 + 2(D_1 + D_2) + \phi(2 - \phi) \right)
\end{aligned} \tag{5.56}$$

The expression of the average powers after the common term of $\frac{V_1 V_2}{8Lf}$ is the pu power. The following conclusions can be made from the maximum achievable pu power, as in (5.57):

$$\begin{aligned}
P_{MaxpuFront} &= 0.5 \rightarrow D_1 = D_2 = 0.5 \\
P_{MaxpuRight} &= 0.5 \rightarrow \phi = D_2 = 0.5 \\
P_{MaxpuLeft} &= 0.5 \rightarrow \phi = D_1 = 0.5 \\
P_{MaxpuMiddle} &= 0.5 \rightarrow D_1 = D_2 = 0.5, \phi = 1 \\
P_{MaxpuRear} &= 1 \rightarrow D_1 = D_2 = \phi = 1
\end{aligned} \tag{5.57}$$

There are two common terms between all of the RMS current equations which are written in (5.58) and (5.59). The RMS currents for all of the regions are obtained in (5.60) - (5.64) . Although some average powers are independent to some variables, all of the variables affect RMS current in all of the regions.

$$I_{com} = \frac{V_1}{V_2} \left(\frac{3}{2} D_1^2 - D_1^3 \right) + \frac{V_2}{V_1} \left(\frac{3}{2} D_2^2 - D_2^3 \right) \tag{5.58}$$

$$I_c = \frac{\sqrt{V_1 V_2}}{2\sqrt{2}LF} \tag{5.59}$$

$$I_{rmsFront} = I_c \left(I_{com} + 3D_1D_2(\phi - 1) \right)^{\frac{1}{2}} \quad (5.60)$$

$$I_{rmsRight} = I_c \left(I_{com} + \frac{1}{2}D_2^3 + \frac{3}{2}D_1^2D_2 + \frac{3}{2}D_2\phi^2 - 3D_1D_2 \right)^{\frac{1}{2}} \quad (5.61)$$

$$I_{rmsLeft} = I_c \left(I_{com} + \frac{1}{2}D_1^3 + \frac{3}{2}D_2^2D_1 + \frac{3}{2}D_1\phi^2 - 3D_1D_2 \right)^{\frac{1}{2}} \quad (5.62)$$

$$I_{rmsMiddle} = I_c \left(I_{com} + \frac{1}{4}(D_1^3 + D_2^3) + \frac{3}{4}D_1D_2(D_1 + D_2) - 3D_1D_2 \right. \\ \left. + \frac{3}{2}D_1D_2\phi - \frac{3}{4}(D_1^2 + D_2^2)\phi + \frac{3}{4}(D_1 + D_2)\phi^2 - \frac{1}{4}\phi^3 \right)^{\frac{1}{2}} \quad (5.63)$$

$$I_{rmsRear} = I_c \left(I_{com} + \frac{3}{2}(D_1^2 + D_2^2) - 3(D_1 + D_2) + 3(D_1 + D_2)\phi \right. \\ \left. - \frac{3}{2}(D_1^2 + D_2^2)\phi - 3\phi + \frac{3}{2}\phi^2 - \frac{1}{2}\phi^3 + 2 \right)^{\frac{1}{2}} \quad (5.64)$$

5.4.3 Optimized Trajectories

The goal of optimization is to minimize RMS current for a given average power. The variables are D_1 , D_2 , and ϕ . The objective function, f , is the RMS current which needs to be minimized. The constraint, g , is the average power which the converter should be able to provide, regardless of the current. The LM method is used for the constraint optimization problem of the DAB. Based on Lagrange optimization methodology, a Lagrange function is the combination of the objective function and the constraint, multiplied by λ , as formulated in (5.65).

$$\Lambda(D_1, D_2, \phi, \lambda) = f(D_1, D_2, \phi) + \lambda_g(D_1, D_2, \phi) \quad (5.65)$$

The optimal solution of the constraint optimization is described by a set of equations of the gradient of the LM, as written in (5.66), for the DAB. Although $\frac{\partial \Lambda}{\partial \lambda} = 0$ is part of $\nabla \Lambda = 0$, it does not reveal any new information, as it is simply the constraint function, g , itself.

$$\begin{aligned} \nabla \Lambda = 0 \rightarrow \\ \frac{\partial \Lambda}{\partial D_1} &= 0 \\ \frac{\partial \Lambda}{\partial D_2} &= 0 \\ \frac{\partial \Lambda}{\partial \phi} &= 0 \end{aligned} \tag{5.66}$$

There are five regions and each has its own f , g , and Λ . As shown in (5.66), there are three equations with four unknowns, which means there is a relationship between the variables rather than an exact value. To find the optimal trajectory in each region, λ needs to be found from one of the three equations of (5.66) and substituted in the others. The expression ϕ should be calculated from one of the remaining equations and substituted into the others. The last equation reveals the relationship between D_1 and D_2 and this relationship should be substituted back into the ϕ expression. If the relationship demonstrates a trajectory outside of the boundary of a region, the boundary is the best feasible solution.

The derivations of the optimal trajectories for all of the regions have been completed, but for each set of conditions the optimal RMS current of one of the regions is minimum. Only the derivation of the best region is presented here. Since the only region that can cover powers above $0.5pu$ is the Rear region, the comparison of regions has been done only up to $0.5pu$. For power higher than $0.5pu$, only the optimal trajectory in the Rear region needs to be derived. Fig. 5.14(b) shows the minimum RMS current that each region can provide for the range of pu power of $0 - 0.5pu$. In this figure, $V_1 = V_2$ and the best result is the Rear (red) region. The corresponding trajectory in the Rear region is shown in Fig. 5.14(r), where $D_1 = D_2 = 1$,

which is the square waveform operation. The optimal trajectories in the other regions for this condition are shown in Figs. 5.14(f), 5.14(l), 5.14(m), and 5.14(g). Fig. 5.14(s) shows the optimal trajectory regardless of region, which is identical to the optimal trajectory of the Rear region in this case. This means if the DAB is being used only for isolation purpose with $V_1 = V_2$, then the square waveform operation is the optimal operation.

Fig. 5.14(c) shows the minimum RMS current when $V_2 > V_1$. The Right and Middle regions have the minimum current and exactly the same value. In Figs. 5.14(n) and 5.14(i), the optimal trajectory lies on the boundary of the Right and Middle regions, which explains why they have the same current. The Left region has the highest current. After $0.5pu$, the only optimal trajectory is the Rear region of Fig. 5.14(t). Fig. 5.14(u) shows the overall trend that the optimal trajectory should be on the boundary of the Left and Right regions: $D_1 + D_2 + \phi = 0$ plane. For higher power, when D_1 is saturated to 1, it is on the $D_1 = 1$ plane. Eventually, when both D_1 and D_2 are saturated, it is on $D_1 = D_2 = 1$ line. A dual situation is shown in Fig. 5.14(a) when $V_2 < V_1$. The optimal trajectory for $P < 0.5\pi$ is the boundary of the Left and Middle regions or $D_1 D_2 + \phi = 0$ plane. For higher power, D_2 would be saturated to 1 and the trajectory is on $D_2 = 1$ plane up to the point where D_1 becomes saturated as well. The last part of the optimal trajectory is on $D_1 = D_2 = 1$ line. It can be observed that the optimal trajectory of any condition is never inside of a region, but always on the surface or boundary of the regions.

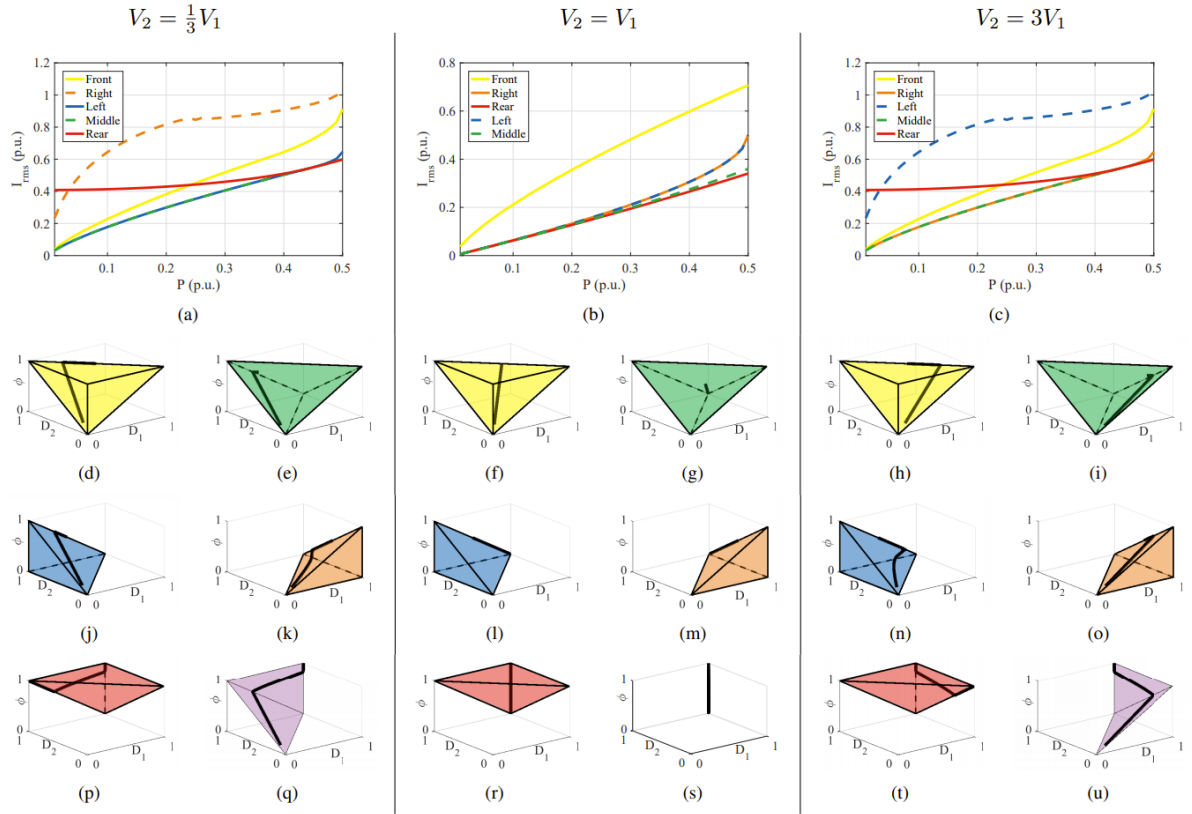


Fig. 5.14 Waveform of various modes of operation: (a) - (c) pu current for each region; (d) - (u) optimal trajectory of D_1 , D_2 and ϕ

5.4.4 Control Structure

There are three zones on the optimal trajectory, as shown in Fig. 5.15(a). These zones are discussed below. The relationship of each zone and the boundary between them is derived and shown in 5.15(b)- (d).

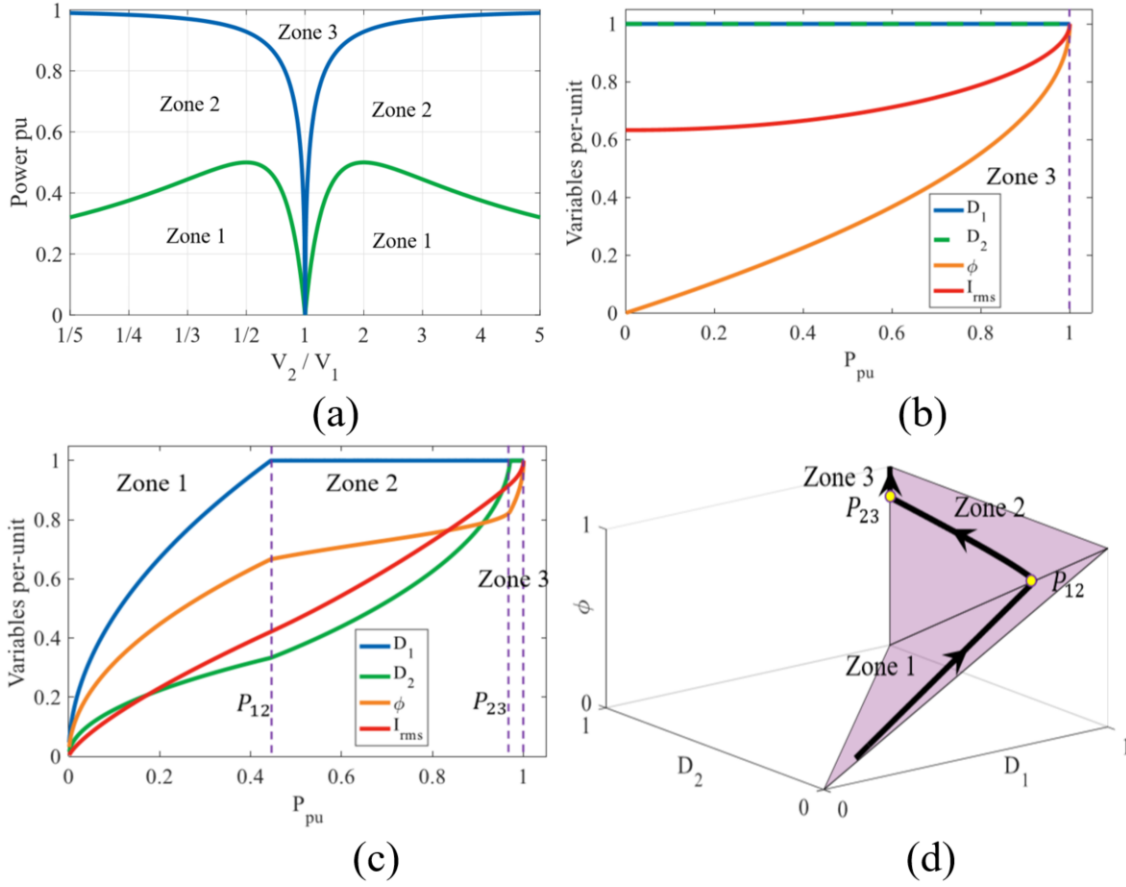


Fig. 5.15 Waveform of various modes of operation: (a) optimal zones of operation. (b)-(c) optimal pu value for D_1 , D_2 and ϕ . (d) optimal trajectory of D_1 , D_2 and ϕ

5.4.4.1 Zone 1

The first zone is low power when $D_1 D_2 \leq 1$. For $V_2 > V_1$, the optimal trajectory is on $-D_1 D_2 + \phi = 0$. Based on the Lagrange Optimization Method, $V_1 D_1 = V_2 D_2$.

$$\begin{aligned}
 \phi &= D_1 D_2 \\
 \phi &= D_1 - \frac{V_1}{V_2} D_1 \\
 D_{1z1V_2>V_1} &= \frac{V_2}{V_2 - V_1} \phi \\
 D_{2z1V_2>V_1} &= \frac{V_1}{V_2 - V_1} \phi
 \end{aligned} \tag{5.67}$$

The trajectory lies on the boundary of the Right and Middle regions, so the power equation of either of them can be used. The pu power is shown in (5.68).

$$\begin{aligned} P_{z1V_2 > V_1} &= 2D_2\phi \\ P_{z1V_2 > V_1} &= \frac{2V_1}{V_2 - V_1}\phi^2 \end{aligned} \quad (5.68)$$

This zone ends when $D_1 = 1$, which means $\phi = \frac{V_2 - V_1}{V_2}$. Substituting this ϕ into (5.68) yields P_{12} , the power at the boundary of Zones 1 and 2.

$$P_{12V_2 > V_1} = 2V_1 \frac{V_2 - V_1}{V_2^2} \quad (5.69)$$

The case of $V_2 < V_1$ is a dual of $V_2 > V_1$.

$$\begin{aligned} D_{2z1V_2 < V_1} &= \frac{V_1}{V_1 - V_2}\phi \\ D_{1z1V_2 < V_1} &= \frac{V_2}{V_1 - V_2}\phi \\ P_{z1V_2 < V_1} &= \frac{2V_2}{V_1 - V_2}\phi^2 \\ P_{12V_2 < V_1} &= 2V_2 \frac{V_1 - V_2}{V_1^2} \end{aligned} \quad (5.70)$$

5.4.4.2 Zone 2

The second zone is medium power when D_1 is reached to the limit of 1 for $V_2 > V_1$. The optimal trajectory is $D_1 = 1$ plane. By solving the LM in the Rear region and eliminating two of the equations via substitution, (5.71) can be derived. This is the solution of a quadratic

equation which relates D_2 to ϕ .

$$D_2^2 + (-2 - \frac{2V_2}{V_1}(\phi - 1))D_2 + -\phi^2 + 2\phi - 1 = 0$$

$$D_{2z_2V_2>V_1} = \frac{V_2}{V_1}(\phi - 1) + 1 + \sqrt{(\frac{V_2}{V_1}(\phi - 1) + 1)^2 + \phi^2 - 2\phi + 1}$$
(5.71)

Substituting $D_1 = 1$ and D_2 from (5.71) into the Rear region power equation gives the power in Zone 2. This zone ends when $D_2 = 1$:

$$P_{23V_2>V_1} = 2 - 2\frac{V_2^2}{V_1^2} + 2\frac{V_2}{V_1}\sqrt{\frac{V_2^2}{V_1^2} - 1}$$
(5.72)

Similarly, for the dual case of $V_2 < V_1$ the following equations can be derived:

$$D_1^2 + (-2 - \frac{2V_2}{V_1}(\phi - 1))D_1 + -\phi^2 + 2\phi - 1 = 0$$

$$D_{2z_2V_2>V_1} = \frac{V_1}{V_2}(\phi - 1) + 1 + \sqrt{(\frac{V_1}{V_2}(\phi - 1) + 1)^2 + \phi^2 - 2\phi + 1}$$

$$\phi = -\frac{V_1}{V_2} + 1 + \sqrt{\frac{V_1^2}{V_2^2} - 1}$$

$$P_{23V_2<V_1} = 2 - 2\frac{V_1^2}{V_2^2} + 2\frac{V_1}{V_2}\sqrt{\frac{V_1^2}{V_2^2} - 1}$$
(5.73)

5.4.4.3 Zone 3

The third and last zone is the high power zone when both D_1 and D_2 are saturated to 1. Varying ϕ is the only way to increase the power. Regardless of the relation between V_1 and V_2 , the power in this zone has the same equation of the square wave. This can be found by substituting $D_1 = D_2 = 1$ into the power equation of the Rear region, as is written in (5.74) .

$$P_{z3} = \phi(2 - \phi)$$
(5.74)

5.5 DAB Loss Minimization Derivation

The switching sequences, key voltages, and current waveforms under TPS conditions are presented in Fig. 5.16 for the DAB converter shown in Fig. 5.11. The DAB contains two full bridges, operating as a DC-AC and AC-DC converter, connected via a HFT. When the TPS control modulation scheme is used to regulate the DAB, the analyses can be divided into six regions, as presented in Section 5.4. However, for the purpose of calculating the total power loss of the converter, three zones are retained and defined with their respective boundary conditions. In Zone 1, which is analogous to the low power region, the power flow follows the following constraint: $0 \leq D_2 \leq \phi_1 \leq 1$. Zone 2, which is the medium power area, is defined by $0 \leq D_2 \leq D_1 \leq \phi \leq 1$. Zone 3 is the high power region with $0 \leq D_1 \leq D_2 \leq \phi \leq 1$ as the boundary condition. The different zones of operation are depicted in Fig. 5.17 - Fig. 5.19. D_1 and D_2 are the duty cycles of the first and second converters, respectively, and ϕ is the phase shift between V_1 and V_2 . The DAB converter efficiency expression will be formulated in terms of the semiconductor and HFT losses in order to minimize the total power loss. Detailed and accurate analysis of each component of the total loss is presented for each of the three zones. In order to minimize the total power loss, the efficiency of the DAB converter will be formulated in terms of the four main losses: conduction, switching, winding, and core losses based on the manipulated variables D_1 , D_2 and ϕ . Therefore, detailed analyses are carried out for each component of the DAB and for each zone of operation.

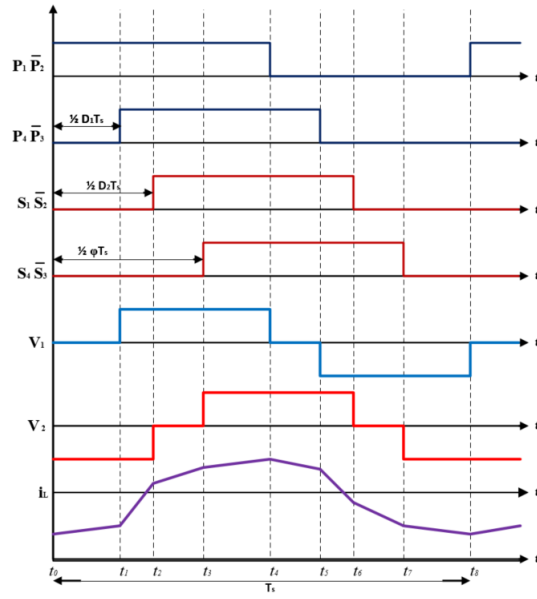


Fig. 5.16 Gates, voltages and current under TPS modulation method

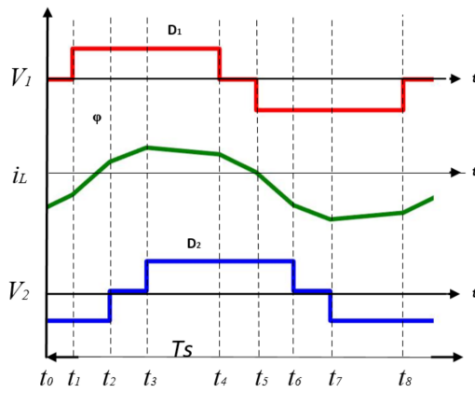


Fig. 5.17 Voltages and current waveforms for Zone 3

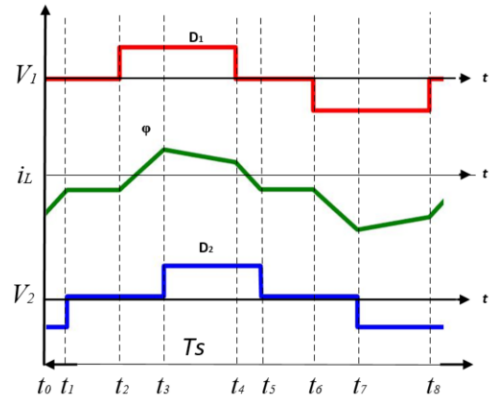


Fig. 5.18 Voltages and current waveforms for Zone 2

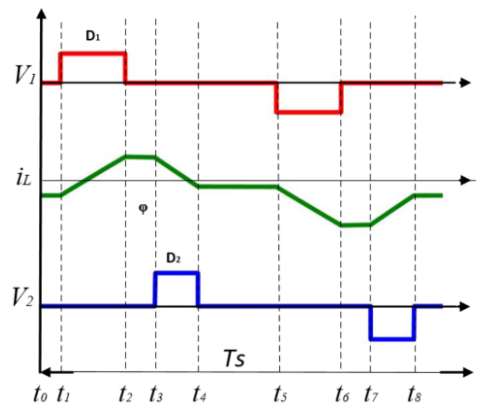


Fig. 5.19 Voltages and current waveforms for Zone 1

5.5.1 Semiconductor Power Losses

In regards to semiconductors, two types of losses are considered for this analysis: conduction and switching. Conduction losses are formulated for each semiconductor device, transistor, and diode, based on current and voltage waveforms for each interval, as demonstrated in Fig. 5.16. V_{on} represents the transistor voltage during on-state, V_d is the diode forward voltage drop, and $I_L(t_x \rightarrow t_y)$ is the current during the conduction intervals. Switching losses are calculated for each switching event, based on Fig. 5.16. V_x and V_y are the voltages at turn-on and turn-off, respectively. i_{Lpi} is the peak current during each switching event, t_f is the fall time, and C_{dev} is the snubber capacitor of the transistor. Due to fact that the converter can operate in either hard-switching or soft-switching, the ZVS constraint is established when the i_l zero crossing is within the time interval where V_1 and V_2 have opposite polarities. When the converter is operating under soft-switching, only turn-off losses are calculated. When the converter is working under hard-switching, turn-on losses are also considered. The governing equations for the conduction and switching losses are formulated in (5.75) and (5.76).

$$P_{cond} = \frac{1}{T_s} \int_{t_x}^{t_y} |I_{L(tx \rightarrow ty)}| V_{on} dt + \frac{1}{T_s} \int_{t_x}^{t_y} |I_{L(tx \rightarrow ty)}| V_d dt \quad (5.75)$$

$$P_{sw} = \frac{1}{2} V_x i_{Lpi} t_f f_s + \frac{1}{2} C_{dev} V_y^2 f_s \quad (5.76)$$

5.5.1.1 Zone 3

In order to formulate the DAB power losses for high power operation in Zone 3, as depicted in Fig. 5.17, the currents at each of the switching events are formulated, as in (5.77), and the

currents at each interval during conduction are formulated, as in (5.78).

$$\begin{aligned}
i_{lp1} &= -I_{lp}(t_0) = I_{lp}(t_4) = -I_{lp}(t_8) = \frac{V_1(1 - D_1) + V_2(\phi + D_2 - 1)}{4Lf_s} \\
i_{lp2} &= -I_{lp}(t_1) = I_{lp}(t_5) = \frac{V_1(D_1 - 1) + V_2(1 + \phi - 2D_1 + D_2)}{4Lf_s} \\
i_{lp3} &= I_{lp}(t_2) = -I_{lp}(t_6) = \frac{V_1(-1 - D_1 + 2D_2) + V_2(1 + \phi - D_2)}{4Lf_s} \\
i_{lp4} &= I_{lp}(t_3) = -I_{lp}(t_7) = \frac{V_1(-1 - D_1 + 2\phi) + V_2(1 + \phi - D_2)}{4Lf_s}
\end{aligned} \tag{5.77}$$

$$\begin{aligned}
I_{L(t0 \rightarrow t1)} &= \frac{V_1(D_1 - 1) - V_2(\phi - 2D_1 + D_2 - 1)}{4Lf_s} \\
I_{L(t1 \rightarrow t2)} &= \frac{V_1(D_1 - 2D_2 - 1) - V_2(\phi - D_2 - 1)}{4Lf_s} \\
I_{L(t2 \rightarrow t3)} &= \frac{V_1(D_1 - 2\phi - 1) - V_2(\phi - D_2 - 1)}{4Lf_s} \\
I_{L(t3 \rightarrow t4)} &= \frac{V_1(1 - D_1) - V_2(1 + \phi + D_2)}{4Lf_s} \\
I_{L(t4 \rightarrow t5)} &= \frac{V_1(1 - D_1) - V_2(1 + \phi - 2D_1 + D_2)}{4Lf_s} \\
I_{L(t5 \rightarrow t6)} &= \frac{V_1(1 + D_1 - 2D_2) - V_2(1 + \phi - D_2)}{4Lf_s} \\
I_{L(t6 \rightarrow t7)} &= \frac{V_1(1 + D_1 - 2\phi) - V_2(1 + \phi - D_2)}{4Lf_s} \\
I_{L(t7 \rightarrow t8)} &= \frac{V_1(D_1 - 1) - V_2(-1 + \phi + D_2)}{4Lf_s}
\end{aligned} \tag{5.78}$$

The final conduction and switching losses for Zone 3 are obtained by substituting (5.77) and (5.78) into (5.75) and (5.76).

$$P_{SW} = \frac{V_1 t_f |V_1 - V_2 + \phi V_2 + D_1 V_1 - 2D_2 V_1 - D_2 V_2| + V_2 t_f |V_1 - V_2 + \phi V_2 - D_1 V_1 + D_2 V_2|}{8L} \tag{5.79}$$

$$P_{cond} = \frac{V_f A}{2Lf_s^2} - \frac{V_f B}{2Lf_s^2} - \frac{\sqrt{2}R_{ds}(V_1 V_2(C + E + F) + V_2^2 G + V_1^2 H)}{96Lf_s^2} + \frac{V_f D_1 I}{2Lf_s^2} - \frac{V_f J}{2Lf_s^2} \tag{5.80}$$

where

$$\begin{aligned}
A &= |(\phi - 1)(1 - D_1 V_1 + D_2 V_2)| \\
B &= |(1 - \phi + D_2)V_2 + (\phi - D_1 + D_2 - 1)V_1|(D_2 - \phi) \\
C &= -4D_1^3 - 6D_1 D_2^2 + 6D_1^2 D_2 + 6D_1^2 \phi \\
E &= -6D_1^2 + 6D_1 D_2 - 6D_2^2 - 6D_1 \phi^2 + 6D_1 \phi \\
F &= 4D_2^3 + 4\phi^3 - 6\phi^2 + 2 \\
G &= 3(D_2 - \phi)^2 + 2(D_2 - \phi)^3 - 1 \\
H &= 3D_1^2 - 1 - 2D_1^3 \\
I &= |V_1(1 - D_1) + (-1 + \phi - D_1 + D_2)V_2| \\
J &= |V_2(-\phi + D_1) + (-1 + D_2)V_1|(D_1 - D_2)
\end{aligned}$$

5.5.1.2 Zone 2

Similar to Zone 3, for Zone 2 the currents at each of the switching events are formulated, as in (5.81), and the currents at each interval during conduction are formulated, as in (5.82). Fig. 5.18 depicts Zone 2.

$$\begin{aligned}
i_{lp1} &= -I_{lp}(t_0) = I_{lp}(t_4) = -I_{lp}(t_8) = \frac{V_1(1 - D_1) + V_2(\phi + D_2 - 1)}{4Lf_s} \\
i_{lp2} &= -I_{lp}(t_1) = -I_{lp}(t_2) = I_{lp}(t_5) = -I_{lp}(t_6) = \frac{V_1(D_1 - 1) + V_2(1 + \phi - 2D_1 + D_2)}{4Lf_s} \\
i_{lp3} &= I_{lp}(t_3) = -I_{lp}(t_7) = \frac{V_1(-1 - D_1 + 2D_2) + V_2(1 + \phi - D_2)}{4Lf_s}
\end{aligned} \tag{5.81}$$

$$\begin{aligned}
I_{L(t0 \rightarrow t1)} &= \frac{V_1(D_1 - 1) + V_2(1 + D_2 - \phi)}{4Lf_s} \\
I_{L(t1 \rightarrow t2)} &= \frac{V_1(D_1 - 1) + V_2(D_2 - \phi + 1)}{4Lf_s} \\
I_{L(t2 \rightarrow t3)} &= \frac{V_1(2\phi - D_1 - 1) - V_2(\phi - 1 - D_2)}{4Lf_s} \\
I_{L(t3 \rightarrow t4)} &= \frac{V_1(1 - D_1) + V_2(-1 + \phi + D_2)}{4Lf_s} \\
I_{L(t4 \rightarrow t5)} &= \frac{V_1(1 - D_1) + V_2(\phi - D_2 - 1)}{4Lf_s} \\
I_{L(t5 \rightarrow t6)} &= \frac{V_1(1 - D_1) + V_2(\phi - D_2 - 1)}{4Lf_s} \\
I_{L(t6 \rightarrow t7)} &= \frac{V_1(1 + D_1 - 2\phi) + V_2(1 + \phi - D_2)}{4Lf_s} \\
I_{L(t7 \rightarrow t8)} &= \frac{V_1(D_1 - 1) + V_2(-1 + \phi + D_2)}{4Lf_s}
\end{aligned} \tag{5.82}$$

The final conduction and switching losses for Zone 2 are obtained by substituting (5.81) and (5.82) into (5.75) and (5.76).

$$P_{SW} = \frac{|(V_1 t_f (V_1(1 - D_1) + V_2(D_2 + \phi - 1)))| + |(V_2 t_f (V_2(1 - \phi + D_2) + V_1(D_1 - 1)))|}{8L} \tag{5.83}$$

$$P_{cond} = \frac{V_f A}{2Lf_s^2} - \frac{R_{ds}(V_1 V_2(B + C) + V_2^2 E + V_1^2 F)}{3Lf_s^2} - \frac{V_f D_1 G}{2Lf_s^2} - \frac{V_f H}{2Lf_s^2} + \frac{D_2 V_f I}{2Lf_s^2} \tag{5.84}$$

where

$$A = |(\phi - 1)(V_1(\phi - D_1) + D_2V_2)|$$

$$B = -6D_1^2D_2 + 6D_1^2\phi - 6D_1^2 + 6D_1D_2^2 + 6D_1D_2$$

$$C = -6D_1\phi^2 + 6D_1\phi - 6D_2^2 + 4\phi^3 - 6\phi^2 + 2$$

$$E = 2D_2^3 - 6D_2^2\phi + 3D_2^2 + 6D_2\phi^2 - 6D_2\phi - 2\phi^3 + 3\phi^2 - 1$$

$$F = -1 - 2D_1^3 + 3D_1^2$$

$$G = |V_2(-\phi + D_2 + 1) + V_1(\phi - 1)|(D_1 - \phi)$$

$$H = |V_2(-\phi + D_2 + 1) + V_1(D_1 - 1)|(D_1 - D_2)$$

$$I = |V_1(1 - D_1) + V_2(\phi - 1)|$$

5.5.1.3 Zone 1

Similar to Zones 3 and 2, for Zone 1 the currents at each switching event are formulated, as in (5.85), and the currents at each interval during conduction are formulated, as in (5.86). Fig. 5.19 depicts Zone 1.

$$\begin{aligned} i_{lp1} &= -I_{lp}(t_0) = I_{lp}(t_4) = -I_{lp}(t_8) = \frac{V_1(1 - D_1) + V_2(\phi + D_2 - 1)}{4Lf_s} \\ i_{lp2} &= -I_{lp}(t_1) = -I_{lp}(t_2) = I_{lp}(t_5) = -I_{lp}(t_6) = \frac{V_2(1 + D_2 - \phi) + V_1(D_1 - 1)}{4Lf_s} \\ i_{lp3} &= I_{lp}(t_3) = -I_{lp}(t_7) = \frac{V_2(1 - 2D_1 + \phi + D_2) + V_1(D_1 - 1)}{4Lf_s} \end{aligned} \quad (5.85)$$

$$\begin{aligned}
I_{L(t0 \rightarrow t1)} &= \frac{V_1(D_1 - 1) + V_2(1 - \phi + D_2)}{4Lf_s} \\
I_{L(t1 \rightarrow t2)} &= \frac{V_1(D_1 - 1) + V_2(1 - \phi + D_2)}{4Lf_s} \\
I_{L(t2 \rightarrow t3)} &= \frac{V_1(D_1 - 1) + V_2(1 + \phi - 2D_1 + D_2)}{4Lf_s} \\
I_{L(t3 \rightarrow t4)} &= \frac{V_1(1 - D_1) - V_2(\phi + D_2 - 1)}{4Lf_s} \\
I_{L(t4 \rightarrow t5)} &= \frac{V_1(1 - D_1) - V_2(1 - \phi + D_2)}{4Lf_s} \\
I_{L(t5 \rightarrow t6)} &= \frac{V_1(1 - D_1) - V_2(1 - \phi + D_2)}{4Lf_s} \\
I_{L(t6 \rightarrow t7)} &= \frac{V_1(1 - D_1) - V_2(1 + \phi - 2D_1 + D_2)}{4Lf_s} \\
I_{L(t7 \rightarrow t8)} &= \frac{V_1(D_1 - 1) - V_2(\phi + D_2 - 1)}{4Lf_s}
\end{aligned} \tag{5.86}$$

The final conduction and switching losses for Zone 1 are obtained by substituting (5.85) and (5.86) into (5.75) and (5.76).

$$P_{SW} = \frac{(|V_1 t_f (V_1(1 - D_1) + V_2(\phi + D_2 - 1))| + |V_2 t_f (V_2(1 + D_2 - \phi) + V_1(D_1 - 1))| + A}{8L} \tag{5.87}$$

where

$$A = 4C_{dev} f_s L (V_1^2 + V_2^2)$$

$$P_{cond} = \frac{V_f A}{2L f_s^2} - \frac{V_f B}{2L f_s^2} - \frac{R_{ds} (2V_1 V_2 (C + D) + V_2^2 (E + F) + V_1^2 G)}{3L f_s^2} - \frac{V_f |V_2| H}{2L f_s^2} \tag{5.88}$$

where

$$A = D_2|V_1(1 - D_1) + V_2(\phi - 1)|$$

$$B = |V_2(1 + D_2 - \phi) + V_1(D_1 - 1)|(D_2 - \phi)$$

$$C = 2D_1^3 - 3D_1^2D_2 - 3D_1^2\phi - 3D_1^2 + 3D_1D_2^2 - 3\phi^2$$

$$D = 3D_1D_2 + 3D_1\phi^2 + 3D_1\phi - 3D_2^2 + 1$$

$$E = 2D_2^3 - 6D_2^2\phi + 3D_2^2 + 6D_2\phi^2$$

$$F = -6D_2\phi - 2\phi^3 + 3\phi^2 - 1$$

$$G = 3D_1^2 - 2D_1^3$$

$$H = (D_1 - 1)(D_2 - D_1 + \phi)$$

5.5.2 HFT Power Losses

The transformer losses are the total sum of the core and winding losses. To obtain the winding loss, the RMS current is determined and both the skin and proximity effect are considered for calculating R_{eff} . Due to the non-sinusoidal waveform characteristic for the given applications, the Improved Generalized Steinmetz Equation (IGSE) [214] is used to obtain the closed form expression for the core loss. The driving equations for the winding and core losses are formulated in (5.89) and (5.90), respectively.

$$P_{W_{loss}} = R_{eff}I_{rms}^2 \quad (5.89)$$

where

$$R_{eff} = \frac{MLT_w N}{\pi \sigma r_l^2 N_s} \left(1 + \frac{\pi^2 N_s \beta}{192} \left(16m^2 - 1 + \frac{24}{\pi^2} \right) \left(\frac{r_l}{\sigma} \right)^4 \right)$$

$$P_{core} = \frac{1}{T_s} \int_0^{T_s} K_i \left| \frac{dB(t)}{dt} \right|^\gamma (\Delta B)^{\theta-\gamma} dt \quad (5.90)$$

where

$$K_i = \frac{2^{1-\theta} K_s \pi^{1-\gamma}}{\frac{1.7061}{\gamma+1.354} + 0.2761}$$

In order to obtain the final expression for the winding losses, the RMS current for each zone needs to be calculated using the expression (5.55). By substituting (5.91), (5.92) and (5.93) into (5.89), the winding losses expressions are obtained in (5.94)

$$I_{rms-Z3} = \frac{\sqrt{3}}{3} \frac{\left(4V_1 V_2 (A + B) + 2V_1^2 C + 2V_2^2 (D - 6E + 3F - 1) \right)^{\frac{1}{2}}}{4L f_s} \quad (5.91)$$

where

$$A = 3D_1(D_1 D_2 + D_1 \phi - D_1 - D_2^2 + D_2 + \phi - \phi^2)$$

$$B = 3(D_2^3 - D_2^2 - \phi^2) + 2(\phi^3 - D_1^3) + 1)$$

$$C = 3D_1^2 - 2D_1^3 - 1$$

$$D = 2(D_2^3 - \phi^3)$$

$$E = D_2^2 \phi + D_2 \phi^2 - D_2 \phi$$

$$F = (\phi^2 + D_2^2)$$

$$I_{rms-Z2} = \frac{\sqrt{3}}{3} \frac{\left(2V_1V_2(A) + 2V_1^2B + 2V_2^2(C - 6D + 3E - 1) \right)^{\frac{1}{2}}}{4Lf_s} \quad (5.92)$$

where

$$A = (6(D_1^2\phi - D_1^2D_2 - D_1^2 + D_1D_2^2 + D_1D_2 - D_1\phi^2 + D_1\phi - D_2^2 - \phi^2) + 4\phi^3 + 2)$$

$$B = 3D_1^2 - 2D_1^3 - 1$$

$$C = 2(D_2^3 - \phi^3)$$

$$D = D_2^2\phi + D_2\phi^2 - D_2\phi$$

$$E = (\phi^2 + D_2^2)$$

$$I_{rms-Z1} = \frac{\sqrt{3}}{3} \frac{\left(V_1V_2(A) - V_1^2B + V_2^2C \right)^{\frac{1}{2}}}{4Lf_s} \quad (5.93)$$

where

$$A = (4D_1^3 + 6(D_1^2D_2 + D_1^2\phi + D_1^2 - D_1D_2^2 - D_1D_2 - D_1\phi^2 - D_1\phi + D_2^2 + \phi^2) - 2)$$

$$B = 3D_1^2 - 2D_1^3 - 1$$

$$C = 2D_2^3 - 6D_2^2\phi + 3D_2^2 + 6D_2\phi^2 - 6D_2\phi - 2\phi^3 + 3\phi^2 - 1$$

$$P_{Wloss} = R_{eff} I_{rms-Z3}^2$$

$$P_{Wloss} = R_{eff} I_{rms-Z2}^2 \quad (5.94)$$

$$P_{Wloss} = R_{eff} I_{rms-Z1}^2$$

The core losses are formulated for each zone, as follows:

$$P_{core-Z3} = K_i(2B_m)^{\theta-\gamma} \left(A(B_m f_s)^\gamma (2^\gamma + 4^\gamma) + B(E^\gamma + F^\gamma) + C(\gamma + (D^\gamma)) \right) \quad (5.95)$$

$$\begin{aligned} A &= \frac{T_s}{2} - \frac{\phi T_s}{2} & B &= \frac{D_2 T_s}{2} - \frac{D_1 T_s}{2} \\ C &= \frac{\phi T_s}{2} - \frac{D_2 T_s}{2} & D &= \frac{4B_m f_s}{\phi} \\ E &= \frac{2B_m}{\frac{D_2 T_s}{2} + \frac{T_s}{2}} & F &= \frac{4B_m f_s}{D_2} \end{aligned}$$

$$P_{core-Z2} = K_i(2B_m)^{\theta-\gamma} \left(A(B_m f_s)^\gamma (2^\gamma + 4^\gamma) + B(C^\gamma + D^\gamma) \right) \quad (5.96)$$

$$\begin{aligned} A &= \frac{T_s}{2} - \frac{\phi T_s}{2} & B &= \frac{\phi T_s}{2} - \frac{D_1 T_s}{2} \\ C &= \frac{2B_m}{\frac{\phi T_s}{2} + \frac{T_s}{2}} & D &= \frac{4B_m f_s}{\phi} \end{aligned}$$

$$P_{core-Z1} = K_i(2B_m)^{\theta-\gamma} \left(\left(\frac{T_s}{2} - \frac{D_1 T_s}{2} \right) (B_m f_s)^\gamma (2^\gamma + 4^\gamma) \right) \quad (5.97)$$

The average power transfer expressions for each of the zones are expressed in (5.98) - (5.100).

$$P_{ave-Z3} = \frac{V_1 V_2 (D_1 (D_2 + \phi - 1) - D_1^2 - D_2^2 + D_2 - \phi^2 + \phi)}{4L f_s} \quad (5.98)$$

$$P_{ave-Z2} = \frac{V_1 V_2 (D_2 - \phi^2 + \phi - D_1 (D_2 - \phi + 1))}{4L f_s} \quad (5.99)$$

$$P_{ave-Z1} = \frac{V_1 V_2 (1 - D_1)(D_2 - D_1 + \phi)}{4L f_s} \quad (5.100)$$

5.6 DAB Control Optimization and Trajectories

The goal of optimization is to minimize the total power loss for a given average power. The variables are D_1 , D_2 , and ϕ . The objective function, f , is the total power loss which needs to be minimized and the constraint, g , is the average power the converter should be able to provide. Two optimization methods have been used, the LM and PSO. Due to the nonlinearity of the system, in certain power regions it is extremely difficult to obtain a closed loop form for the optimal degree of freedom. In such a case, PSO is utilized to obtain an optimal numerical value for the degree of freedom. This case is also referred to as local optimization (LO). However, in other power regions it is possible to obtain a closed loop form for the optimal degree of freedom. In this case the LM method is used for the constraint optimization problem of the DAB. This case is also referred to as global optimization (GO). Contrary to the LO method, the GO method covers multiple target functions, such as peak current stress, RMS current, and total power loss. For each of the modes and power regions where GO is feasible, as summarized in Table 5.2, the corresponding average power transferred and the objective function can be used to obtain the closed form expressions, according to (5.65) and (5.66)

Table 5.2 Optimization methods based on the power regions

| $V_1 < V_2$ | Zone 1 | Zone 2 | Zone 3 |
|--------------------|------------|------------|------------|
| Objective function | Power Loss | Power Loss | Power Loss |
| Methods | PSO | PSO | LM |
| Global | False | False | True |
| Local | True | True | False |

In Zone 3, GO exists. Therefore, the closed form expressions for minimizing the power loss can be obtained. For the sake of simplicity, the peak current stress (i_{lp1}) from (5.77) is chosen as the objective function and the corresponding average power for Zone 3 (5.98) is used. Substituting the pu expressions, as formulated in (5.101) and (5.102), into (5.65) and (5.66), yields the closed form expressions for D_1 and D_2 formulated in (5.103) and (5.104), where $K = \frac{2V_1}{V_2}$. The rated values of the power and the peak current are computed, as follows:

$$P_r = \frac{V_1 V_2}{8L f_s} \text{ and } I_r = \frac{V_2}{8L f_s}$$

$$P_{ave-Z3pu} = 2(D_2 - D_1 + \phi - \phi^2 - D_1 D_2 + D_1 \phi) \quad (5.101)$$

$$I_{lp1} = \frac{2V_1}{V_2}(1 - D_1) + (\phi + D_2 - 1) \quad (5.102)$$

$$D_{1V_2 > V_1} = 2\phi + \frac{24D_2 - 24D_2^2 + 4K(6D_2^2 - 6D_2 + 1) - 4}{2\sqrt{A + 2B + C} - 8D_2 + 4} - 1 \quad (5.103)$$

where

$$A = K^2(6D_2 - 6D_2^2 - 1)$$

$$B = K(6D_2^2 - 6D_2 + 1)$$

$$C = 8D_2(1 - D_2)$$

$$D_{2V_2 > V_1} = 2D_1(4 + K^2 - 6K) + \phi(6K - K^2 - 4) + (2K - 2)^2 + \sqrt{2K}D \quad (5.104)$$

where

$$A = K^2(-3(2D_1 - \phi)^2) - 6D_1 + 3\phi + 1$$

$$B = K(12D_1 - 6\phi - 1 + 6(2D_1 - \phi)^2)$$

$$C = 8D_1(2\phi - 2D_1 - 1) + 4\phi(1 - \phi)$$

$$D = \frac{\sqrt{A + B + C}}{5(7K^2 - 10K + 4)}$$

5.6.1 Optimization Trajectory for Zone 3

For GO, the optimal D_1 , D_2 and ϕ for power loss minimization are the same for the RMS current minimization and the peak current minimization. The boundary and optimal trajectory for the high power region (Zone 3) are shown in Figs. 5.20 - 5.23. For Zone 3, it can be seen that the optimal duty cycles for both the primary and the secondary sides are between $0.7 \leq D_1, D_2 \leq 1$. The analytical average power transfer, total power loss, and the efficiency calculation based on the optimal TPS variables, are shown in Fig. 5.22. The overall loss breakdown for this region is shown in Fig. 5.23

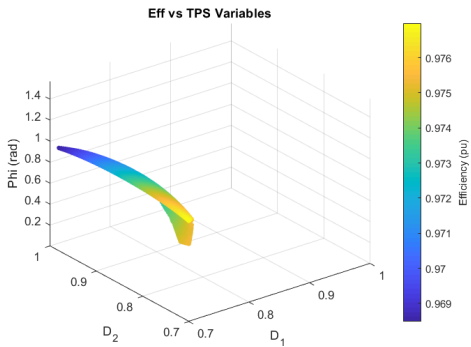


Fig. 5.20 Optimal control variables vs. efficiency

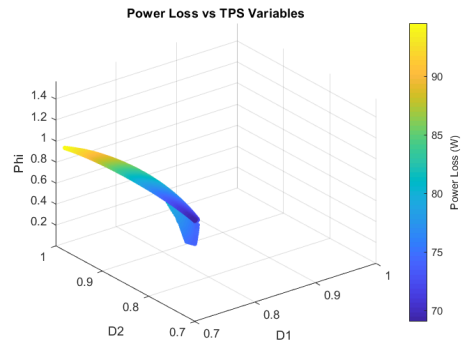


Fig. 5.21 Optimal control variables vs. power losses

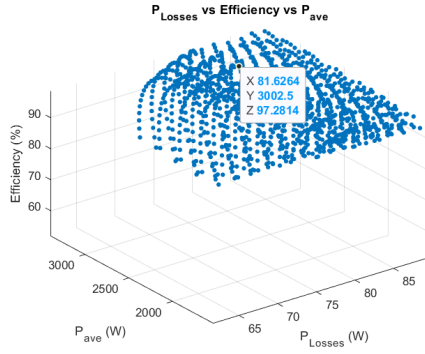


Fig. 5.22 Analytical average power, efficiency, and power loss calculation

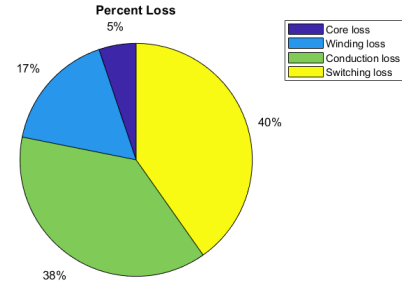


Fig. 5.23 Loss breakdown for Zone 3

5.6.2 Optimization Trajectory for Zone 2

In Zone 2, GO is not applicable due to the fact that the optimal variables that minimize the power loss are different from the optimal variables that minimizes the RMS current or the peak current. Therefore, in Zone 2, LO is used to obtain the optimal TPS variables. The boundary and optimal trajectory for the medium power region (Zone 2) are shown in Figs. 5.24 - 5.27. For Zone 2, it can be seen that the optimal duty cycles for both the primary and secondary sides are between $0.5 \leq D_1, D_2 \leq 0.7$. The analytical average power transfer, total power loss, and efficiency calculation based on the optimal TPS variables are shown in Fig. 5.26. The overall loss breakdown for this region is shown in Fig. 5.27

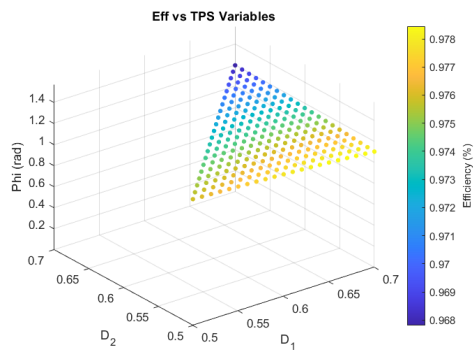


Fig. 5.24 Optimal control variables vs. efficiency

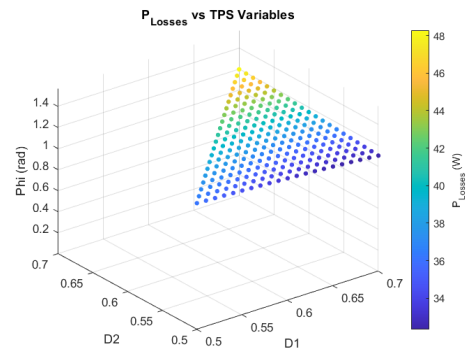


Fig. 5.25 Optimal control variables vs. power losses

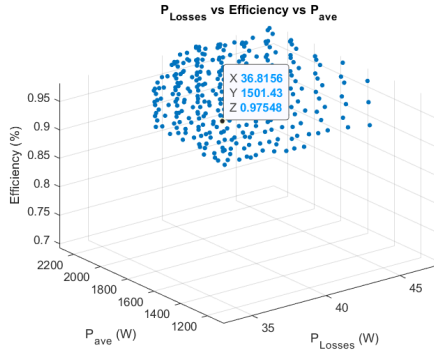


Fig. 5.26 Analytical average power, efficiency (pu), and power loss calculation

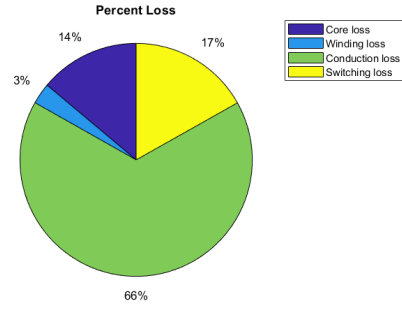


Fig. 5.27 Loss breakdown for Zone 2

5.6.3 Optimization Trajectory for Zone 1

In zone 1, GO is not applicable due to the fact that the optimal variables that minimize the power loss are different from the optimal variables that minimizes the RMS current or the peak current. Therefore, in Zone 1, LO is used to obtain the optimal TPS variables. The boundary and the optimal trajectory for the low power region in Zone 1 are shown in Figs. 5.28 - 5.31. For the low power zone, it can be seen that the optimal duty cycles for both the primary and secondary sides are between $0.0 \leq D_1, D_2 \leq 0.5$. The analytical average power transfer, total power loss, and efficiency calculation based on the optimal TPS variables are shown in Fig. 5.30. The overall loss breakdown for this region is shown in Fig. 5.31

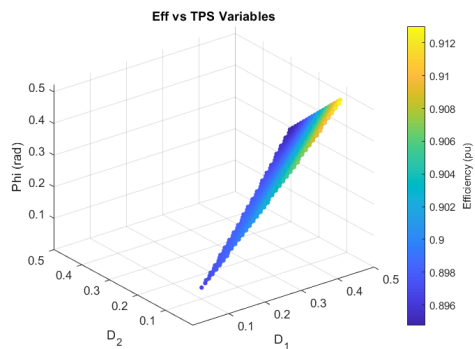


Fig. 5.28 Optimal control variables vs. efficiency

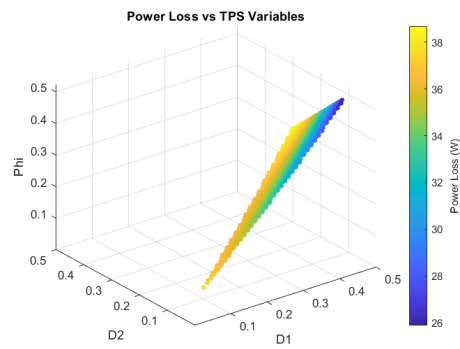


Fig. 5.29 Optimal control variables vs. power losses

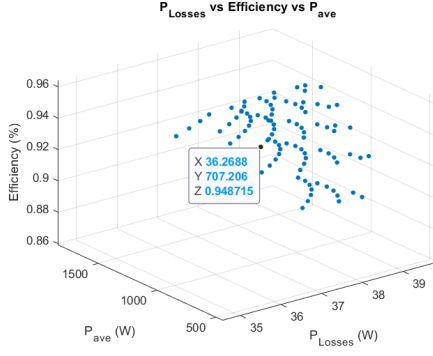


Fig. 5.30 Analytical average power, efficiency (pu), and power loss calculation

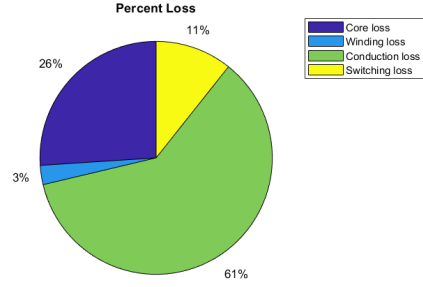


Fig. 5.31 Loss breakdown for Zone 1

The flowchart of the offline PSO technique is presented in Fig. 5.32. This method is used for obtaining the optimal control variables for Zones 1 and 2. The PSO formulation comprises two principal equations, as seen in (5.105) and (5.106), where X is defined as particle positions (TPS variables), and V as the particle velocity that is used to modify the particle position X for every iteration. P_{best} is the best remembered individual particle position and G_{best} is the best remembered swarm position. k is the iteration index, c_1 and c_2 are positive constants, and r_1 and r_2 are two randomly generated numbers, such that $0 \leq r_1, r_2 \leq 1$ [215].

$$X_i^{k+1} = X_i^k + V_i^{k+1} \quad (5.105)$$

$$V_i^{k+1} = V_i^k + C_1 r_1 (P_{best_i}^k - X_i^k) + c_2 r_2 (G_{best}^k - X_i^k) \quad (5.106)$$

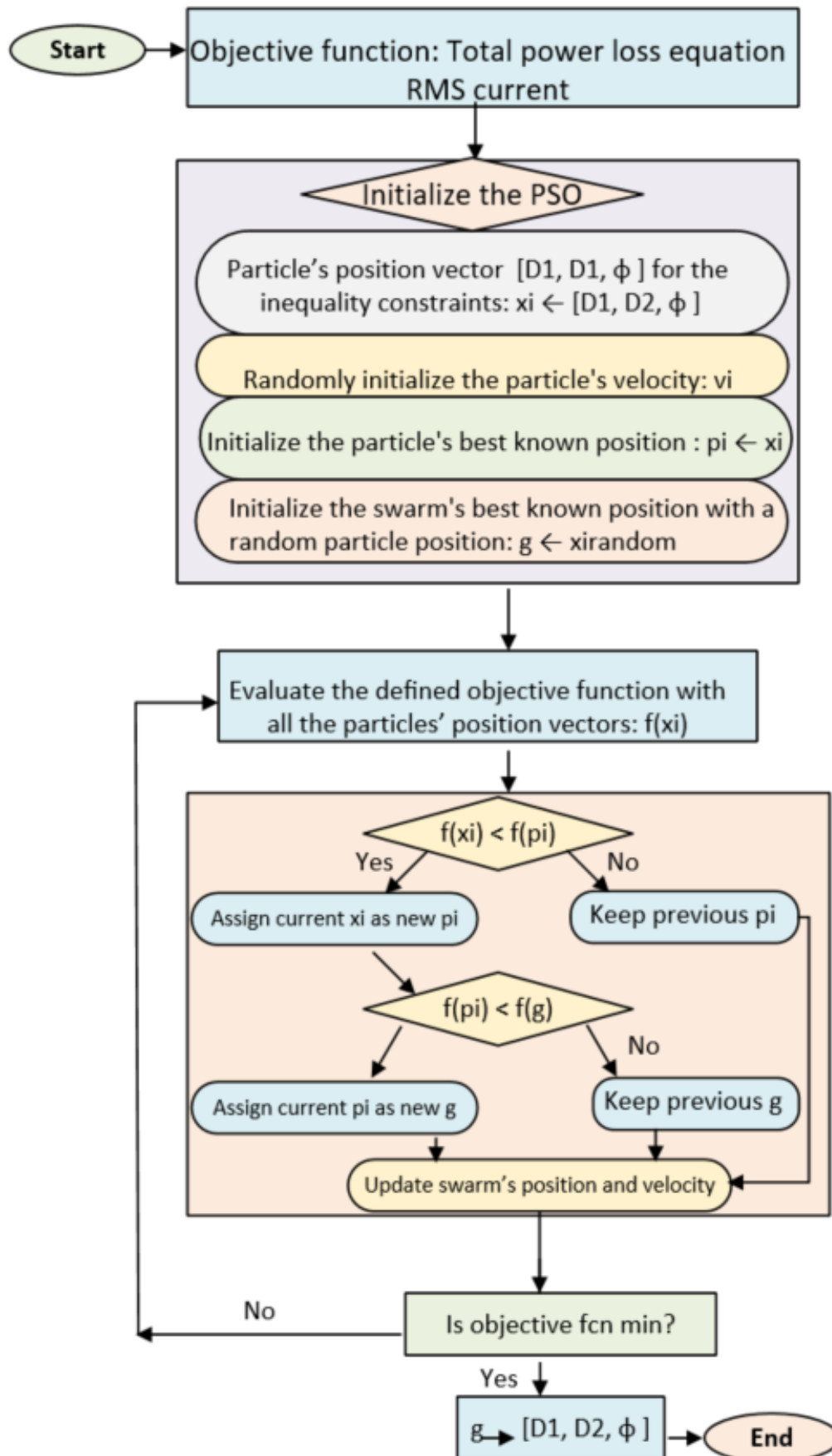


Fig. 5.32 PSO flow chart

5.7 DAB Control Structure

The optimal closed loop control for the ISOP DAB converter is shown in Fig. 5.33. This figure depicts both the buck and boost operation modes of the ISOP DAB converter. The voltage PI controller generates the initial phase shift ϕ_i . In order to estimate the average power transferred from the primary to the secondary bridge, ϕ_i is applied in the optimal control variable generation block. The operating zone is then determined according to the estimated average power. The optimal $D_{1_{opt}}$ and $D_{2_{opt}}$ are calculated either from (5.103) and (5.104) or are chosen from the PSO look-up table for the other operating zones.

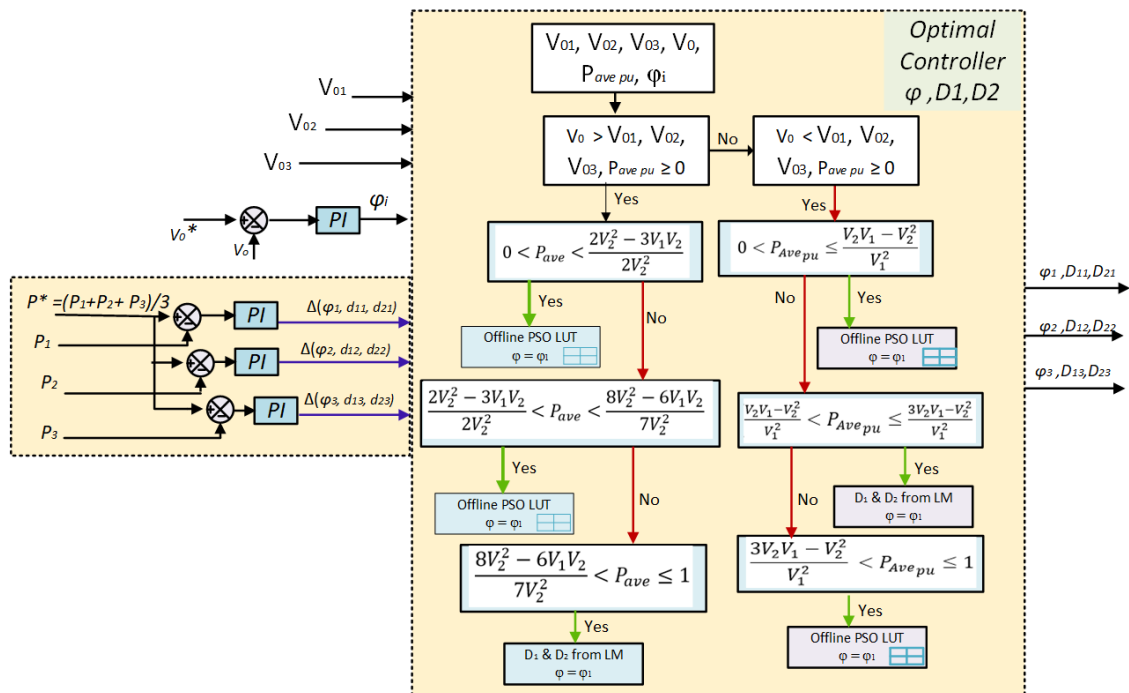


Fig. 5.33 Optimal closed loop control of the DAB

5.8 HFT Design and Optimization

A design optimization and methodology for HFT is presented in this section for high efficiency power electronic applications, such as SSTs. The presented method can help to interactively select the optimal transformer design based on various criteria, including the core shape, core ma-

materials, wire, and optimal design specifications. Advancement in high power and high switching semiconductor devices and development of various magnetic materials enable researchers to design high power density converters at a reduced size and volume, thus improving the cost and weight of the overall system. For achieving galvanic isolation between the input and the output [216] - [222] in HFT applications, two types of converter topologies are mainly used: resonant and DAB converter configurations.

The design procedure of HFTs is cumbersome and presents many challenges when compared to the design of traditional line frequency transformers. The line frequency transformer typically operates on low grid frequency (50Hz or 60Hz) and sinusoidal voltage and current, while HFTs operate under square or multilevel voltages and nonsinusoidal currents at a higher frequency in the range of KHz to MHz. These operation characteristics of HFTs have great effect on core losses and temperature rise [214]– [225] and on the insulation coordination and winding losses [226]– [235]. In MV and high power DC-DC applications, the most crucial component in the converter is the HFT, due to its capability to enable power transfer between each stage of the converter and provide both insulation and galvanic isolation. The most commonly used magnetic materials are the nanocrystalline and MnZn ferrite, owing to their capability to operate at high frequencies. Different transformer core shapes have been presented in the literature: UU shape in [236]- [238] and EE shape in [239]– [241].

5.8.1 Core Loss Determination

Depending on the converter topology and application, various methods can be used to estimate the core loss of the HFT. The original Steinmetz Equation is the most used technique for evaluating the core loss and designing the transformer [214] and [223], as stipulated in (5.107)

$$P_c = K f^\alpha B_m^\beta \quad (5.107)$$

For applications that require three level voltage at the transformer terminals, as seen in Fig. 5.34, the IGSE is formulated based on the characteristics of the flux waveform seen in Fig. 5.34 and presented in (5.110). To determine the core loss for $(1 - D)T$, (5.108) is used. For DT , (5.109) is used. K , α , and β are the Steinmetz coefficients.

$$\left| \frac{dB(t)}{dt} \right| = 0 \quad (5.108)$$

$$\left| \frac{dB(t)}{dt} \right| = \frac{2\Delta B}{DT} \quad (5.109)$$

$$P_{core} = \frac{1}{T_s} \int_0^{T_s} K_i \left| \frac{dB(t)}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt \quad (5.110)$$

$$K_i = \frac{2^{1-\beta} K_s \pi^{1-\alpha}}{\frac{1.7061}{\alpha+1.354} + 0.2761}$$

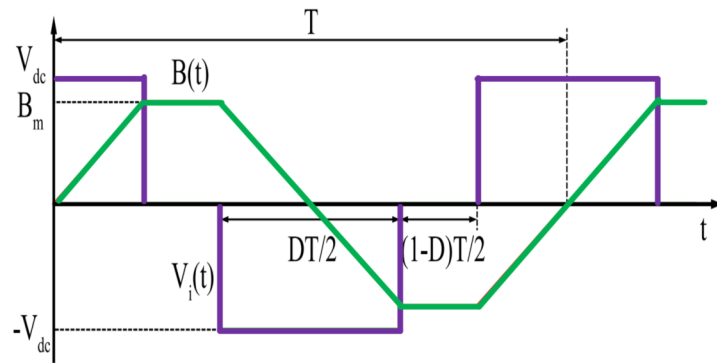


Fig. 5.34 Flux density waveform for a generic three-level voltage waveform

5.8.2 Winding Loss Determination

Litz wire is the prime winding wire in HFT due to its ability to operate at high frequency while reducing the conduction loss. Litz wires incorporate the number of strands, N_s , and the radius, r_l . When a time-varying current passes through the Litz wire, the current can potentially be

distributed unevenly due to the well-known skin and internal proximity effects. The skin effect pushes the current path to the surface in each strand, which is described by the skin depth δ , while the proximity effect is characterized by the interaction between each strand and the external magnetic field generated by the currents flowing through the rest of the strands. Both the proximity and the skin effects can increase the winding loss. The method presented in [228] is used to derive winding loss, with the assumption of $r_l \leq \delta$, to obtain the winding loss, as in (5.112).

$$\delta = \frac{1}{\sqrt{\pi \sigma f \mu}} \quad (5.111)$$

μ is the magnetic constant, σ is the conductivity of the conductor material, and f is the frequency.

$$P_{W_{loss}} = R_{eff} I_{rms}^2 \quad (5.112)$$

where

$$R_{eff} = \frac{MLT_w N}{\pi \sigma r_l^2 N_s} \left(1 + \frac{\pi^2 N_s \beta}{192} \left(16m^2 - 1 + \frac{24}{\pi^2} \right) \left(\frac{r_l}{\sigma} \right)^4 \right)$$

I_{rms} is the RMS current, m is number of layers, β is the fill factor, and MLT_w is the mean length turn of the winding.

5.8.3 Optimization Procedure

The HFT design calls for the selection of the right magnetic core shape and material and the optimal size of the winding conductor. In addition, different design criteria, such as volume, weight, temperature rise, and power loss, must be considered. In HFT applications, the leakage inductance calculation is crucial for ensuring proper operation of both resonant and non-resonant converters. The volume and weight are directly related to the leakage inductance of

the transformer. The winding structure is dependant on the type of conductor. After obtaining the optimal conductor area, the winding length and core shape can be chosen for the optimal transformer. In the optimization process, the system parameters are determined and a database containing different core shapes, magnetic materials, and conductor sizes and types is built. Based on the design requirements, the core shape is selected based on the required leakage inductance and materials are selected based on the operating frequency and power level. Once the number of turns, maximum flux density, current density, and window area are determined, the conductor type can be selected based on its diameter and frequency range. The optimization steps will search for the transformer with the lowest volume, total loss, and temperature. This step will repeat until the optimal design is obtained. Fig. 5.35 presents the design strategy.

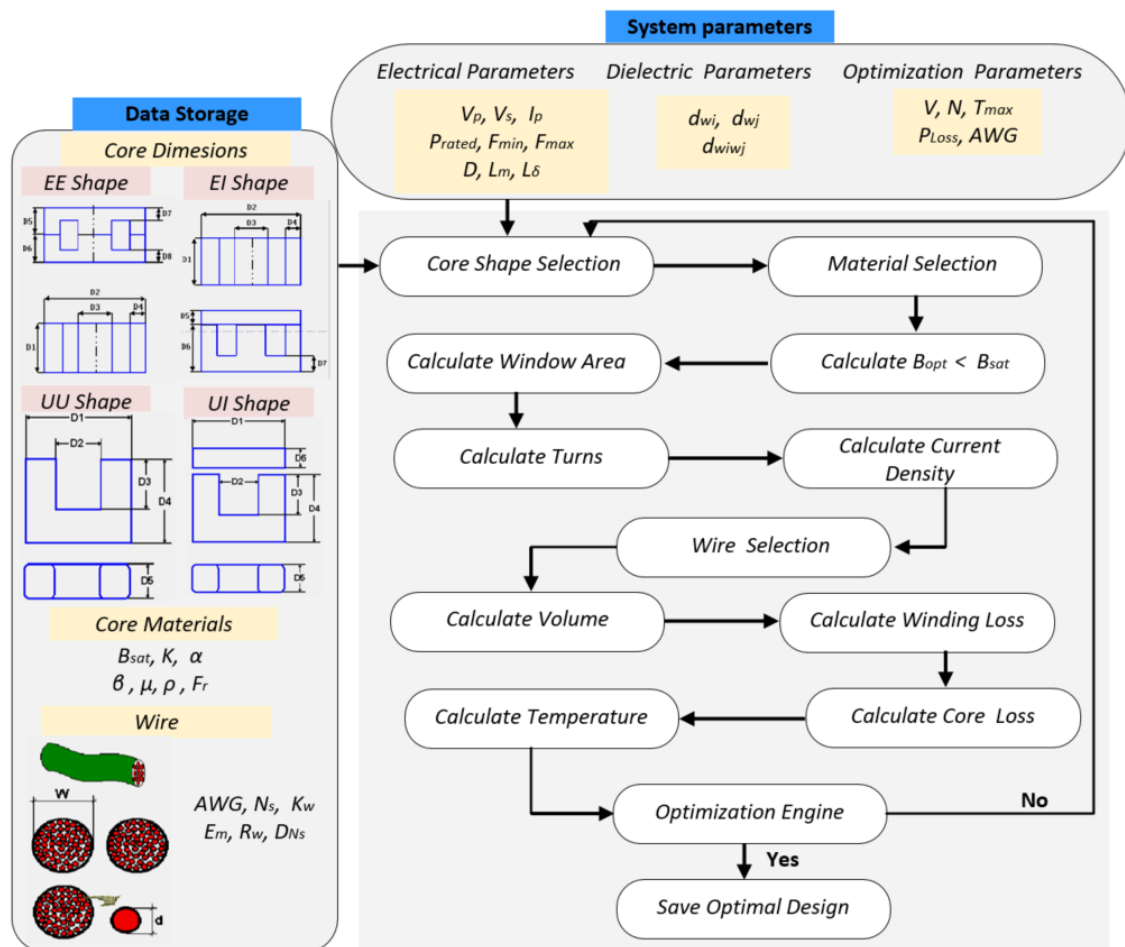


Fig. 5.35 HFT design optimization method

The following figures are the outputs of the optimization process. Fig. 5.36 shows all the transformer designs that have the lowest number of turns and Fig. 5.37 shows the footprint of the designs with the lowest number of turns. The next criteria of the optimal transformer are fulfilled based on the selected optimal conductors. Fig. 5.38 and Fig. 5.39 demonstrate the final choice for the transformer design with the lowest total power loss and lowest temperature rise. Based on the outputs of the optimization, design ID# 51 is the optimal design for this transformer.

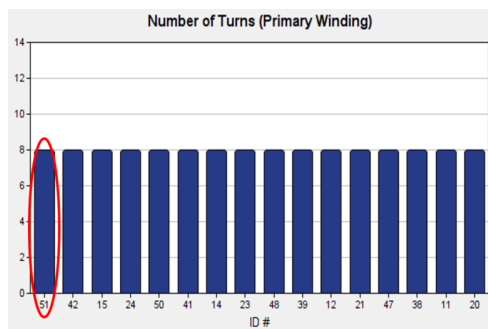


Fig. 5.36 HFT designs with the lowest number of turns

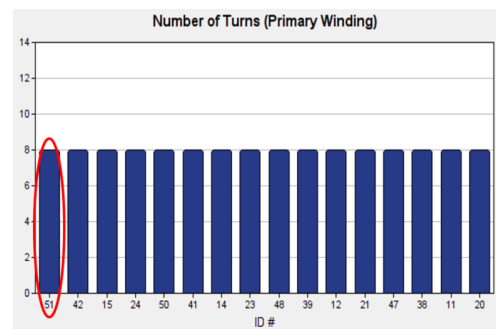


Fig. 5.37 HFT designs with the lowest volume

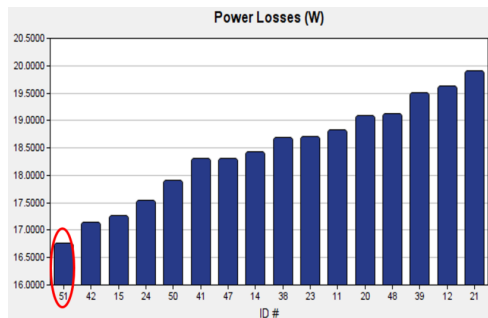


Fig. 5.38 HFT designs with the lowest power loss

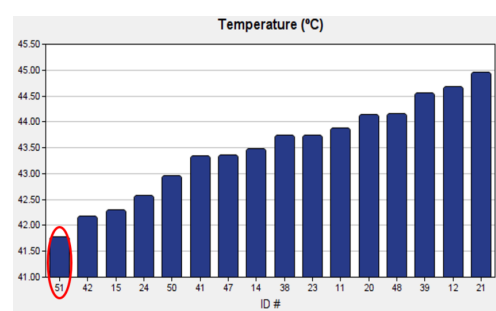


Fig. 5.39 HFT designs with the lowest temperature

Based on the obtained optimal HFT model, Ansys/Maxwell was used to perform the finite element analysis for this transformer. Fig. 5.40 and Fig. 5.41 show the UU simulated transformer model. The prototype for this transformer model is seen in Fig. 5.42. Fig. 5.43 shows the primary and secondary voltages and currents passing through the transformer in a DAB set test.

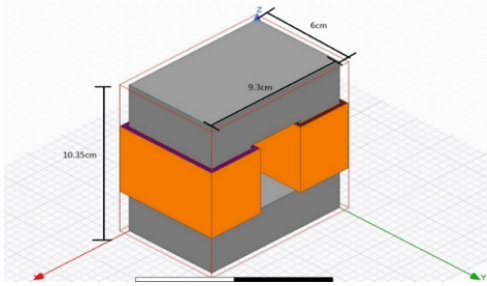


Fig. 5.40 HFT design FEA model

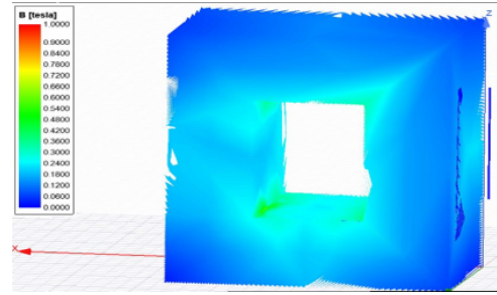


Fig. 5.41 HFT design FEA model simulation

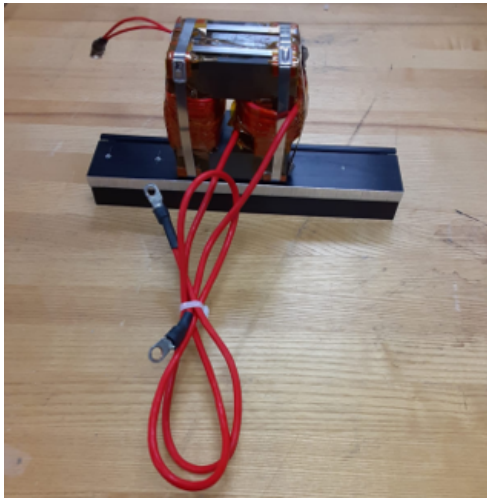


Fig. 5.42 HFT prototype

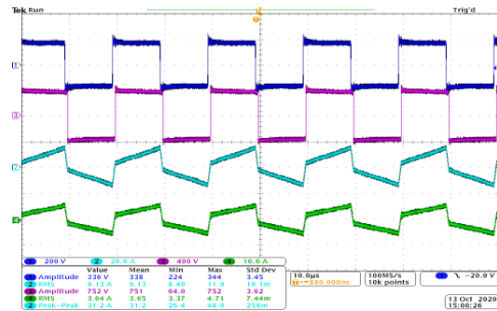


Fig. 5.43 HFT prototype experimental result

CHAPTER 6

Experimental and Simulation Results

6.1 A Model-Based Design Approach

For several decades, HIL testing has been used in the automotive and aerospace industries to overcome many engineering challenges. Power electronic engineers now face many challenges analogous to those that triggered HIL use in other industries as the demands of designing energy and electrical power systems grow. The benefits of HIL testing are particularly applicable to the demand of real-time requirements of power electronic applications. With the new generation of semiconductor devices, power converters are able to switch at higher frequencies. As a result, validating high-power converters is becoming more difficult and expensive. The high-fidelity, real-time simulation performed in HIL testing is highly beneficial to the development of high-performance power converters. The capability of HIL systems to handle a plant simulation of highly complex power converters helps decrease the need for considerable investment in high-power lab infrastructure. HIL technology is based on the foundations of model-based design (MBD) and is used to implement and validate embedded control systems using real-time simulation.

MBD is a mathematical-based visual approach for the development of advanced control systems. Use of the MBD technique has allowed highly complex control architectures to be prototyped, verified, tested, and validated in a manner that is faster and more cost effective

than traditional embedded design methodology. MBD integrates plant modeling, controller design, simulation of the plant and controller, and controller deployment in each step of the design process. Because MBD enables faster development of complex algorithms using already created building blocks for both time and discrete domain validation, the need for extensive software coding is eliminated. Fig. 6.1 depicts an MBD application development [242].

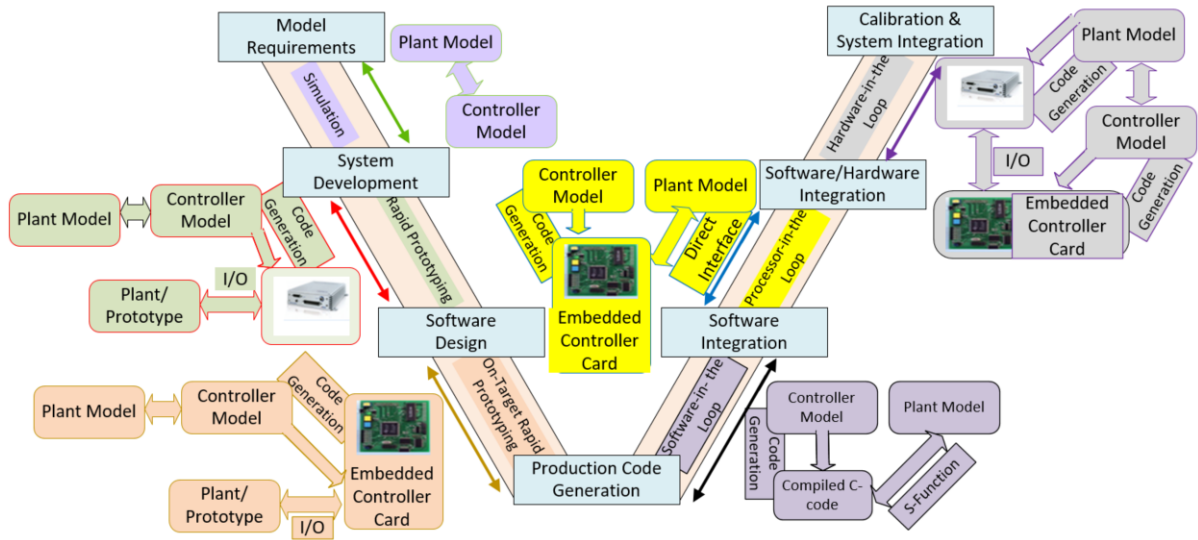


Fig. 6.1 The stages of MBD

The HIL system emulates the electrical sensor and actuators in order to interface between the plant model and embedded controller under test. The plant controls the values of the emulated sensors, which are read and processed by the embedded controller to generate control signals for the regulating the plant model.

Both simulation and real time validation utilizing HIL were used for this work. Results for these methods are presented to validate the steps in the development of the embedded controller for the fast charger.

6.2 Simulation Results

To validate the proposed control structure, simulations were carried out using the MATLAB/Simulink software. A single-phase, three module converter, as seen Fig. 6.2, was used to verify the presented algorithm. The dynamics of the fast charger for the worst case scenario are discussed and presented. The converter was tested for all three power regions, as discussed in Chapter 5. Table 6.1 contains the parameters of the system. Fig. 6.3 depicts the overall control block diagram of the system. The design of the proposed configuration utilizes 277V AC grid and generates 170V inner DC bus voltage per module to establish the DC-link for the ISOP DAB converter, which in turn generates 400V output.

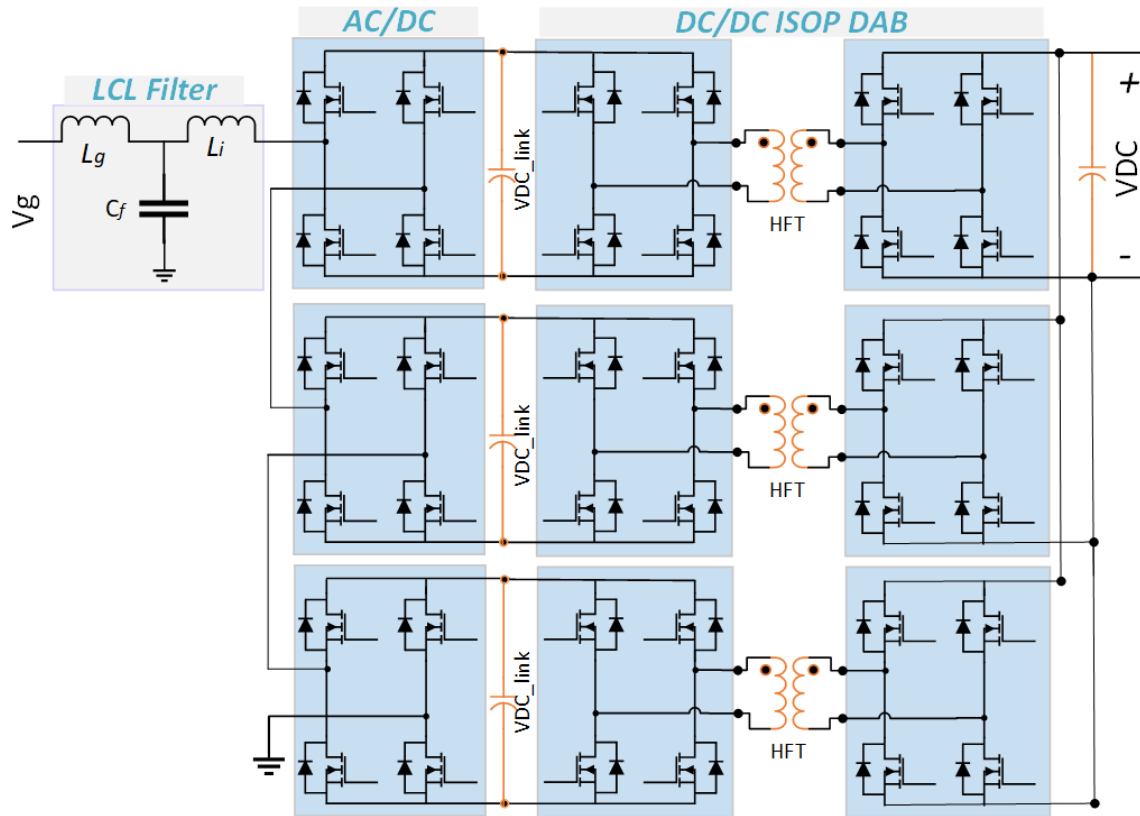


Fig. 6.2 The single-phase system

Table 6.1 System Parameters

| Symbols | Value | Symbol / Names | Value |
|------------|----------------|----------------------|--------------|
| V_g | $277 V_{RMS}$ | Grid frequency | 60 Hz |
| L_i | 0.8 mH | AFE frequency | 10 kHz |
| C_f | 10 μ F | DAB output voltage | 400 |
| L_g | 0.5 mH | DAB frequency | 50 kHz |
| r_i, r_g | 0.08, 0.05 ohm | Rated power per cell | 3 kW |
| V_{dc} | 167 V | Power modules | CCS050M12CM2 |

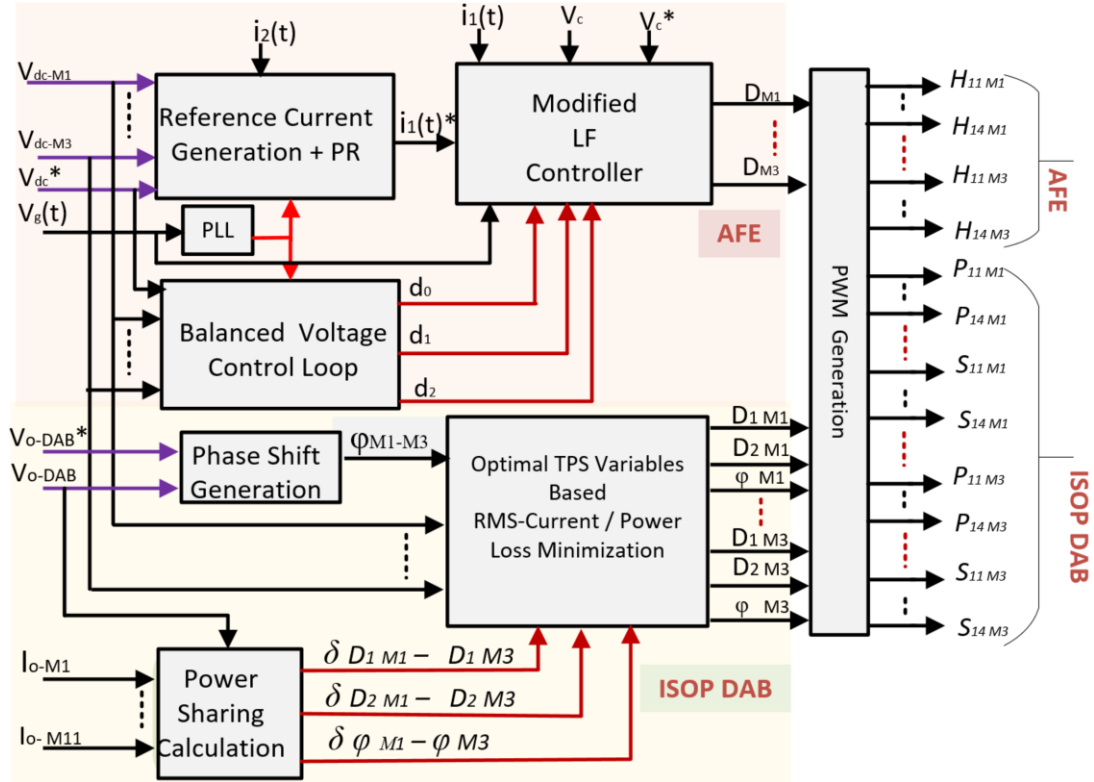


Fig. 6.3 Control structure of the fast charger

6.2.1 AFE Simulation Results

Fig. 6.4 shows the grid voltage, grid current, and the three DC bus voltages of the AFE, demonstrating its performance at steady-state. It can be noticed that all three DC bus voltages

are equal and the system exhibits low overshoot and DC bus voltage ripple (2 volts). The grid current is sinusoidal and in phase with grid voltage.

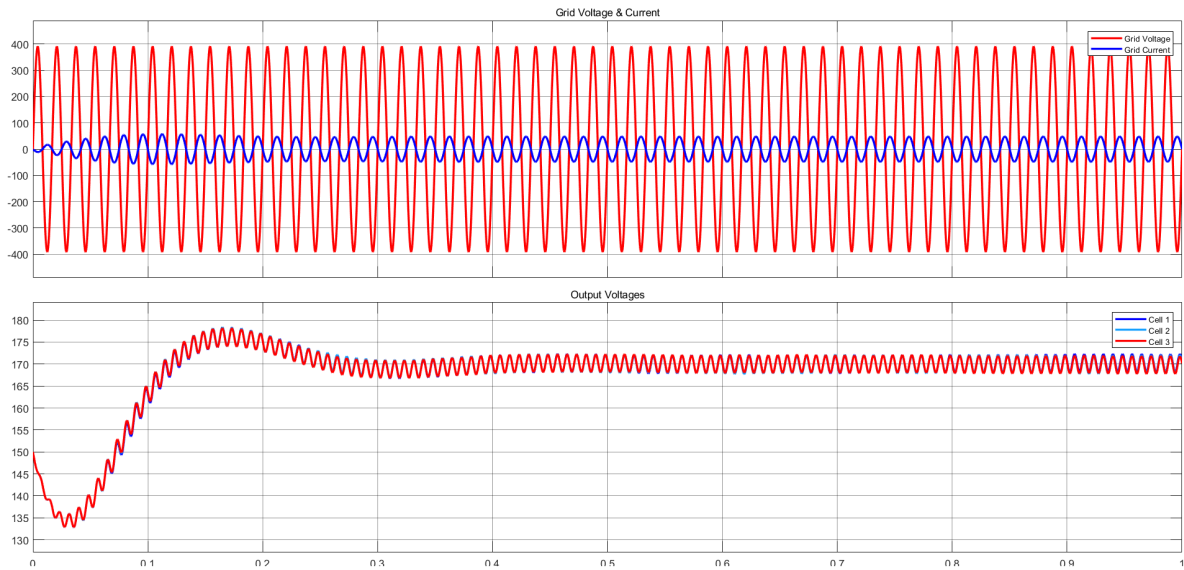


Fig. 6.4 Steady-state performance of the AFE

The tracking performance of the DC bus voltages and grid current can be seen for all three regions for both steady-state and transient operation, as in Fig. 6.5. In Zone 1, which is the low power region, the system was loaded at 23% (0s-0.7s). In Zone 2, the medium power region, a step load was applied to bring the converter total power to 50% (0.7s-1.4s). In Zone 3, a 50% load step-up was added to bring the system to full capacity (1.4s – 2s).

The goal of this test was to ensure that under the worst condition, the DC bus voltage is limited to 10% overshoot or undershoot and the grid current is maintained sinusoidal and in phase with the grid voltage. As seen in Fig. 6.5 and Fig. 6.6, during load steps, the control provides robust voltage and current tracking accuracy. Fig. 6.6 is an expanded view of Fig. 6.5 at 50% load step. To further prove the performance of the control strategy, the THD of the grid current is measured for the low, medium, and high power regions. At low power, the THD is low (3.05%). The results are shown in Fig. 6.7 - Fig. 6.9.

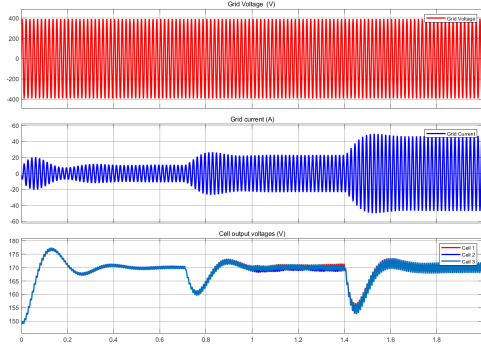


Fig. 6.5 Dynamic performance of the AFE

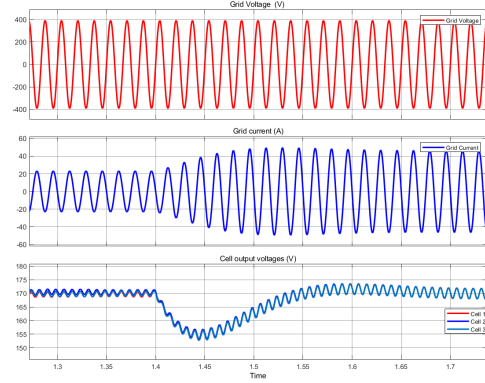


Fig. 6.6 Transient at 50% load step

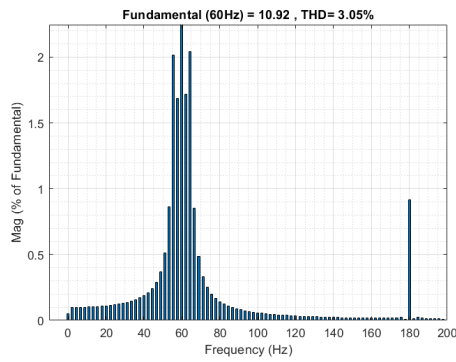


Fig. 6.7 THD at low power operation

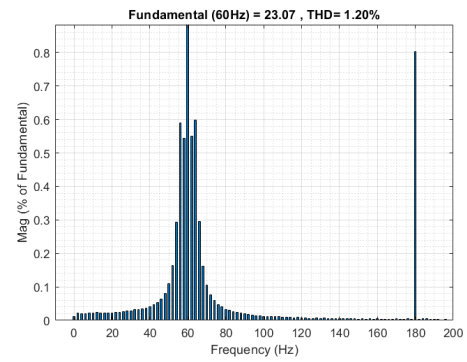


Fig. 6.8 THD at medium power operation

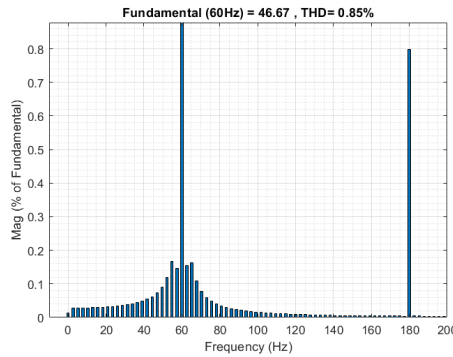


Fig. 6.9 THD at rated power operation

To further validate the dynamic performance of the AFE, unbalanced loading is applied at 0.7s. Originally, the converter was operating at steady-state under a balanced condition. A load step was applied to bring each cell of the converter to a different power level. During unbalanced operation, the converter maintained high DC voltage tracking accuracy with a 1.2 V difference between the DC bus voltages. The grid current was sinusoidal and in phase with the grid voltage. Fig. 6.10 and Fig. 6.11 demonstrate the dynamic performance of the AFE.

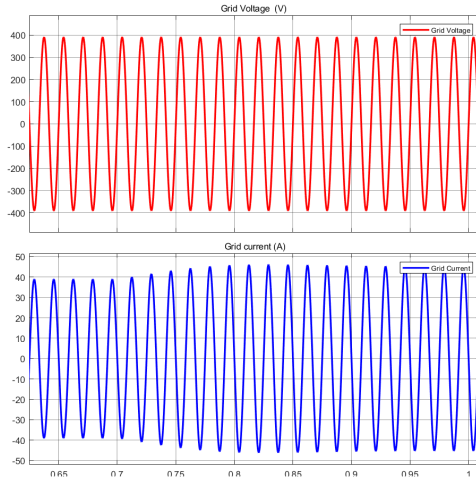


Fig. 6.10 Grid voltage and current of the AFE under unbalanced condition

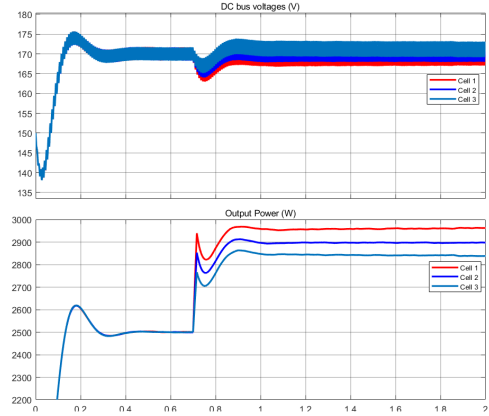


Fig. 6.11 DC voltages and powers of the AFE under unbalanced condition

6.2.2 DAB Simulation Results

The performance of the RMS current minimization, power sharing, and DC output voltage regulation are presented in this section. In order to study and validate the RMS current minimization, two control methods were applied and their performances were compared for the same power levels. Fig. 6.12 - Fig. 6.21 demonstrate the performance of the DAB for all three operating zones. Fig. 6.12 and Fig. 6.13 show the power regions for 23%, 50% and 100% power rated for both the traditional SPS and the TPS control methods, respectively. While both methods can effectively transfer the same power at steady-state, it can be noticed that during load steps, the TPS method provides lower overshoot and undershoot than the SPS method. It can also be noticed that the converter shares the same power level between each cell of the ISOP.

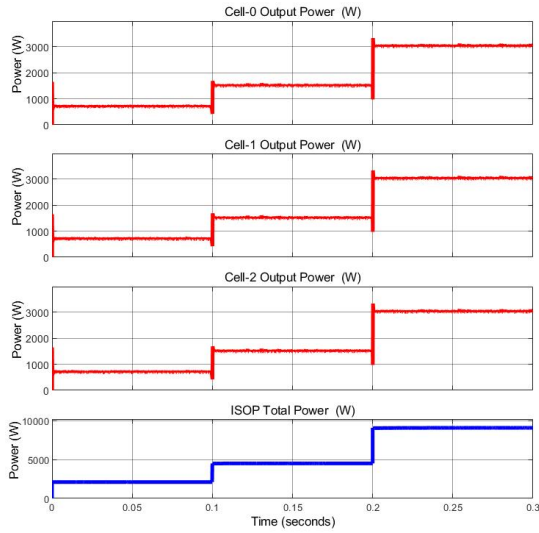


Fig. 6.12 Average and total power transfer of the ISOP under SPS method

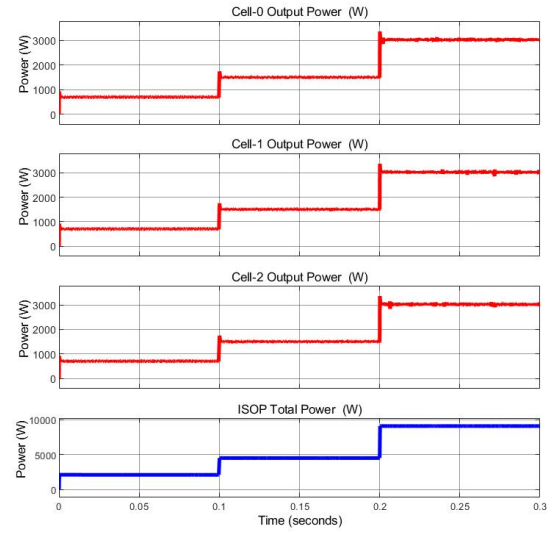


Fig. 6.13 Average and total power transfer of the ISOP under TPS method

The TPS method was compared to the SPS method to evaluate the RMS current minimization algorithm. In Fig. 6.14, the converter is operating under SPS method, while in Fig. 6.15 the TPS method was used to minimize the RMS current. Both control methods provide accurate output voltage tracking. However, it can be seen that for the same power level, the TPS provides better performance. The RMS current is decreased by 11.9A at the low power zone, 8.2A at the medium power zone, and 1.3A at the rated power zone. Therefore, from the comparison between the SPS and TPS methods, one can see that the applied RMS current minimization based TPS technique improves the converter performance while maintaining the same power transfer. Ultimately, the goal of the output voltage is to reflect any load step effects on the AFE side to maintain a stiff output DC voltage. As seen in Fig. 6.14 and Fig. 6.15, the over/undershoot of the output of the converter is approximately 1% during the load steps. This improves the voltage regulation.

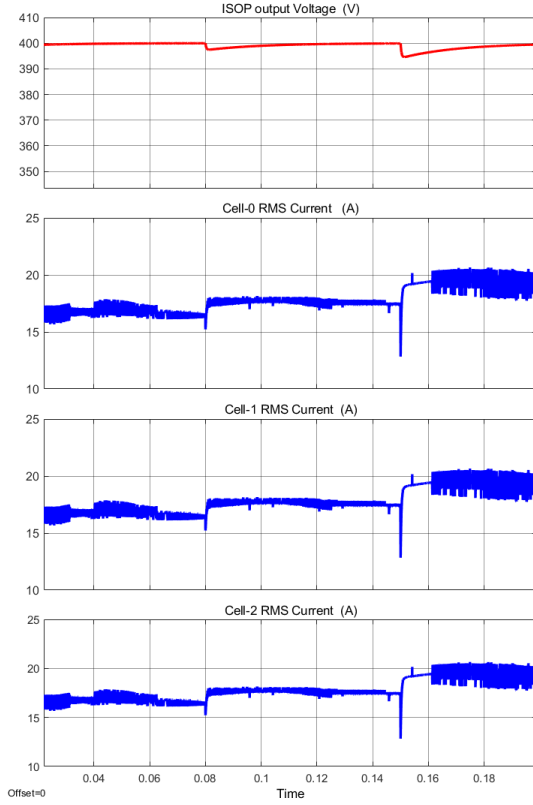


Fig. 6.14 Output voltage and RMS currents of the ISOP under SPS method

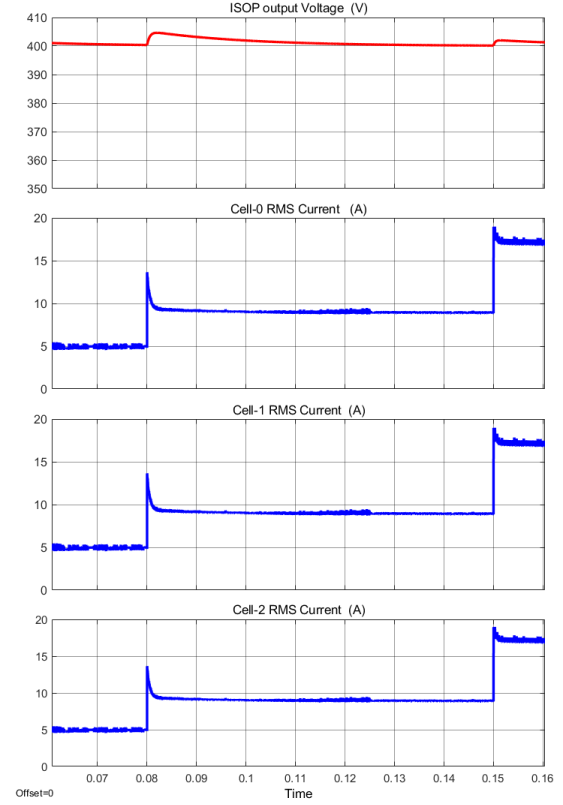


Fig. 6.15 Output voltage and RMS currents of the ISOP under TPS method

Fig. 6.16 - Fig. 6.21 show the primary voltages, V_{prim} , secondary voltages, V_{sec} , and leakage currents, I_l , of the HFT for each cell of the ISOP under both SPS and TPS control methods for all three regions. Table 6.2 presents a summary of the RMS current values for both the traditional SPS and the optimized TPS methods.

Table 6.2 Summary of the RMS current for both the SPS and TPS methods

| Control Methods | Low Power | Medium Power | Rated Power |
|-----------------|-----------|--------------|-------------|
| SPS (A) | 16.9 | 17.9 | 19.2 |
| TPS (A) | 5.0 A | 9.7 A | 17.9 A |

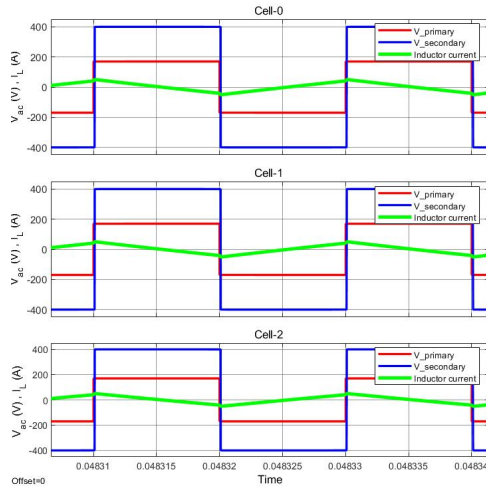


Fig. 6.16 V_{prim} , V_{sec} and I_l of the ISOP under SPS method for Zone 1

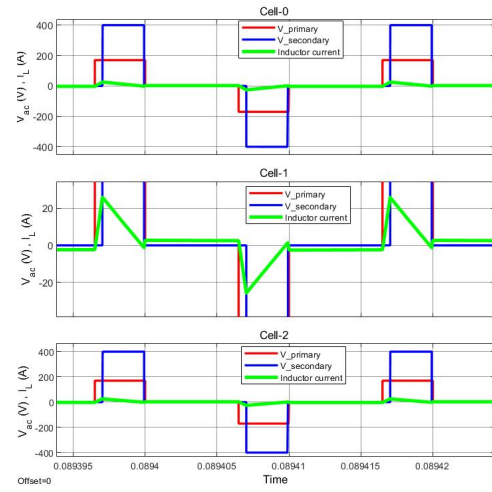


Fig. 6.17 V_{prim} , V_{sec} and I_l of the ISOP under TPS method for Zone 1

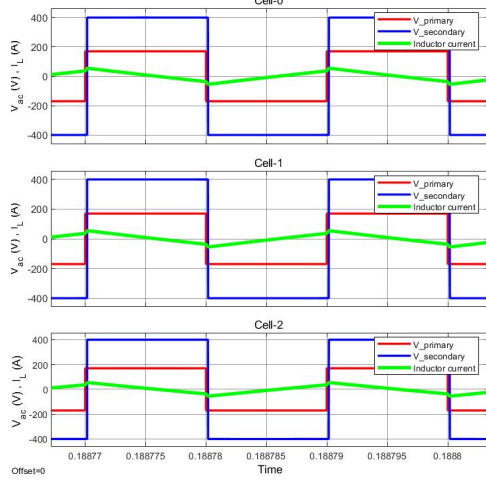


Fig. 6.18 V_{prim} , V_{sec} and I_l of the ISOP under SPS method for Zone 2

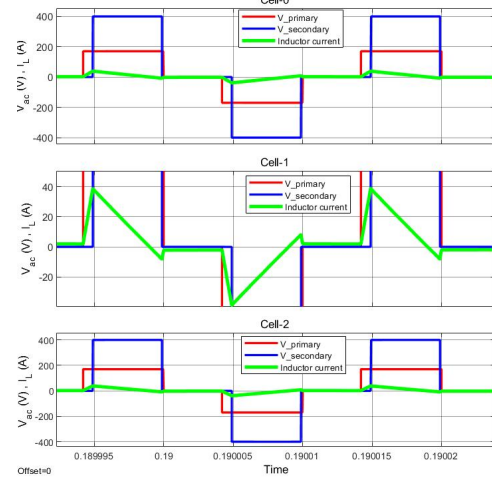


Fig. 6.19 V_{prim} , V_{sec} and I_l of the ISOP under TPS method for Zone 2

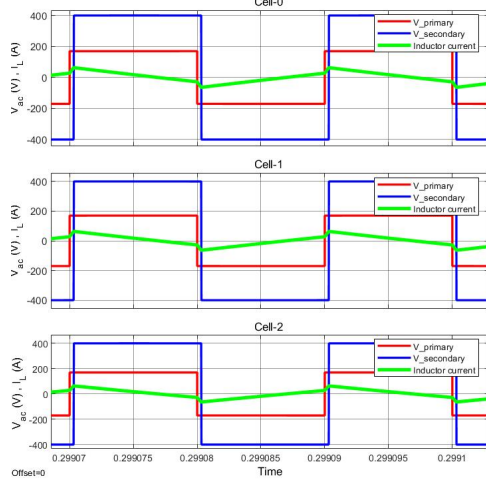


Fig. 6.20 V_{prim} , V_{sec} and I_l of the ISOP under SPS method for Zone 3

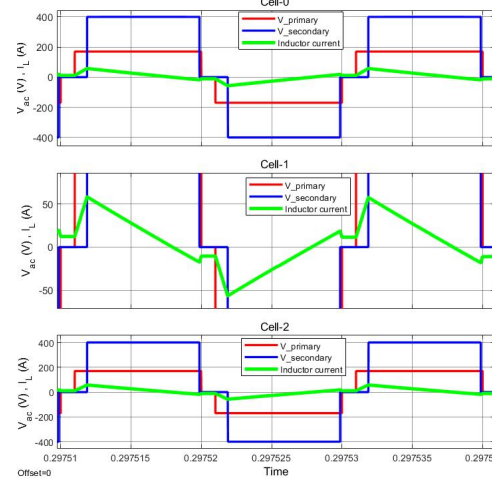


Fig. 6.21 V_{prim} , V_{sec} and I_l of the ISOP under TPS method for Zone 3

6.3 System Loss Analysis

In order to have an accurate representation of the conduction and switching losses of the power modules, the Matlab/Simulink environment was used to model the heatsink and to implement a look-up table based on the manufacturer's datasheet of the power module. A half-bridge MOSFET module of the system is shown in Fig. 6.22, which includes its loss calculation based on the measured voltage and current across each MOSFET. Fig. 6.23 shows the steps in calculating both the switching and conduction losses. To obtain the switching losses at both turn-on and turn-off, the voltage across the module, the current flowing into the module, and the junction temperature are used to calculate the energy on and off losses. For the conduction loss, the current of the module and its junction temperature are used to calculate the saturation voltage across the MOSFET.

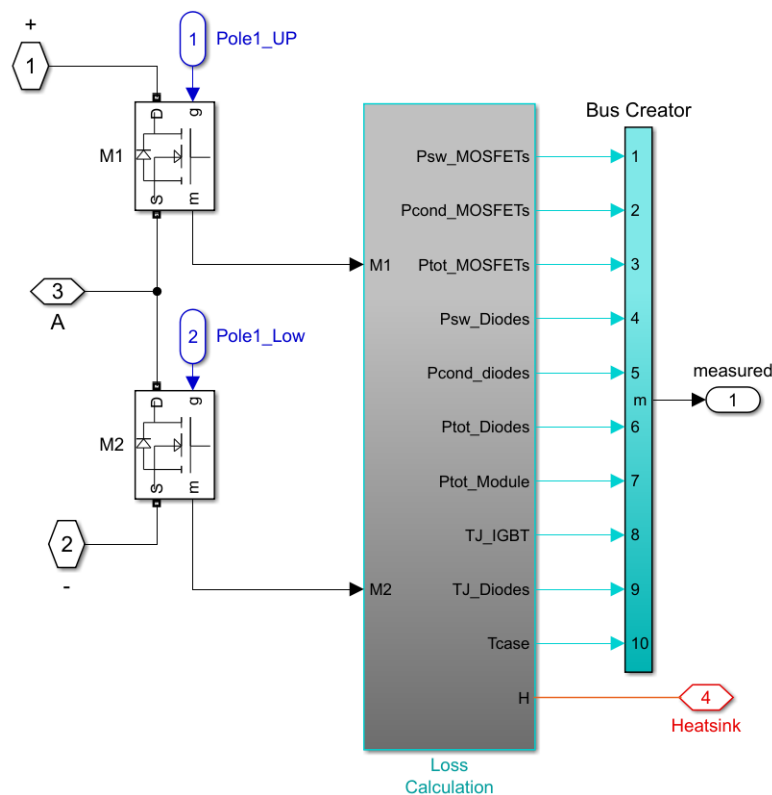


Fig. 6.22 Half-bridge module loss calculation model

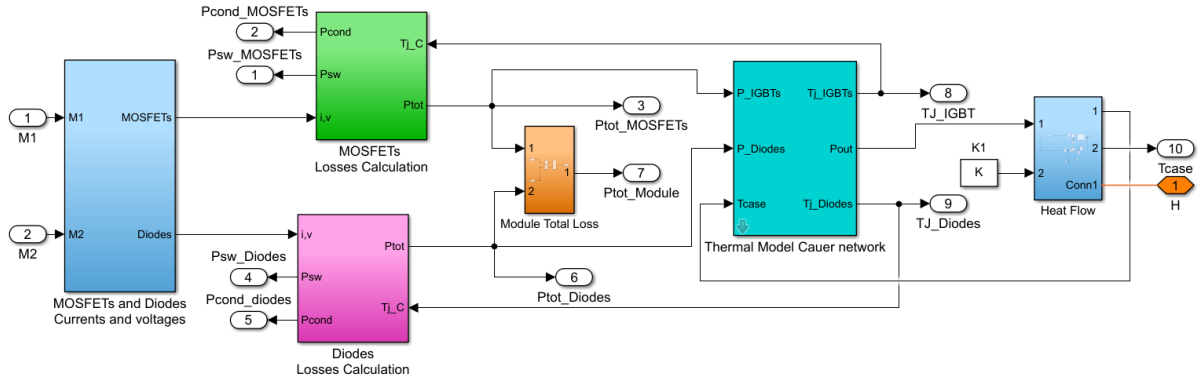


Fig. 6.23 Simulink loss calculation model

Fig. 6.24 and Fig. 6.25 show the performance of a single DAB converter in the ISOP system. The TPS control can be seen in the shape of the primary and secondary voltages of the HFT in Fig. 6.24 for the highest power region. Fig. 6.25 shows the voltages and leakage current under SPS control method. These figures demonstrate the tracking accuracy of the DAB converter output voltage.

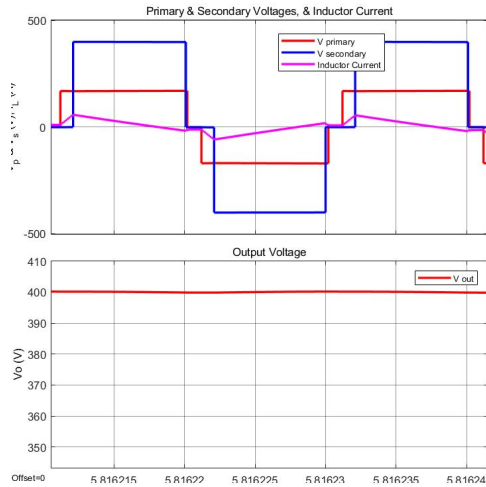


Fig. 6.24 V_{prim} , V_{sec} and I_l of the ISOP under TPS method for Zone 3

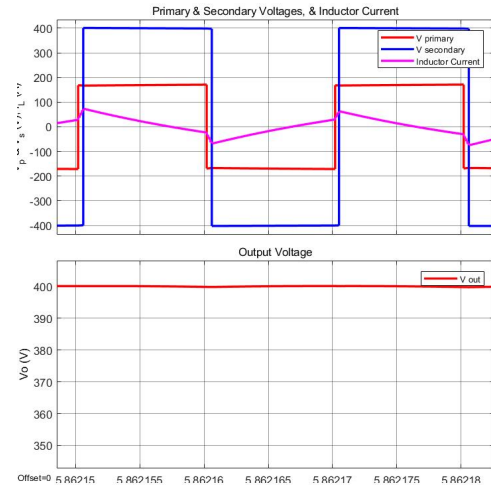


Fig. 6.25 V_{prim} , V_{sec} and I_l of the ISOP under SPS method for Zone 3

In order to validate the efficiency technique for the DAB converter, as derived in Chapter 5, the traditional SPS method is compared to the TPS method. Fig. 6.26 and Fig. 6.27 show these two cases. In Fig. 6.26, the TPS method is used; Fig. 6.27 shows the performance of the DAB under the SPS method. For the same power level and voltage rating, it can be concluded that

the applied control strategy provides higher efficiency, as expected, from the analytical results from Fig. 5.22, Fig. 5.26 and Fig. 5.30.

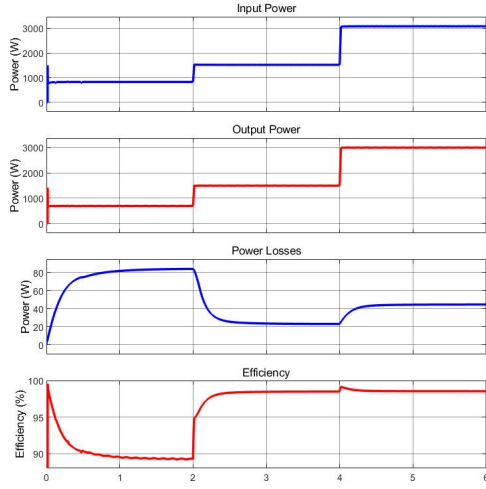


Fig. 6.26 Average power transfer for one cell and overall losses and efficiency of the ISOP under TPS method

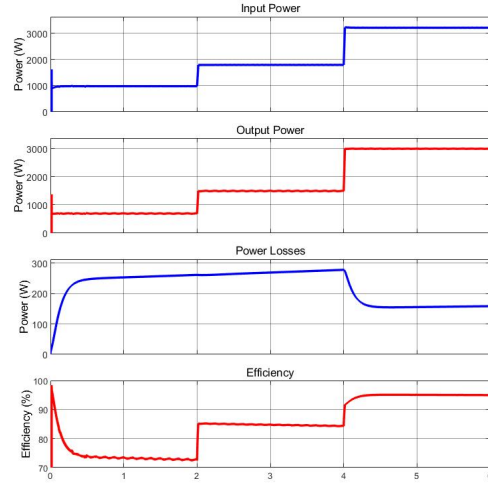


Fig. 6.27 Average power transfer for one cell and overall losses and efficiency of the ISOP under SPS method

The overall loss for the system is formulated as in (6.1), based on the conduction and switching losses of the AC-DC stage, the LCL filter losses, and the switching, conduction, core, and winding losses of the DC-DC stage. Fig. 6.28 and Fig. 6.29 show the overall loss breakdown and the efficiency of the system. The traditional SPS method was compared to the optimal TPS method. These figures clearly demonstrate the efficiency improvement of the converter under optimal TPS variables for all the power regions. The efficiency of the system was improved 15.74% in low power operation, 12.7% in medium power operation, and 3.67% at rated power operation.

$$P_{loss-total} = P_{loss-total-AFE} + P_{loss-total-LCL} + P_{loss-total-DAB} \quad (6.1)$$

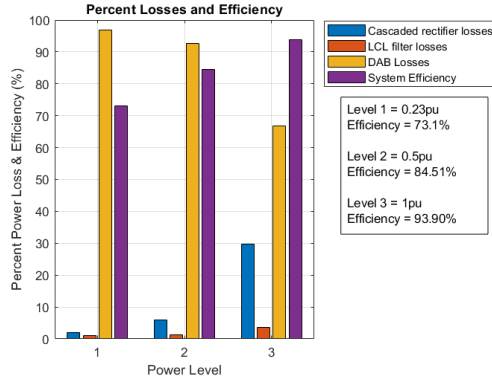


Fig. 6.28 Loss breakdown and efficiency of the system under SPS method

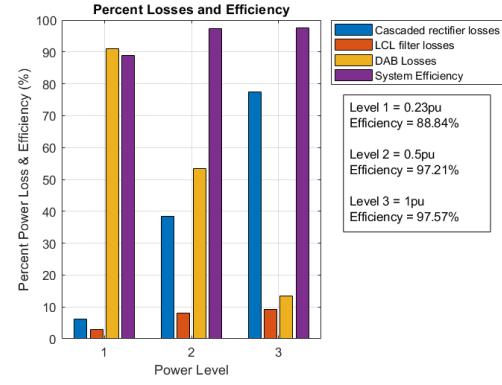


Fig. 6.29 Loss breakdown and efficiency of the system under TPS method

6.4 HIL Setup for the AFE

In order to validate the proposed controller for the AFE, the Typhoon HIL 604 device was used to model the power stage, as seen in Fig. 6.30. The grid, the passive components, and the power MOSFET were modeled using the Typhoon library. HIL is a closed-loop, model-based computerized testing solution. In this HIL testing, the controller under test (the derived modified LF) was designed using the Matlab/Simulink autocode generation capability. The generated code was downloaded to the TMDSCNCD28388D control card, which was connected to the Typhoon HIL DSP 180 Interface, as seen in Fig. 6.31. The Typhoon HIL interface board was directly connected to a real-time 604 simulator. This configuration facilitated HIL testing to establish how the actual controller would perform with the physical system at higher precision than would be possible in a fully simulated lab environment.

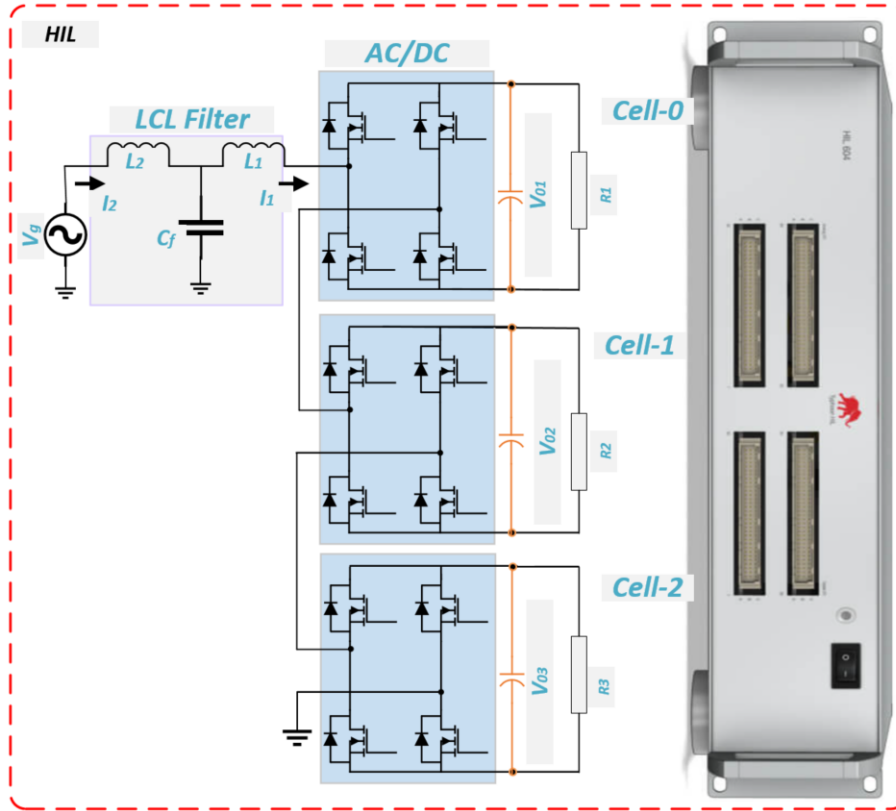


Fig. 6.30 HIL set-up

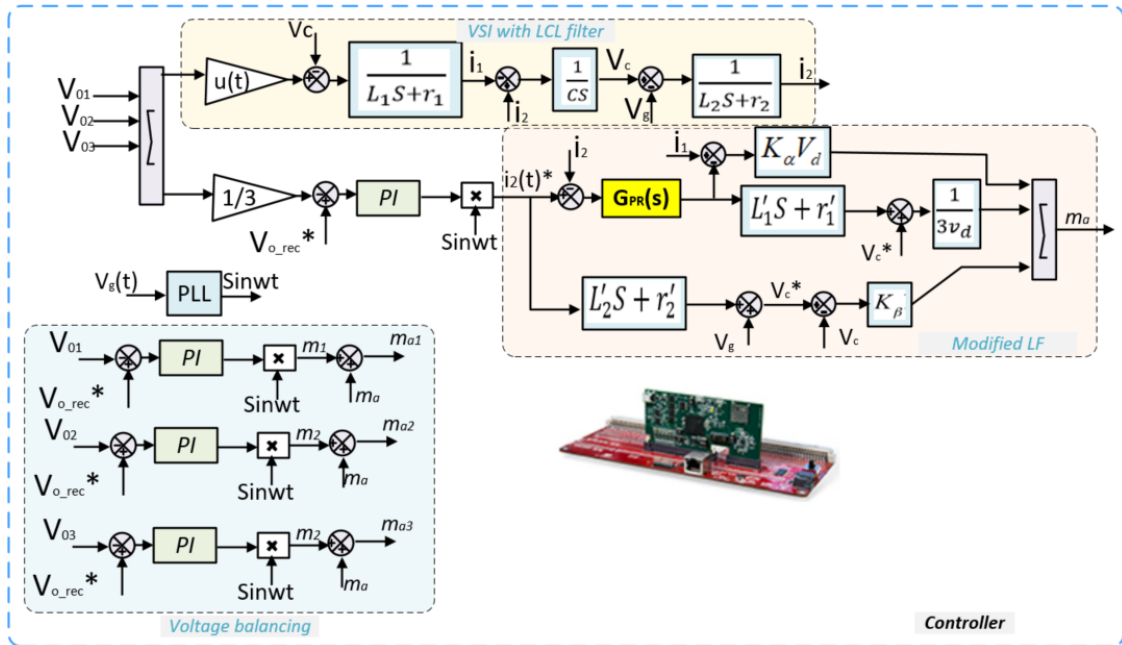


Fig. 6.31 Controller set-up

Fig. 6.32 - Fig. 6.45 demonstrate the results of the HIL experimental study of the AFE converter. These figures can be separated into three categories. Fig. 6.32 - Fig.6.36 present the

results for the converter operating under balanced conditions, while Fig. 6.37 - Fig. 6.39 show the results for the converter operating under both balanced and unbalanced conditions for two scenarios. Fig. 6.40 - Fig. 6.48 show the effect of the gain selection for K_β and K_α on the performance of the converter.

Fig. 6.32 shows the grid current and voltage, and two of the three DC bus voltages of the experimental results when the converter is operating at steady-state. Fig. 6.33 - Fig. 6.36 illustrate the dynamic performance of the converter. The three DC bus voltages and the grid current are shown for the three operating regions of the converter. Initially, in Fig. 6.33, the converter is operating under low power condition. A step load is applied to bring the converter to medium power operation. At the last stage, another step is applied to bring the converter to full power operation. The step load dynamic is used to test the transient response of both the voltage and current control strategies and the voltage balancing controller. During transition, it can be seen that the grid current presents smooth transient with no overshoot, and the undershoot observed in the DC bus voltages are within the less than 10% over/undershoot design specification.

Fig. 6.34 - Fig. 6.36 show the performance of the converter under the worst case scenario, a heavy load step-down and step-up condition. During this step-up and step-down, the robust grid current control method and the output voltage regulation technique proved to be effective in maintaining the proper operation of the converter. As demonstrated in these figures, the CHBML-AFE with the proposed control strategy generates balanced cell voltages and draws sinusoidal current from the grid. The harmonics content of the current signal is low and the THD value is measured as 2.7%.

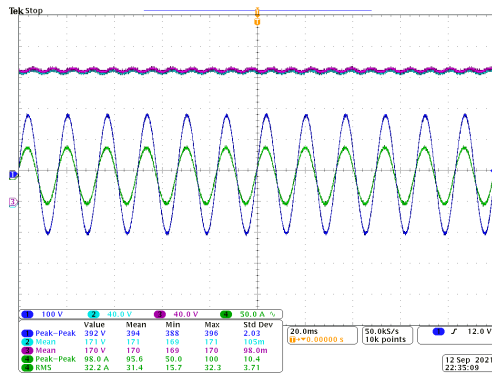


Fig. 6.32 Grid voltage and current, and the DC bus voltages

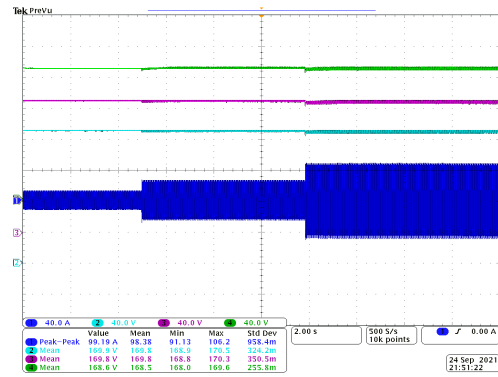


Fig. 6.33 Grid current and DC voltages during load steps

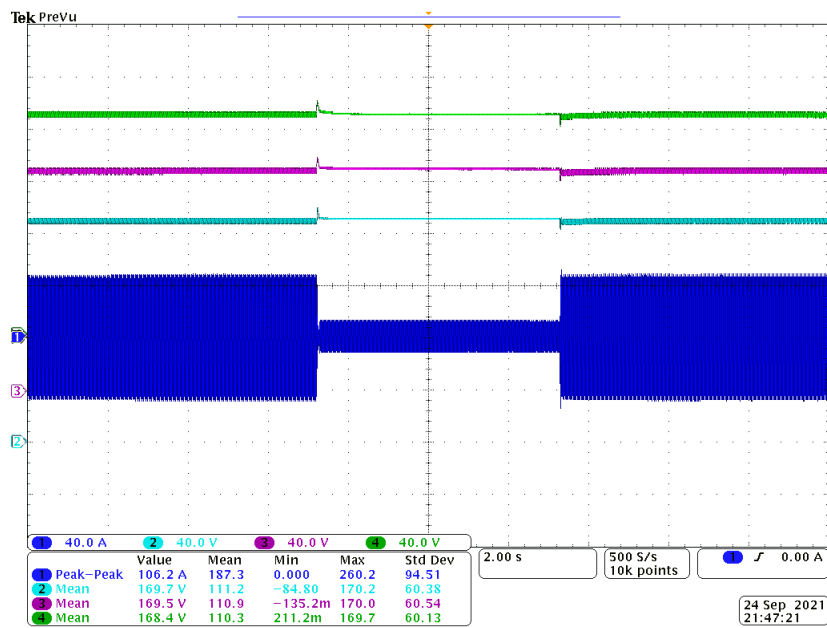


Fig. 6.34 Worst case of load steps of 3 DC bus voltages and the grid current

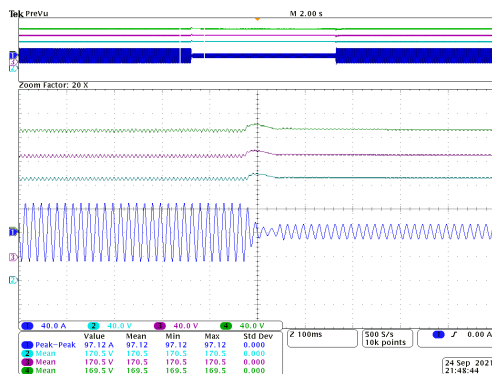


Fig. 6.35 Exploded view of the worst case of load steps from high to low power

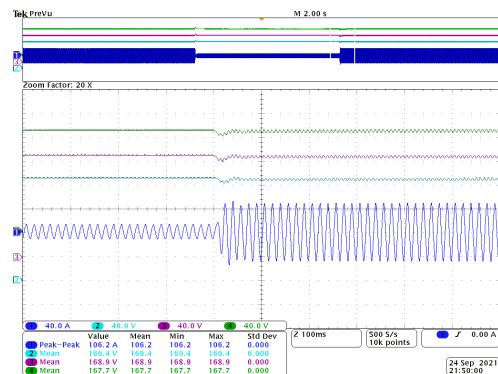


Fig. 6.36 Exploded view of the worst case of load steps from low to high power

Fig. 6.37 and Fig. 6.38 show the three output DC currents and the grid current for both the

balanced and unbalanced operation of the converter. Fig. 6.37 shows a light load unbalance, while Fig. 6.38 shows a heavy load unbalance. Fig. 6.39 shows the three DC output voltages and grid current for an unbalanced condition. In this scenario, the system was initially operating under a balanced condition. A load step-up was applied to bring the converter to unbalanced operation, which can be seen in the different levels of the DC output currents. During the unbalanced stage, each cell of the converter was operating under a different power level. A step-down was then applied to bring the converter back to normal operation. This test was designed to specifically check the DC voltage control. It is seen that the output voltages maintained stable and balanced operation during the transitions. In both scenarios, the converter maintained good transient and steady-state performance with minimal disturbance. Based on these results, it can be concluded that the proposed control strategy, utilizing the voltage balancing control and the LF based current control supported with additional capacitor feedback loop and PR controller, provides excellent steady-state and transient response with very limited overshoot and undershoot. Additionally, all the output voltages are well balanced, even during unbalanced loading.

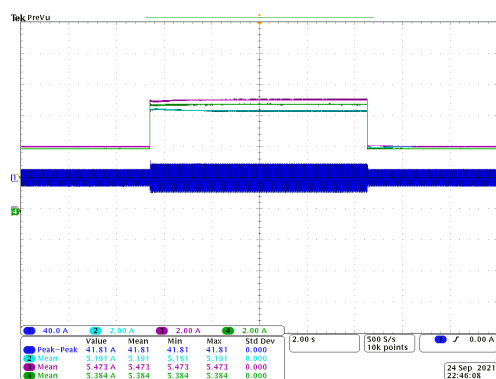


Fig. 6.37 Output DC currents and grid current during both balanced and unbalanced operation at light load

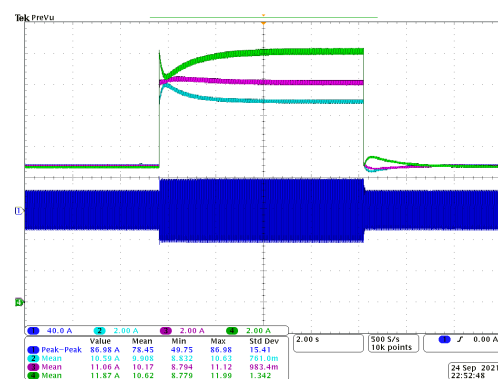


Fig. 6.38 Output DC currents and grid current during both balanced and unbalanced operation at heavy load

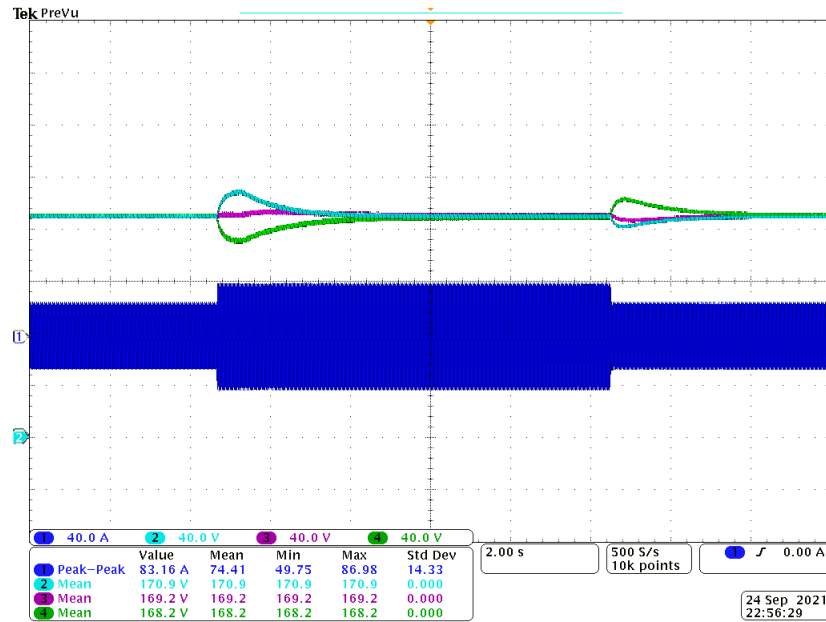


Fig. 6.39 Output DC voltages and grid current during both balanced and unbalanced operation

The performance of the converter without the added capacitor voltage feedback loop was investigated. When $K_{\beta} = 0$, a load step-down and step-up, similar to Fig. 6.34, was applied to compare the effect of the added capacitor voltage loop on the converter. The difference between Fig. 6.34 and Fig. 6.40 clearly demonstrates how the added capacitor voltage loop improves the dynamic response of the converter. As presented in the control analysis in Chapter 5, removing the additional capacitor voltage feedback loop introduces higher overshoot and undershoot, more oscillation, and increased settling time. Fig. 6.41 and Fig. 6.42 show a zoomed version during load step-down and step-up, respectively.

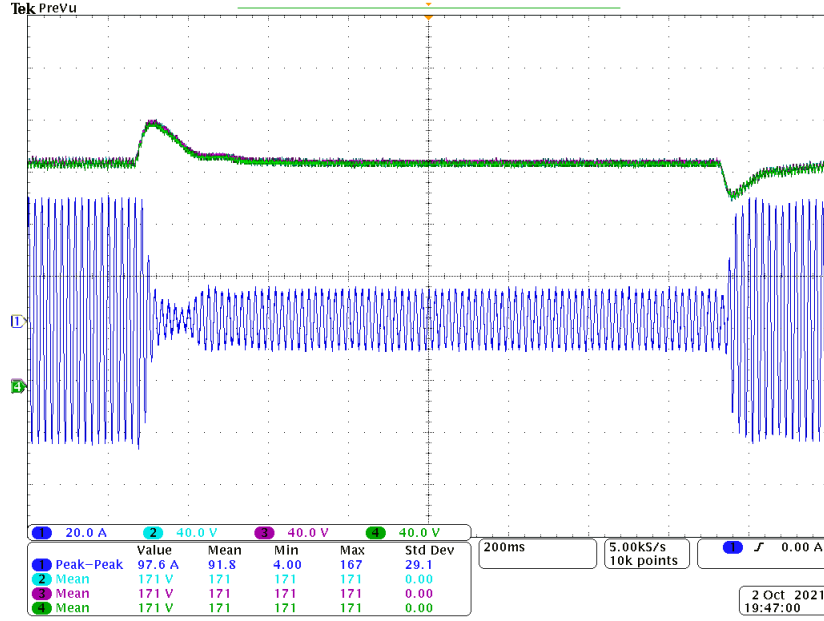


Fig. 6.40 DC bus voltages and grid current when $K_\beta = 0$

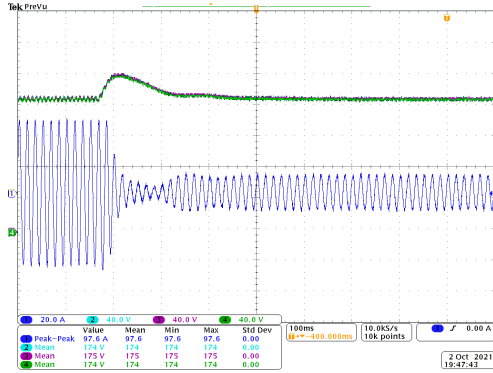


Fig. 6.41 Zoomed DC bus voltages and grid current when $K_\beta = 0$ during transient from high to low power

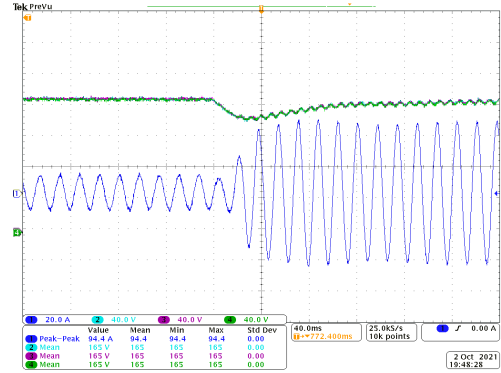


Fig. 6.42 Zoomed DC bus voltages and grid current when $K_\beta = 0$ during transient from low to high power

The effect of varying the K_β and K_α parameters to determine optimal range of operation for these parameters was also investigated. As presented in the root locus analysis in Chapter 5, K_α gains significantly affect the real part of the conjugate poles, but have comparatively less effect on the imaginary parts. Therefore, K_α improves the system dynamics by reducing the overshoot and undershoot during load steps, but can provide limited resonance damping effect to suppress the oscillations introduced by the complex conjugate poles of the LCL filter. When K_α is increased to a larger number, the oscillation becomes worse and can potentially cause the

system to go to unstable operation. Fig. 6.43 - Fig. 6.45 demonstrate the effect of increasing the value of K_α up to its upper limit before the system becomes unstable.

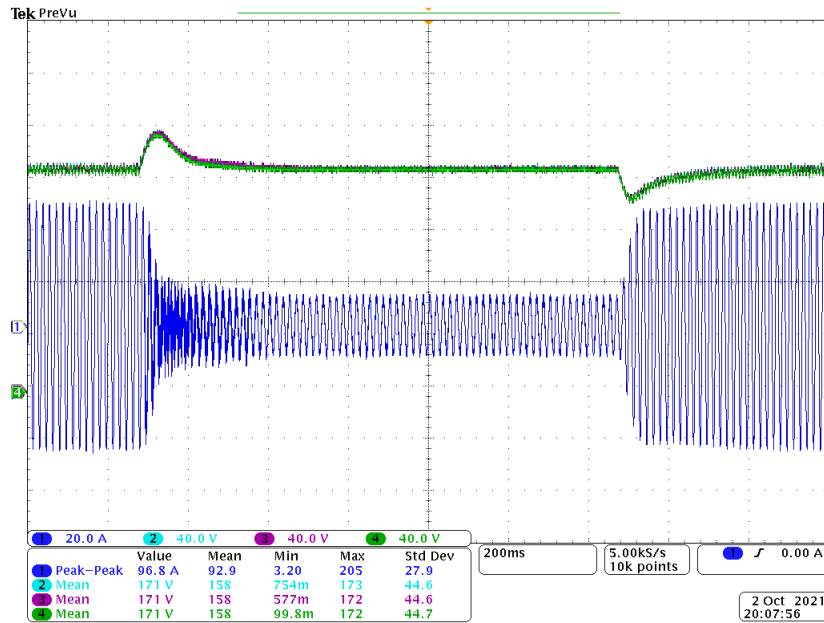


Fig. 6.43 DC bus voltages and grid current for a large $K_\alpha = 300$

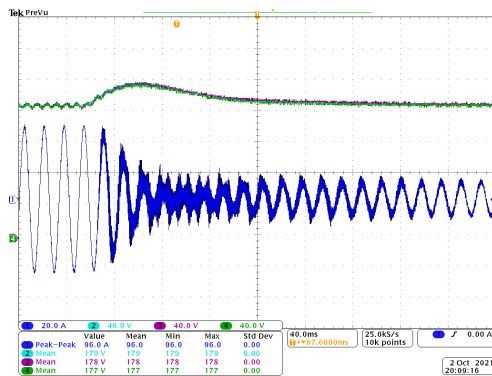


Fig. 6.44 Zoomed DC bus voltages and grid current for a large $K_\alpha = 300$ for step-down

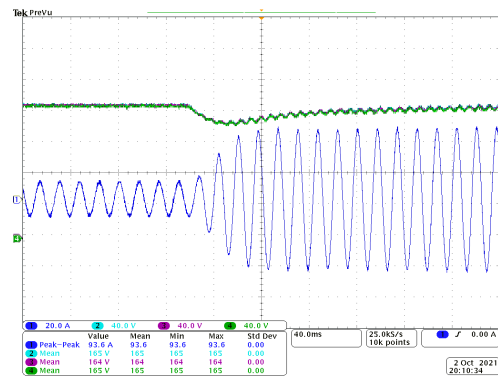


Fig. 6.45 Zoomed DC bus voltages and grid current for a large $K_\alpha = 300$ for step-up

When K_β is chosen within the range determined in Chapter 5 from the root locus plot, the damping ratio increases while the real pole moves toward the imaginary axis. However, the damping ratio is decreased with larger K_β values, as the real pole moves toward zero. This leads to deterioration in the dynamic response, higher overshoot and undershoot, and an increased risk for instability of the system. However, it should be noticed that even for large values of K_β ,

the oscillation is considerably decreased compared to the large value of K_α . This demonstrates the significance of the added capacitor voltage loop for providing better damping and reducing the oscillation. Fig. 6.46 - Fig. 6.48 demonstrate the effect of increasing the value of K_β up to its upper limit before the system becomes unstable. Therefore, optimum determination of the controller gains greatly affects the performance of the controller. Since the closed-loop transfer function is extremely complex, simulation and experimental studies are used to determine the optimal range for K_β and K_α in order to obtain a fast dynamic response and globally stable system.

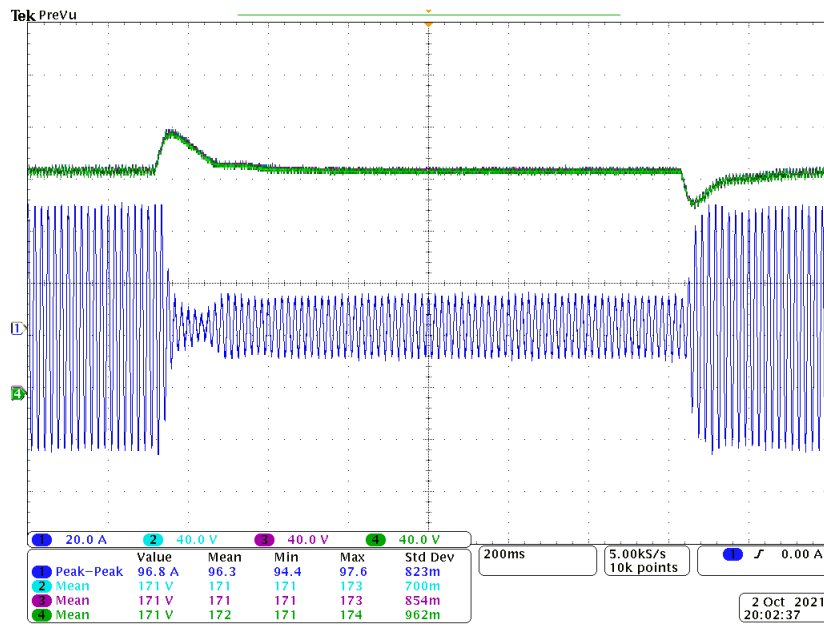


Fig. 6.46 DC bus voltages and grid current for a large $K_\beta = 30$

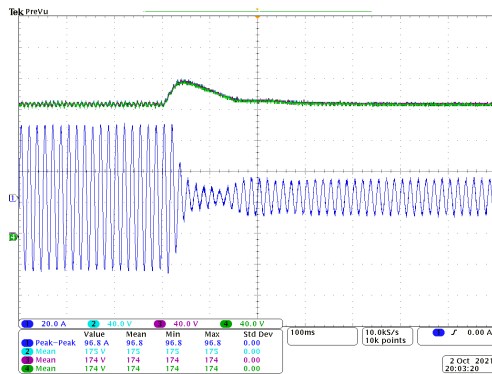


Fig. 6.47 Zoomed DC bus voltages and grid current for a large $K_\beta = 30$ for step-down

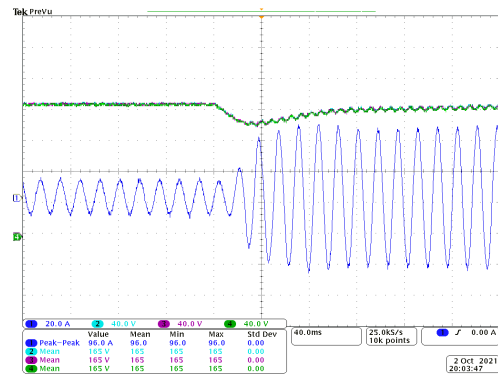


Fig. 6.48 Zoomed DC bus voltages and grid current for a large $K_\beta = 30$ for step-up

6.5 DAB Experimental Results

Utilizing the Typhoon HIL 604 device and the TMDSCNCD28388D control card, as seen in Fig. 6.49 and Fig. 6.50, the performance of the DAB was tested for three cases; low power, medium power, and rated power. To validate the efficiency improvement of the DAB converter, the RMS current minimization scheme was compared to the power loss minimization method. The derived method was compared to the traditional SPS and the optimized DPS methods. Fig. 6.51, Fig. 6.53, and Fig. 6.55 show the performance of a single DAB using the SPS method, Fig. 6.52, Fig. 6.54, and Fig. 6.56 present the experimental results for the DAB converter for the optimized DPS control technique, and Fig. 6.57 - Fig. 6.59 present the results for the optimized TPS algorithm.

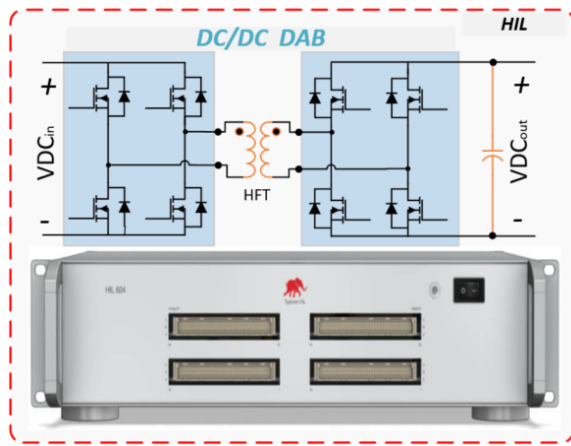


Fig. 6.49 DAB HIL set up

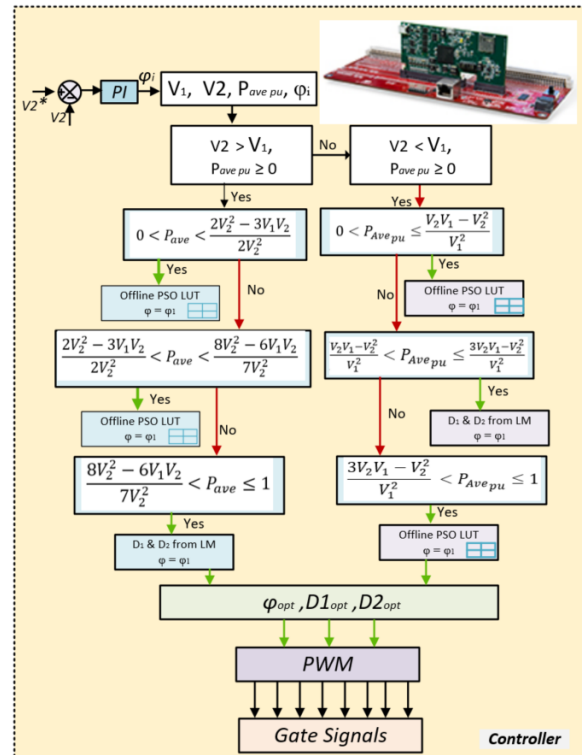


Fig. 6.50 DAB controller set up

6.5.1 Performance of the DAB with RMS Current Minimization

Fig. 6.51 - Fig. 6.56 show the three operation zones for the DAB converter. (Ch1 blue) is the output DC current, (Ch2 turquoise) is the transformer primary voltage, (Ch3 magenta) is the transformer secondary voltage, and (Ch4 green) is the transformer inductor current. The power levels can be identified based on the output DC currents of each of the presented results. The issue of high circulating and peak currents can be seen in the figures demonstrating the SPS method. At rated power, the peak current reached as high as 68.0A and the RMS current was 18.2A. However, these issues are even worse when the converter is operating at reduced power. For half of the rated power, the peak current only decreases by 4.0A and the RMS current by 0.9A. At the low power zone, the effect of the high peak and circulating current is even more severe. From rated power to 25% rated power, the peak current only decreases by 4.8A and the RMS current by only 0.8A. These results prove the need for improvement in the performance of the DAB converter, especially at non-rated power operation.

In the DPS method, the optimized inner phases D_1 and D_2 , which are equal, are used in addition to the phase shift control. At high power operation, the optimized DPS method provides some improvement in peak current reduction and RMS current minimization compared to the SPS method. However, the effect of the optimized DPS method at reduced power operation is more apparent. At medium power, the peak current is 44.8A and the RMS current is 14.4A. At low power operation, the optimized DPS method reduces the peak current and the RMS current by more than 50%, which significantly improves the performance of the converter at low power.

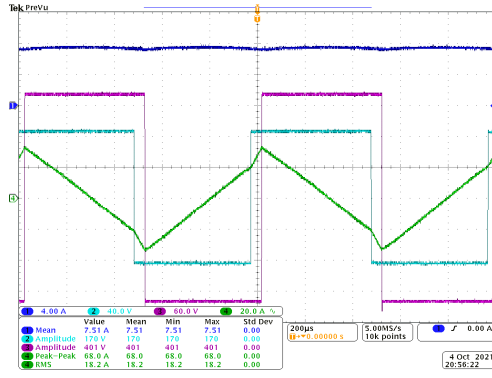


Fig. 6.51 DAB operation at rated power under the SPS method

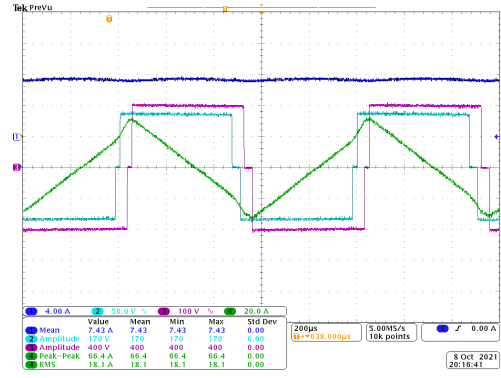


Fig. 6.52 DAB operation at rated power under the DPS method

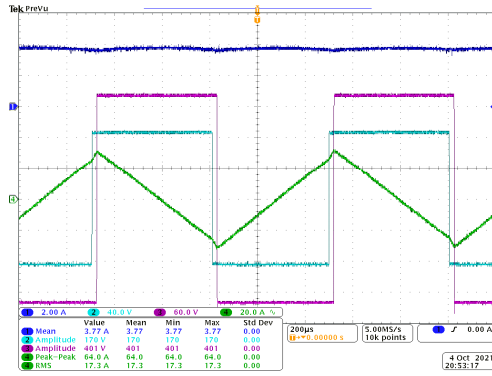


Fig. 6.53 DAB operation at medium power under the SPS method

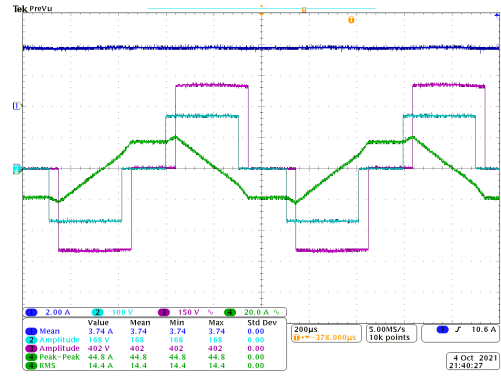


Fig. 6.54 DAB operation at medium power under the DPS method

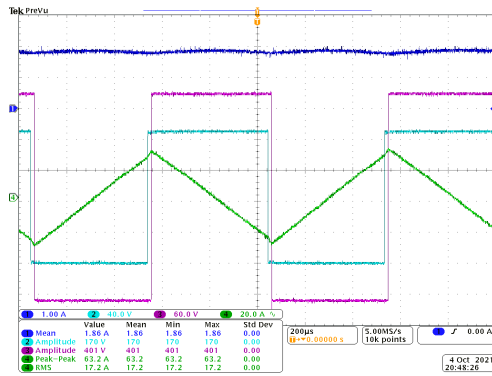


Fig. 6.55 DAB operation at low power under the SPS method

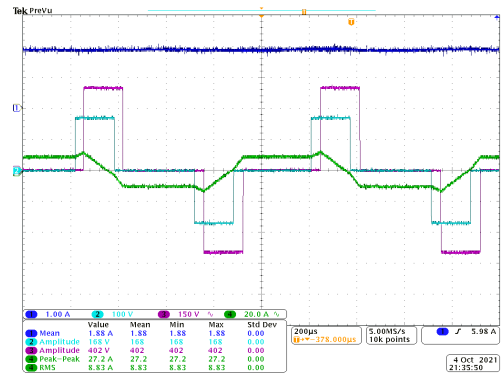


Fig. 6.56 DAB operation at low power under the DPS method

Fig. 6.57 - Fig. 6.59 show the performance of a single DAB converter in the ISOP system using the TPS method under all three operating zones. The TPS control can be seen in the shape of the primary and secondary voltages of the HFT. For the same power levels and voltage rating, it can be seen that the applied RMS current minimization strategy provides higher performance, as expected. Compared to both the SPS and DPS methods, the effectiveness of the TPS control

technique based RMS current minimization is obvious. At rated power, the peak and RMS currents are considerably reduced. Greater impact of this technique can be seen at medium and low power operations. Table 6.3 below summarizes the performance results of the three control methods.

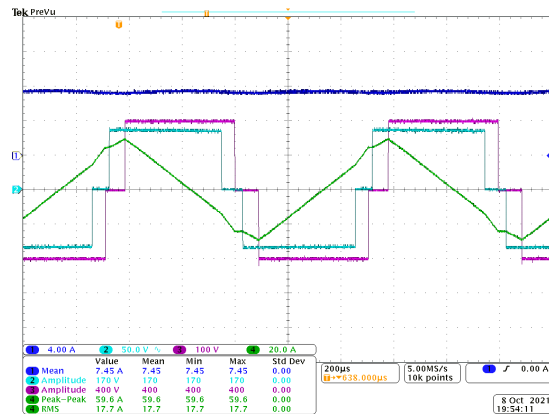


Fig. 6.57 DAB operation at rated power under the TPS method

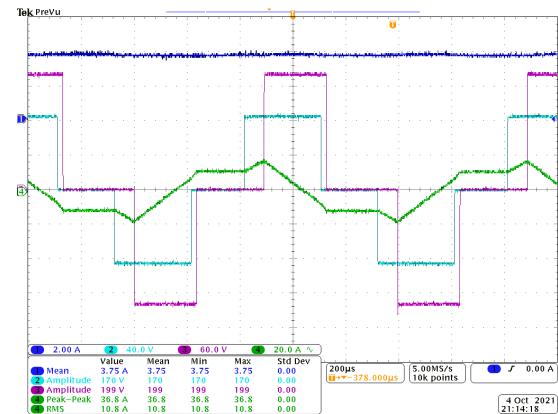


Fig. 6.58 DAB operation at medium power under the TPS method

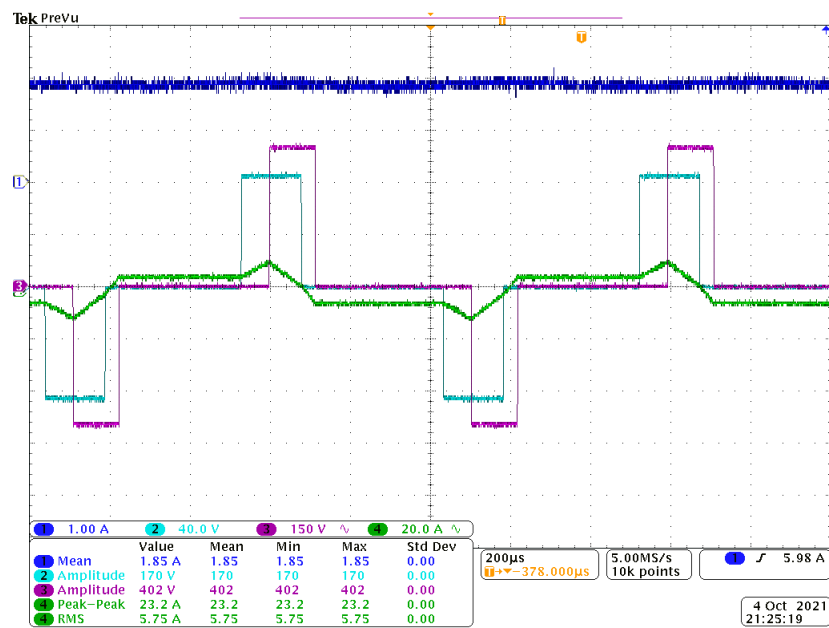


Fig. 6.59 DAB operation at low power under the TPS method

Table 6.3 Performance Comparisons of the RMS Current Minimization

| Control Methods | Rated Power | Medium Power | Low Power |
|-----------------|-------------|--------------|-----------|
| SPS I_{Peak} | 68.8 A | 64.0A | 63.2 A |
| DPS I_{Peak} | 66.4 A | 44.8 A | 27.2 A |
| TPS I_{Peak} | 59.6 A | 36.8 A | 23.2 A |
| SPS I_{RMS} | 18.2 A | 17.3 A | 17.2 A |
| DPS I_{RMS} | 18.1 A | 14.4 A | 8.83 A |
| TPS I_{RMS} | 17.7 A | 10.8 A | 5.75 A |

6.5.2 DAB Performance Based Total Power Loss Minimization

To further improve the performance of the DAB converter, a total power loss minimization scheme was employed. As noted in the optimization algorithms presented in Table 5.2, for the high power zone there is very little room to optimize the performance converter. However, at lower power, the optimization method based on the total power loss shows greater superiority than the RMS current minimization scheme. Utilizing total loss minimization, the three operation zones are presented in Fig. 6.60, Fig. 6.62, and Fig. 6.64 for the DPS control method. The TPS method is shown in Fig. 6.61, Fig. 6.63, and Fig. 6.65.

For the optimized TPS method, it can be seen at high power operation that power loss minimization provides equal performance as the RMS current minimization in reducing the peak current and the RMS current. However, the effectiveness of the optimized TPS method at reduced power operation is more apparent. At low power operation, the optimized TPS based power loss minimization method reduces the peak current and the RMS current by 0.8A and 1.04A, respectively. This significantly improves the performance of the converter at low power. The performance of the SPS, DPS, and TPS modulation techniques for both the RMS current

minimization and power loss minimization methods are summarized in Table 6.3 and Table 6.4, respectively.

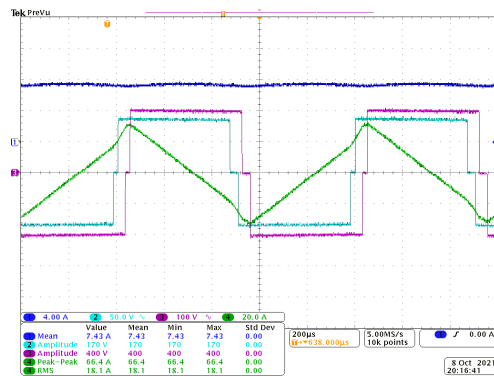


Fig. 6.60 DAB operation at rated power under the DPS based power loss minimization method

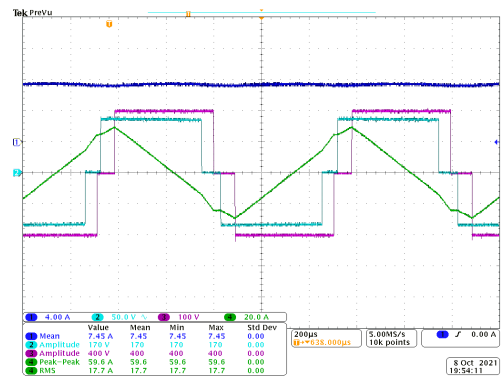


Fig. 6.61 DAB operation at rated power under the TPS based power loss minimization method

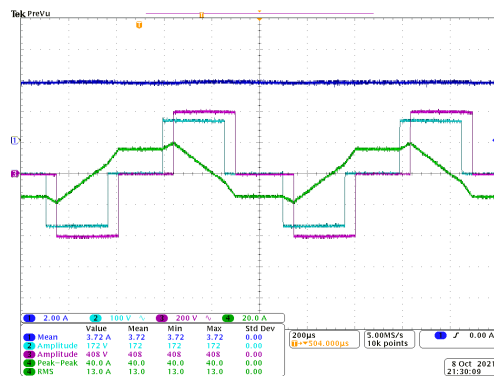


Fig. 6.62 DAB operation at medium power under the DPS based power loss minimization method

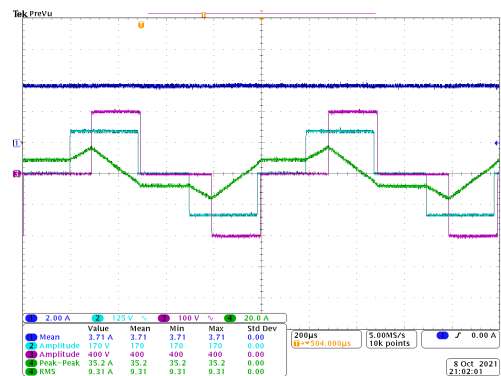


Fig. 6.63 DAB operation at medium power under the TPS based power loss minimization method

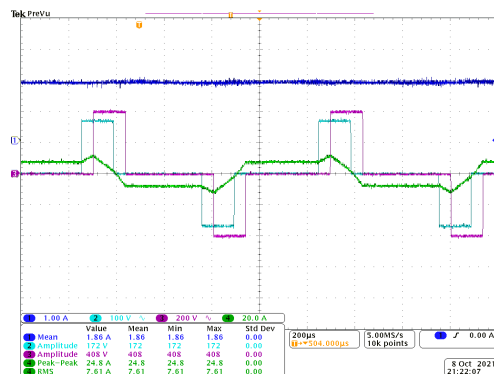


Fig. 6.64 DAB operation at low power under the DPS based power loss minimization method

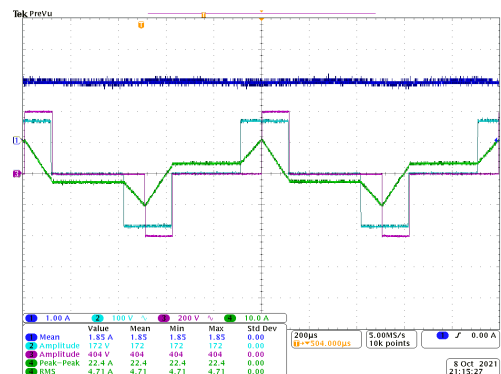


Fig. 6.65 DAB operation at low power under the TPS based power loss minimization method

Table 6.4 Performance Comparisons of the Power Loss Minimization

| Power Loss Minimization | Rated Power | Medium Power | Low Power |
|--------------------------------|-------------|--------------|-----------|
| SPS I_{Peak} | 68.8 A | 64.0A | 63.2 A |
| DPS I_{Peak} | 66.4 A | 40.0 A | 24.8 A |
| TPS I_{Peak} | 59.6 A | 35.2 A | 22.4 A |
| SPS I_{RMS} | 18.2 A | 17.3 A | 17.2 A |
| DPS I_{RMS} | 18.1 A | 13.0 A | 7.61 A |
| TPS I_{RMS} | 17.7 A | 9.31 A | 4.71 A |
| SPS efficiency | 96.1% | 88.56% | 77.74% |
| DPS efficiency | 96.58% | 92.13% | 88.34% |
| TPS efficiency | 98.75% | 97.46% | 92.25% |

For the same power levels and voltage rating, it can be seen that the applied power loss minimization strategy is superior to the RMS current minimization strategy, especially at low power operation. At rated power, the optimization is global. Thus, the performance for both optimization methods yields the same results for both peak and RMS currents. However, the significant impact of the power loss minimization strategy can be seen at both medium and low power operation. Compared to both DPS and TPS based RMS current minimization methods, the superiority of the TPS based power loss minimization is apparent.

The total efficiency of the DAB converter was calculated for all power regions for the SPS, DPS, and TPS modulation schemes for the power loss minimization strategy. Table 6.4 summarizes the results. It can be seen that the overall efficiency for the DAB converter was greatly improved utilizing TPS method based power loss minimization, especially at low power.

CHAPTER 7

Conclusion and Future Work

In this work, a multi-level converter architecture for MV AC to LV DC for fleet EV fast charging was developed to provide modular structure, scalability, galvanic isolation, and high efficiency. The overall controller structure is composed of two parts: the AFE and the DAB controls. For the AFE control, a robust current control structure based on a modified LF was implemented to achieve voltage balancing, regulate the AC current among all the stages of the converter, and provide low THD. To obtain the optimal efficiency, the DAB control structure was derived based on the TPS modulation scheme for two methods: RMS current minimization and power loss minimization. The power loss minimization scheme was found to be superior in improving the efficiency of the converter by providing lower RMS and peak currents and lower core and winding losses. Thus, the power loss minimization scheme was selected for this work. Additionally, an HFT was developed to provide isolation between the stages of the converter.

The control strategy that is proposed for the single-phase three-cell CHBML-AFE with LCL filter employs a modified LF based current control, a PI based voltage control, and a cell voltage balancing controller. A PI based voltage controller is used for the DC voltage control. It also generates the amplitude of the current reference signal. An additional capacitor voltage feedback loop is used to modify the conventional LF based control method in order to suppress the resonance introduced by the LCL filter. The AFE current reference signal is

generated by the designed PR controller to decrease the dependency on the system parameters and improve the robustness of the system. A DC voltage balancing control is also applied to keep the output voltage balanced, even when the load is unbalanced. Analysis of the grid current transfer function and the influence of the PR gains and LF control parameters have been studied to determine the performance of the employed control strategy. The simulation and experimental results prove that the proposed control strategy provides fast transient response, eliminates steady-state error, and keeps the cell voltages equal in both balanced and unbalanced conditions. Additionally, the current drawn from the grid is sinusoidal, resulting in a low THD.

An RMS current minimization technique based on Lagrange optimization for an ISOP of three modules was analyzed and found to be inferior to the power loss minimization method. Detailed analyses of the RMS current and average power transferred in the DAB for each mode and the power sharing controller for all operation zones were presented. Although the RMS minimization TPS based method can provide some improvement in the efficiency of the system by minimizing conduction and winding losses, that improvement is sub-optimal as the method offers little effect on the switching and core losses.

Contrary to the RMS current minimization method, which only affects two sources of loss, the power loss minimization method affects all four major sources of loss in the system: conduction, switching, winding, and core. This results in greater improvement in the efficiency of the system. Detailed formulations of each of the four sources of loss for three zones of operation were obtained and analyzed using the TPS method. These equations were used to formulate the final total loss expressions for each operation zone. The resulting loss expressions were then minimized to find the optimal TPS control variables based on two optimization methods, PSO and LM. The offline PSO method is utilized in LO and results in a numerical value. The LM is utilized in GO and results in a closed form expression. In the case of LO, although the

optimal duty cycles that minimize the total power loss are not necessarily the optimal values for the minimum RMS current or peak current stress, they still provide overall improvement in the efficiency due to their inclusion of all four sources of loss. Conversely, in the case of GO, the optimal duty cycles minimize the RMS, peak current, and power loss at the same time for the entire power range.

In addition to the robust current control of the AFE and the optimal TPS control of the DAB, the voltage balancing method was applied on the AFE side to maintain equal inner DC bus voltages and an inner current loop was added to the DAB. These allowed for equal power sharing between the converter modules under various conditions, such as converter shutdown and mismatch in module components, for the ISOP SST system.

This work demonstrates the superiority of the applied robust current control based modified LF and the optimal TPS modulation based total power loss minimization method for achieving higher overall efficiency for a fleet EV fast charger.

With the increasing demand for EVs and the need for extremely fast and efficient charging, continued research into improving various fleet fast chargers is necessary. For the specific concept of the system presented in this dissertation, ideas for future work must include insulation coordination requirements to accommodate high voltage and current as well as optimal thermal design for H-bridges and transformers.

LIST OF PUBLICATIONS

1. Development of a Data Analytics Platform for an Electrical/Water Microgrid. G. Jean-Pierre, H. Akbariaghaghighat, T. Zhao, A. Berger, N. Nafsin, F. Bin Nasir, H. Bravo, J. Lin, A. Nasiri, and M. Nowak. Power Electronics for Distributed Generation Systems (PEDG) 2021.
2. A Control Scheme for a DC Extreme Fast Charger with RMS Current Minimization. G. Jean-Pierre, S. Beheshtaein, N. Altin, and A. Nasiri. Power Electronics for Distributed Generation Systems (PEDG) 2021.
3. Sliding Mode Control Scheme for a Cascaded H-Bridge Multilevel Active Front End. G. Jean-Pierre, N. Altin, and A. Nasiri. Power Electronics for Distributed Generation Systems (PEDG) 2021.
4. An Optimal Design of a Hybrid Liquid/Air Cooling System for High Power, Medium Frequency, and Medium Voltage Solid-State Transformer. S. Beheshtaein, A. Alshafei, G. Jean-Pierre, N. Altin, M. Khayamy, and A. Nasiri. Power Electronics for Distributed Generation Systems (PEDG) 2021.
5. Control and Loss Analysis of a Solid State Transformer Based DC Extreme Fast Charger. G. Jean-Pierre, S. Beheshtaein, N. Altin, and A. Nasiri. 2021 IEEE Transportation Electrification Conference and Expo (ITEC)
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 11. A Three-Port LLC Resonant Converter for Photovoltaic-Battery Hybrid System. G. Jean-Pierre, N. Altin, and A. Nasiri. 2019 IEEE Transportation Electrification Conference and Expo (ITEC) A High Power High Frequency Transformer Design for Solid State Transformer Applications. A. El Shafei, S. Ozdemir, N. Altin, G. Jean-Pierre, and A. Nasiri. 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA)
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Curriculum Vitae

Education

PhD in Electrical Engineering: University of Wisconsin – Milwaukee

- Advisor: Prof. Adel Nasiri
- Degree Focus: Power Electronics
- Minor: Business Management
- September 2017 - December 2021

Master of Science in Electrical Engineering: University of Wisconsin – Milwaukee

- Advisor: Prof. Adel Nasiri
- Thesis title: Inductance Measurement Fixture and Mathematical Model Development to Support AC Drive System Simulation Tools.
- Degree Focus: Controls Systems and Power Electronics
- Graduated May 2017

Bachelor of Science in Electrical Engineering: University of Wisconsin – Milwaukee

- Graduated Cum Laude
- Graduated May 2016

Work Experience

Electrical Engineering Intern – Eaton Research Lab: September 2020 – Current

- **Project: DC Fast Charger**
- Developed and mapped control requirements for DC fast charger
- Contributed to design of interface boards for main and local controllers by extracting sensor scaling data and modifying LTspice simulations
- Contributed to controller and software design by developing protection functions and trip settings, and implementing start/stop functions
- Designed and implemented fault handling state machines, protection schemes, and signal conditioning in MATLAB/Simulink
- Developed model based design software for local controllers by creating an autocode generation framework in MATLAB/Simulink

- Designed a precharge function by implementing a duty cycle control for the dual active bridge (DAB) converter
- Developed HMI based VT100 for system level software testing
- Developed a test plan for board level and system level testing

Teaching Assistant – University of Wisconsin – Milwaukee, Department of Computer and Electrical Engineering and Applied Sciences: September 2021 – Current

- Teach Introduction to Control Systems course ELECENG 474/474G

Research Assistant – Center for Sustainable Electrical Energy Systems, University of Wisconsin – Milwaukee: May 2017 – August 2021

- **Development of a multi-level direct medium voltage DC fast battery charger**
- Developed a medium voltage AC to low voltage DC input series output parallel (ISOP) DAB multilevel converter as an isolated modular controllable converter
- Modeled and simulated the multi-level inverter and the ISOP DAB converter using MATLAB/Simulink
- Performed optimization for the high frequency transformer design using PE/Expert
- Developed the control strategy for controlling the multilevel inverter based on the Lyapunov control technique
- Developed the control strategy for the ISOP DAB with RMS current and power loss minimization control and power sharing algorithm
- **Development of a compact multiport bidirectional LLC resonant converter for grid-tied photovoltaic-battery hybrid system**
- Proposed new converter topology for integrating PV battery and utility grid
- Proposed new maximum power point tracking technique for controlling the battery current using MATLAB/Simulink
- **Modular Expeditionary Technology Evaluation Resource (METER) for Eaton/US Air Force**
- Identified new technologies and assets to be evaluated for the METER concept
- Identified and developed specifications for an electrical distribution system
- Developed a real time simulation model using the Typhoon HIL for a full scale microgrid system, including sensors for various electrical key performance indicators
- Developed an electrical test bed for system validation
- Provided report and presented on identification of technologies and assets to be evaluated for the METER concept and electrical system design, components, specifications and modeling results
- **Basic Expeditionary Airfield Resources (BEAR) for Eaton/US Air Force**

- Supported the development of a distributed energy system for demonstration and validation of power technology
- Provided technical expertise in electrical power generation, distribution, and conversion systems
- Modeled and simulated the legacy expeditionary technologies and resources to provide design evaluation and integration capability to enable high confidence validation of energy and sustainment resource technologies using PSCAD

Control Hardware Intern – Rockwell Automation: December 2015 – May 2017

- Performed testing and verification for new and existing boards
- Designed the analog section for a low power control board using LTSpice and Mentor Graphics
- Wrote firmware supported test procedures
- Performed inductance measurement fixture and mathematical model development to support AC drive system simulation tools using Simplorer, ANSYS and GOSET
- Assisted in the control development platform for SiC design

Quality Engineer Intern – Rockwell Automation: Summer 2015

- Collected and analyzed quality data
- Worked in the quality lab on analysis and fixtures of defective drives
- Wrote customer-oriented quality improvement reports

Academic Activities

Peer Reviewer

- Reviewed journal articles and conference papers for IEEE IAS, Sustainability (MDPI), Energies (MDPI), ITEC, ECCE, APEC, PEDG, and ICRERA

Co-founder and Vice President

- UW-Milwaukee Institute of Electrical and Electronic Engineers Power and Energy Society Student Branch (IEEE-PELS/IAS/IES): Spring 2015 – Spring 2016

Treasurer

- UW- Milwaukee Student Branch of the Optical Society of America: September 2015 – May 2018

University Innovation Fellow: Jan 2015 – Current

Electrical Engineering Program Representative

- UW-Milwaukee: January 2015 – December 2015

Math Engineering Tutor

- UW-Milwaukee: January 2014 – May 2016