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Wireless Power Transfer Using Class-De Converter Via Strongly Coupled Two Planar Coils

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WIRELESS POWER TRANSFER USING CLASS-DE CONVERTER VIA STRONGLY COUPLED TWO PLANAR COILS

by

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ABSTRACT

WIRELESS POWER TRANSFER USING CLASS-DE CONVERTER
VIA
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Wireless power systems are getting popular with the improvement in the technology not just because it is a fancy and cool conception but also because it is more convenient and safer in some applications. For example, this project aims to help high power data center design to be changed to wirelessly powered center to provide a safe and hands-on work environment even under different load conditions. Thinking of the basic conception of magnetic induction theory, electric power ranging from microwatts to thousand watts can be wirelessly transferred from one coil to another without having a core material. The purpose of this project is to apply high efficiency class-de converter methodology to obtain alternating current so that this alternating current is transmitted from primary coil to secondary while being stepped up as required within the project specifications. At the load side is a full bridge diode rectifier that is converting the captured alternating current back to direct current. In the scope of this project, mathematical calculations for the circuit elements' values under the class-de power amplifier topology, simulation results, and feedback control method will be discussed.

To

Turkish Government,

my Family,

and those who supported me.

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CHAPTER I

INTRODUCTION

A wireless power system is a system that is capable of transferring electrical power from a power source to an electrical load without having any electrical connections. This system may transfer electrical power ranging from microwatts to megawatts with sufficient circuit components and design. In a basic wireless power system there can be three main bodies: DC-AC converter, Transmitter and Receiver Coils, AC-DC Converter. Besides these, there are different control systems and switching methods. In addition to its power range, a wireless power system may be divided into three for its ability to transfer power to varying distances: Short Distance, Medium Distance, and Long Distance. Distance range has a magnificent amount of affect on efficiency of the overall system as the transferred electrical power degrades with the distance. In other way, the distance will assign the coupling factor between two coils, as it is equal to 1 for an ideal transformer.

As Maxwell has proved, the magnetic induction theory allows the receiver coil to capture the magnetic fields and induce current on it. However, the important part here is to capture as many as magnetic field lines to keep the efficiency at highest point. Because of this reason, having two inductively coupled planar coils with enough surface area is one of the most efficient designs for the wireless power systems. In this project, we have two parallel planar coils with different numbers of turns. Aim is to capture most of the magnetic waves that are produced by the primary coil and circulating in the air freely. The design of the planar coils is beyond the scope of this project and was studied by my friend Ethan Zimany as his master's degree thesis topic.

In this project, the requirements are given so the output has to be at $10V_{dc}$ and supplying $500W$, the coils have a gap of 2mm maximum distance in between. For the easiness, the input dc source will have enough voltage level to be able to supply the class-DE converter's needed voltage level.

Class-D Power Amplifier

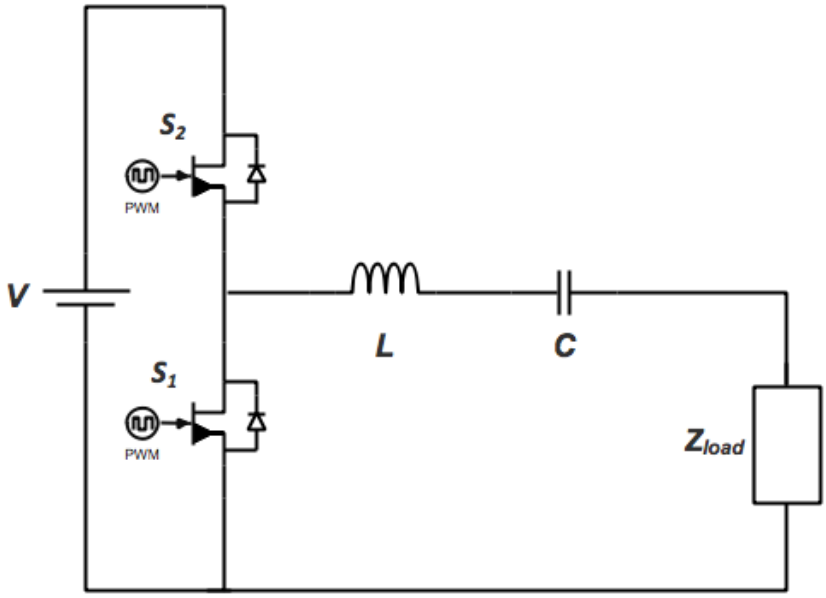

Figure 1.1: Class-D Power Amplifier Circuit Schematics

Class-D power amplifiers are known with their high efficiency operations in power electronics under high frequency applications. Timing the switching action of the transistors at zero voltage is the key point of this kind of amplifiers. The transistors are controlled with 50% fixed duty cycle so that the transistor voltage and current waveforms alternate right on time. One of the advantages of class-D amplifiers is that having same amount of supplier voltage stress across the transistors, enabling them to function at high voltage levels. [1]

A class-D inverter circuit with ideal components can achieve 100% efficiency. However, in real life, the contributors to power loss in a class-D system are the transistor losses and the series resistance of both the inductor and capacitor.

Class-E Power Amplifier

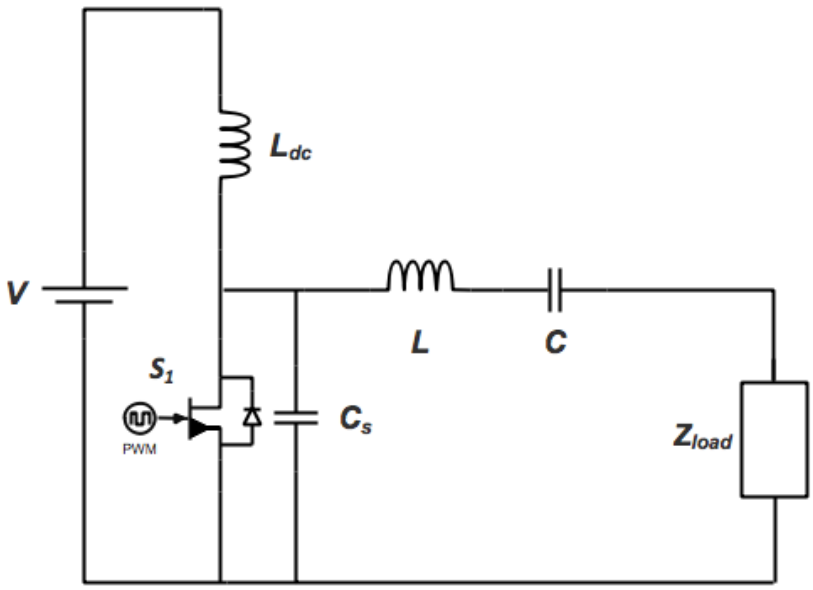

Figure 1.2: Class-E Power Amplifier Circuit Schematics

Class-E type power amplifiers are consisted of single switch in contrast to class-D types, making it easier to build and use. The complexity of out-of-phase two PWM gate signals is eliminated. In class-E power amplifiers, amount of power delivered to the output is higher than class-D type of converters with the same supply voltage level. On the other hand, in this type of converters, transistor has a 3.562 times of input voltage level on it. In other words, high stress on the transistor will refrain users utilizing this topology where the application requires high voltage at the input. [2]

CHAPTER II

WIRELESS POWER TRANSFER SYSTEM

This project's outline consists of two main parts: High Efficiency Class-DE Power Amplifier and Resonant Inductive Planar Coils. The focus of this paper will be on the converter design and power electronics where Ethan Zimany studied the detailed design steps of transmitter and receiver coils. Project requires the system to have $500W$ power at full load and a constant $10V_{dc}$ voltage at the output. The switching frequency of the transistors is 30kHz. Under these operating conditions, a highly efficient high current wireless power system is simulated and built as a prototype. The following subsections will define each main system, provide formulation for the circuit design, explain and prove the overall system's practicality. Below figure 2.1 depicts the general concept of the overall system.

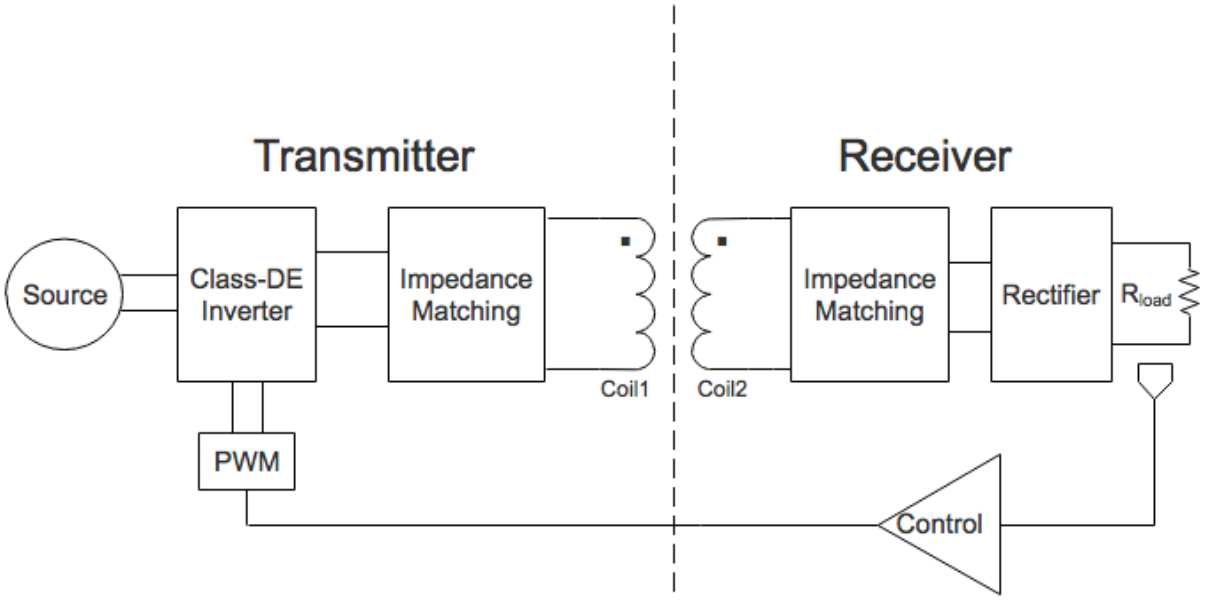

Figure 2.1: Proposed Wireless Power Transfer System Diagram

Class-DE Converter Design

Class-DE power amplifiers are not recently explored; however, their usage became more common in power electronics with the increasing interest in wireless systems. A class-DE power amplifier can be modeled by two series transistors in parallel with a dc voltage source, two shunt capacitors across the each of these transistors, a series inductor-capacitor pair that is connected from the mid-point of the two transistors, and in series to that a load is connected as shown in figure 2.2.a.

We can simply say that class-DE topology is brought together by picking the advantages of both class-D and class-E amplifiers leaving out their lacks or disadvantages. As in class-D, class-DE has 2 transistors with less stress across them, as well as higher power pushing capability as in class-E. Eventually, after a careful design, the expected waveforms should occur as displayed in figure 2.3.

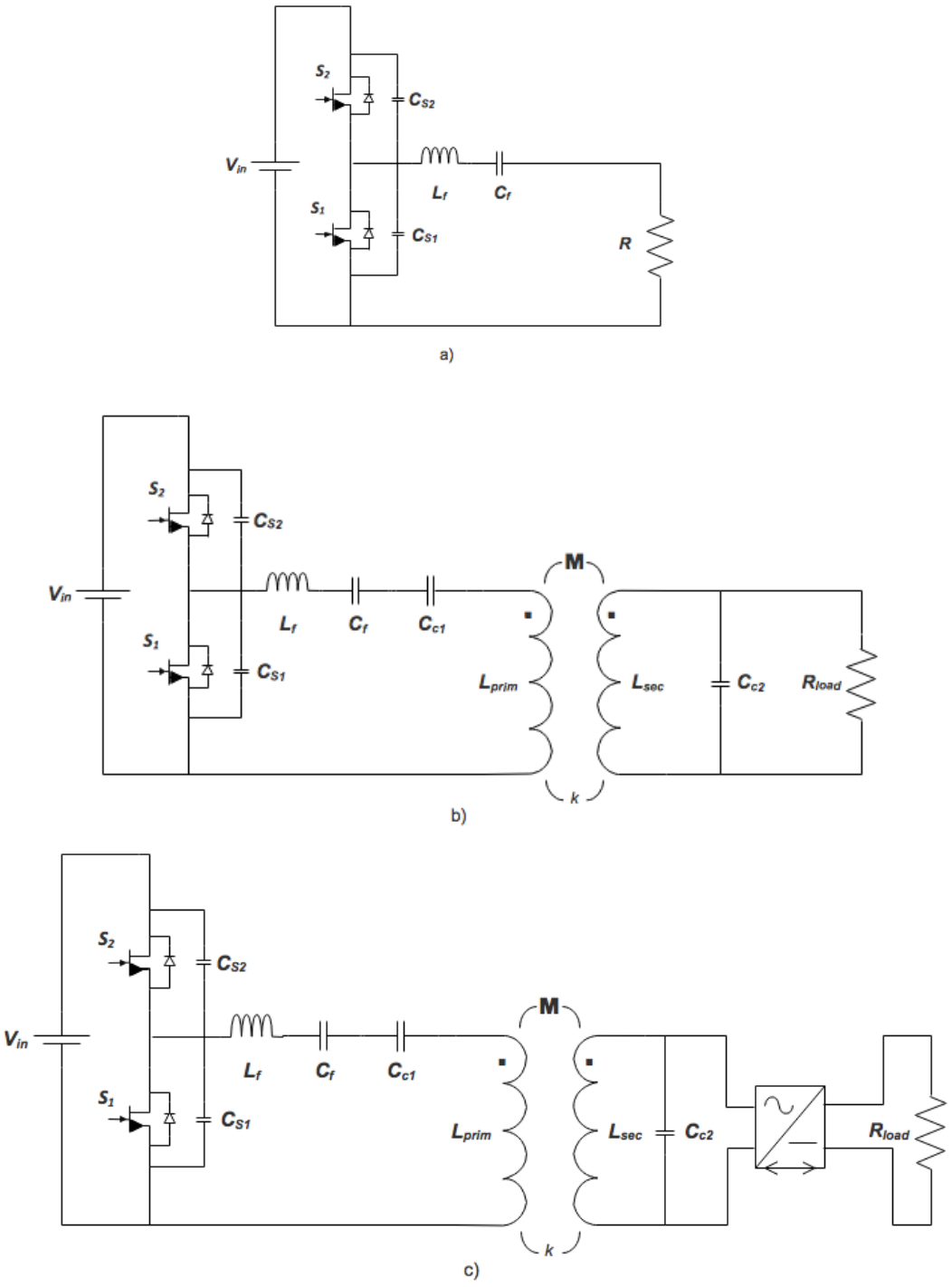

Figure 2.2: a) Class-DE Power Amplifier Circuit Schematics b) Class-DE Power Amplifier with Inductive Coils and Load c) Class-DE Power Amplifier with Inductive Coils, Rectifier, and Load

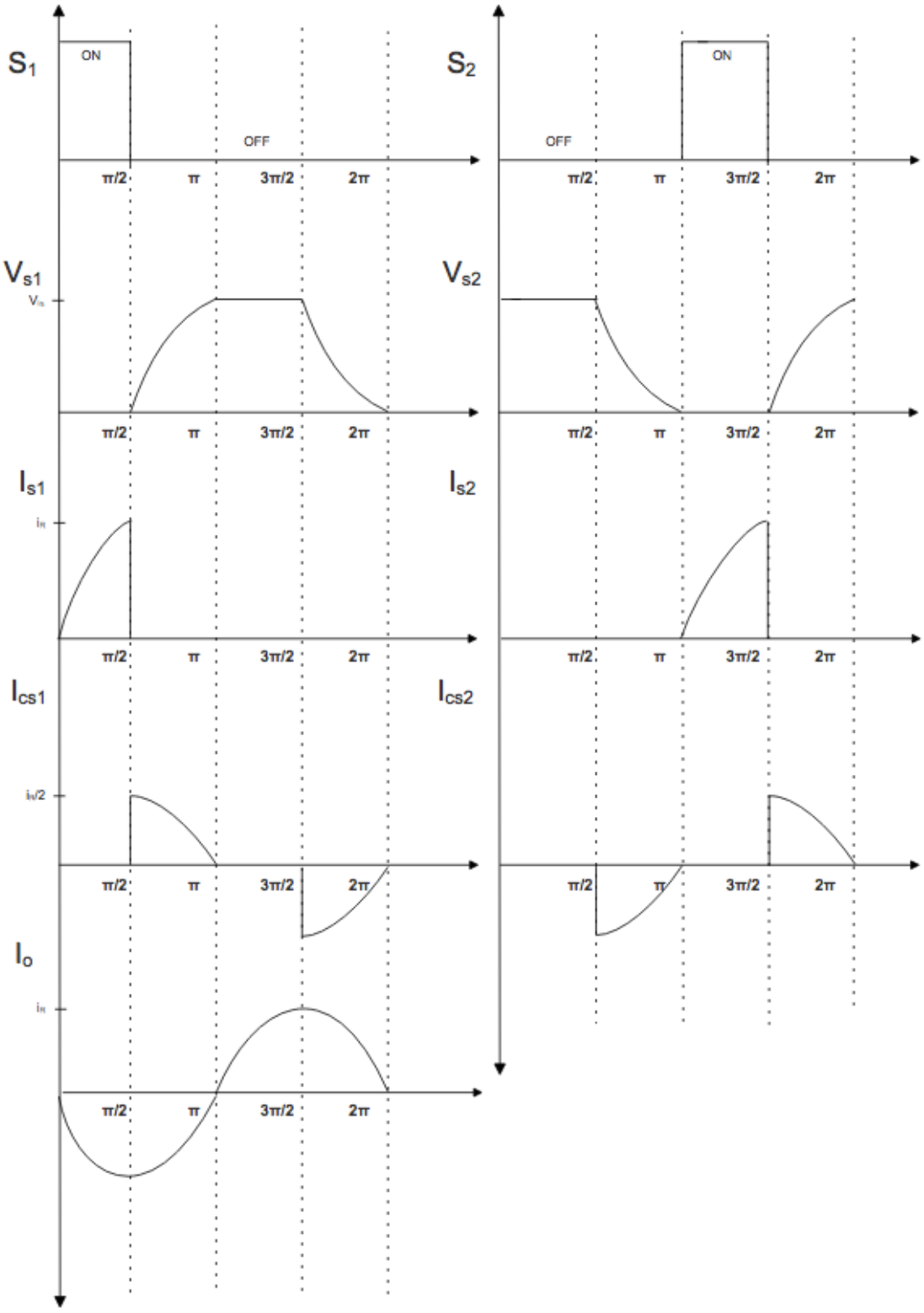

Figure 2.3: Waveforms of a Class-DE Power Amplifier

Based on paper [3], the class-DE power amplifiers are operated at fixed duty cycle of 25%. The operating mode requires ON mode of one switch at a time for 25% of the PWM signal. Between ON times of two transistors, there are two 25% of dead times, where both transistors are OFF. The driving pattern is shown in table 2.1 where θ is the angular time.

	$\mathbf{0 < \theta < \frac{\pi}{2}}$	$\mathbf{\frac{\pi}{2} < \theta < \pi}$	$\mathbf{\pi < \theta < \frac{3\pi}{2}}$	$\mathbf{\frac{3\pi}{2} < \theta < 2\pi}$
$\boldsymbol{S_1}$	ON	OFF	OFF	OFF
$\boldsymbol{S_2}$	OFF	OFF	ON	OFF

Table 2.1: Driving Pattern of the Transistors

The loaded quality factor of the class-DE converter, Q, should be high enough to obtain sinusoidal waveforms. For this project, Q is selected to be 10. The circuit analysis is made as below to provide simple formula for each element with some assumptions [3].

Primary equations for the circuit analysis are listed assuming ideal switch conditions:

$$i_{s2}(\theta) + i_{cs2}(\theta) = i_{s1}(\theta) + i_{cs1}(\theta) + i_o(\theta) \quad (1)$$

$$v_{s1}(\theta) = V_{in} - v_{s2}(\theta) \quad (2)$$

$$i_{out}(\theta) = I_{out} \sin(\theta + \varphi) \quad (3)$$

$$i_{cs1}(\theta) = \omega C_{s1} \frac{dV_{s1}(\theta)}{d(\theta)} \quad (4)$$

$$i_{cs2}(\theta) = \omega C_{s2} \frac{dV_{s2}(\theta)}{d(\theta)} \quad (5)$$

$$\omega = \frac{1}{\sqrt{L_f C_f}} \quad (6)$$

$$Q = \frac{\omega L_r}{R} \quad (7)$$

$$L_r = L + L_f \quad (8)$$

$$v_{s1}(\theta) = 0 \ \ where \ \ (0 \leq \theta \leq \frac{\pi}{2}) \tag{9}$$

$$i_{s1}(\theta) = 0 \ \ where \ \ (\frac{\pi}{2} \leq \theta \leq 2\pi) \tag{10}$$

$$v_{s2}(\theta) = 0 \ \ where \ \ (\pi \leq \theta \leq \frac{3\pi}{2}) \tag{11}$$

$$i_{s2}(\theta) = 0 \ \ where \ \ (0 \leq \theta \leq \pi \ \ and \ \frac{3\pi}{2} \leq \theta \leq 2\pi) \tag{12}$$

ZVS and ZVDS conditions are provided with below equations:

$$v_{s1}(2\pi) = 0 \ \ and \ \frac{dv_{s1}(\theta)}{d(\theta)}\Big|_{\theta=2\pi} = 0 \tag{13}$$

$$v_{s2}(\pi) = 0 \ \ and \ \frac{dv_{s1}(\theta)}{d(\theta)}\Big|_{\theta=\pi} = 0 \tag{14}$$

To analyze the circuit easily, we will divide the circuit into 4 intervals:

<u>Interval 1</u> **$(0 \leq \theta \leq \frac{\pi}{2})$:**

In this case only the bottom switch S_1 is closed and conducting. The equivalent circuit is given as in figure 2.4.

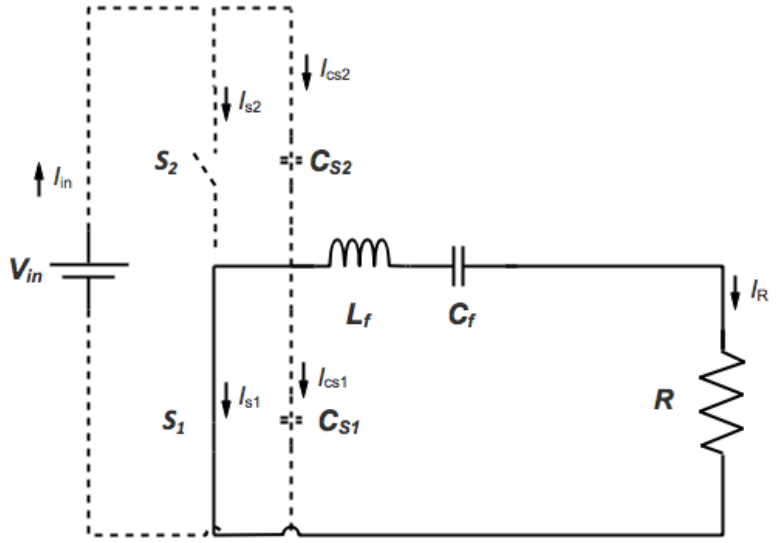

Figure 2.4: Class-DE Operation Mode During Interval 1

Since the S_1 will be conducting, there will be no voltage stress across it, therefore resulting in zero current flowing in ideal conditions. Integrating equation (9) into (4) will prove the statement.

$$i_{cs1}(\theta) = 0 \tag{15}$$

Integrating (9) into (2) will give us the voltage across the S_2 and shunt capacitor across it C_{S2}. Having constant voltage across a capacitor will result in zero current in ideal conditions as we can see from equations (16) and (5).

$$v_{s2}(\theta) = V_{in} \tag{16}$$

$$i_{cs2}(\theta) = 0 \tag{17}$$

(3), (12), (15), and (17) will be placed in equation (1) and hence we get the current flowing through the circuit during interval 1.

$$i_{s1}(\theta) = I_{out} \sin(\theta + \varphi) \tag{18}$$

<u>Interval 2</u> **$(\frac{\pi}{2} \leq \theta \leq \pi)$:**

In this range, both of the transistors are open and do not conduct. Figure 2.5 below is the equivalent circuit of this interval showing the current flow directions and switch states. This time, instead of transistor currents, we will have shunt capacitor currents in our Kirchhoff current equation (1).

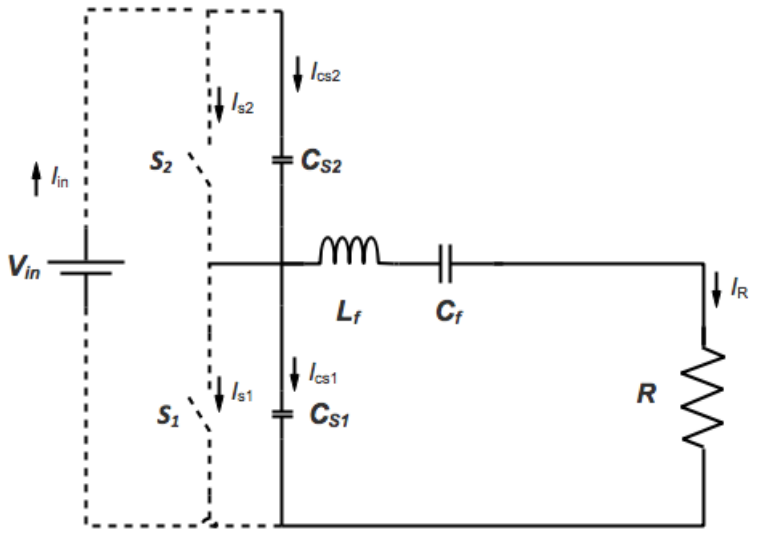

Figure 2.5: Class-DE Operation Mode During Interval 2

Substituting (3), (4), (10), and (12) into (1) we obtain

$$-\omega c_{s1}\frac{dV_{s1}(\theta)}{d(\theta)} + \omega c_{s2}\frac{dV_{s2}(\theta)}{d(\theta)} = I_{out}\ \sin(\theta+\varphi) \tag{19}$$

Substituting (2) for $V_{s1}(\theta)$ into (19)

$$\frac{dV_{s2}(\theta)}{d(\theta)} = \frac{I_{out}}{w(c_{s1}+c_{s2})}\sin(\theta+\varphi) \tag{20}$$

Integrating equation (20)

$$v_{s2}(\theta) = \int_{\frac{\pi}{2}}^{\theta}\frac{I_{out}}{w(c_{s1}+c_{s2})}\sin(u+\varphi)du + v_{s2}(\frac{\pi}{2}) \tag{21}$$

Hence it is found from equation (2) and (9)

$$v_{s2}\left(\frac{\pi}{2}\right) = V_{in} \tag{22}$$

To solve for φ, using equation (22) in integration of (21) results in

$$v_{s2}(\theta) = V_{in} - \frac{I_{out}}{w(c_{s1}+c_{s2})}\{\cos(\theta+\varphi) - \cos\left(\frac{\pi}{2}+\varphi\right)\} \tag{23}$$

Substituting (14) into (23) and solving for φ, we find

$$\sin\left(\varphi-\frac{\pi}{4}\right) = \frac{w(C_{s1}+C_{s2})V_{in}}{\sqrt{2}I_{out}} \tag{24}$$

Also, substituting (14) into (20) and solving for φ, we get

$$\sin(\varphi + \pi) = 0, \quad so \quad \varphi = 0 \quad or \quad \varphi = \pi \tag{25}$$

For $\varphi = 0\ and\ \pi$ consequently, (24) becomes

$$-\frac{1}{\sqrt{2}} = \frac{w(C_{s1}+C_{s2})V_{in}}{\sqrt{2}I_{out}} \tag{26}$$

$$\frac{1}{\sqrt{2}} = \frac{w(C_{s1}+C_{s2})V_{in}}{\sqrt{2}I_{out}} \tag{27}$$

For the convenience, we consider $\varphi = \pi$ so that the flow direction of the output current I_o stays positive. So the following equations are determined for the output current equation.

$$I_{out} = w(C_{s1} + C_{s2})V_{in} \tag{28}$$

$$\varphi = \pi \tag{29}$$

Placing (28) and (29) into (23), we get equation (30). Using equation (30) and (2), we obtain equation (31) for $v_{s1}(\theta)$.

$$v_{s2}(\theta) = V_{in}(1 + \cos\theta) \tag{30}$$

$$v_{s1}(\theta) = -V_{in}\cos\theta \tag{31}$$

To find the currents flowing through the shunt capacitors we substitute (31) into (4) and (30) into (5) respectively.

$$i_{Cs1} = wC_{s1}V_{in}\sin\theta \tag{32}$$

$$i_{Cs2} = -wC_{s2}V_{in}\sin\theta \tag{33}$$

Finally, the output current during this interval can be found from equation (3) and (29).

$$i_{out}(\theta) = -I_{out}\sin\theta \tag{34}$$

Interval 3 **($\pi \leq \theta \leq \frac{3\pi}{2}$):**

This interval is the symmetry of the interval 1, in other words, the bottom switch S_1 is open and the top switch S_2 is closed. So knowing that, we can analyze the circuit as in interval 1. Equivalent circuit of this interval is as below.

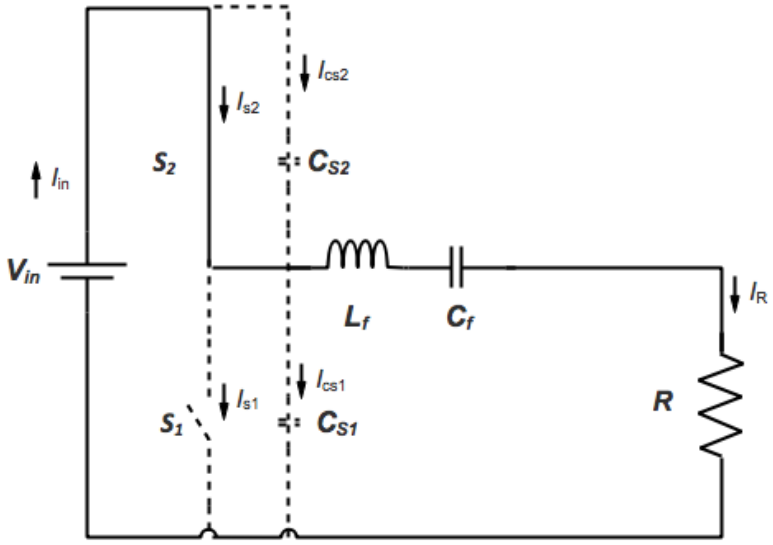

Figure 2.6: Class-DE Operation Mode During Interval 3

To start with, we know that there is no current flowing through the shunt capacitor C_{S2}. The voltage across the switch S_1 and shunt capacitor C_{S1} are equal to input voltage. Therefore, resulting from equations (4) and (36) there will be no current flowing through the shunt capacitor C_{S1}.

$$i_{Cs2}(\theta) = 0 \tag{35}$$

$$v_{S1}(\theta) = Vin \tag{36}$$

$$i_{Cs1}(\theta) = 0 \tag{37}$$

Using equations (10), (35), and (37) in equation (1) and having the equation (34) as a source we get

$$i_{S2}(\theta) = i_{out}(\theta) = -I_{out} \sin\theta \tag{38}$$

Interval 4 $\left(\frac{3\pi}{2} \leq \theta \leq 2\pi\right)$**:**

As in interval 2, during this interval, both of the switches are open. The equivalent circuit is same as figure 2.5 but shunt capacitor currents flow in the opposite directions with respect to interval 2.

If we substitute (10), (11), and (34) into the equation (1)

$$i_{Cs2}(\theta) - i_{Cs1}(\theta) = -I_{out} \sin\theta \tag{39}$$

Placing (2), (4), and (5) into (39)

$$\frac{dv_{S2}(\theta)}{d\theta} = -\frac{I_{out}}{w(C_{S1}+C_{S2})} \sin\theta \tag{40}$$

Integrating (40)

$$v_{S2}(\theta) = \int_{\frac{3\pi}{2}}^{\theta} -\frac{I_{out}}{w(C_{S1}+C_{S2})} \sin u \, du + v_{S2}(\tfrac{3\pi}{2}) \tag{41}$$

Substituting (11) into (41)

$$v_{S2}(\theta) = \frac{I_{out}}{w(C_{S1}+C_{S2})} \cos\theta \tag{42}$$

Substituting (28) into (42), we get voltage across the S_2 (43) and if we take its derivative, we obtain (44).

$$v_{S2}(\theta) = Vin \cos\theta \tag{43}$$

$$\frac{dv_{S2}(\theta)}{d\theta} = -V_{in} \sin\theta \tag{44}$$

From (2) and (43), we get voltage across the S_1 (45) and its derivative (46)

$$v_{S1}(\theta) = V_{in}(1 - \cos\theta) \tag{45}$$

$$\frac{dv_{S1}(\theta)}{d\theta} = V_{in} \sin\theta \tag{46}$$

Using the derivative equation (46) and (44) in (4) and (5) respectively, we come up with current equations that are flowing through shunt capacitors C_{S1} and C_{S2}.

$$i_{Cs1}(\theta) = wC_{S1}V_{in}\sin\theta \tag{47}$$

$$i_{Cs2}(\theta) = w - C_{S2}V_{in}\sin\theta \tag{48}$$

As a result, we can gather up 7 general equations for the all interval periods using the above findings.

$$v_{S1}(\theta) = \begin{cases} 0 & (0 < \theta \leq \frac{\pi}{2}) \\ -V_{in}\cos\theta & (\frac{\pi}{2} < \theta \leq \pi) \\ V_{in} & (\pi < \theta \leq \frac{3\pi}{2}) \\ V_{in}(1-\cos\theta) & (\frac{3\pi}{2} < \theta \leq 2\pi) \end{cases} \tag{49}$$

$$v_{S2}(\theta) = \begin{cases} V_{in} & (0 < \theta \leq \frac{\pi}{2}) \\ V_{in}(1+\cos\theta) & (\frac{\pi}{2} < \theta \leq \pi) \\ 0 & (\pi < \theta \leq \frac{3\pi}{2}) \\ V_{in}\cos\theta & (\frac{3\pi}{2} < \theta \leq 2\pi) \end{cases} \tag{50}$$

$$i_{S1}(\theta) = \begin{cases} I_{out}\sin\theta & (0 < \theta \leq \frac{\pi}{2}) \\ 0 & (\frac{\pi}{2} < \theta \leq \pi) \\ 0 & (\pi < \theta \leq \frac{3\pi}{2}) \\ 0 & (\frac{3\pi}{2} < \theta \leq 2\pi) \end{cases} \tag{51}$$

$$i_{S2}(\theta) = \begin{cases} 0 & (0 < \theta \leq \frac{\pi}{2}) \\ 0 & (\frac{\pi}{2} < \theta \leq \pi) \\ -I_{out}\sin\theta & (\pi < \theta \leq \frac{3\pi}{2}) \\ 0 & (\frac{3\pi}{2} < \theta \leq 2\pi) \end{cases} \tag{52}$$

$$i_{Cs1}(\theta) = \begin{cases} 0 & (0 < \theta \leq \frac{\pi}{2}) \\ wC_{S1}V_{in}\sin\theta & (\frac{\pi}{2} < \theta \leq \pi) \\ 0 & (\pi < \theta \leq \frac{3\pi}{2}) \\ wC_{S1}V_{in}\sin\theta & (\frac{3\pi}{2} < \theta \leq 2\pi) \end{cases} \tag{53}$$

$$i_{Cs2}(\theta) = \begin{cases} 0 & (0 < \theta \leq \frac{\pi}{2}) \\ -wC_{S2}V_{in}\sin\theta & (\frac{\pi}{2} < \theta \leq \pi) \\ 0 & (\pi < \theta \leq \frac{3\pi}{2}) \\ -wC_{S2}V_{in}\sin\theta & (\frac{3\pi}{2} < \theta \leq 2\pi) \end{cases} \quad (54)$$

$$i_{out}(\theta) = -I_{out}\sin\theta \quad (55)$$

The average input current can be calculated using the integral of the summation two branches' current. Additionally, we think of identical shunt capacitors.

$$I_D = \frac{1}{2\pi}\int_0^{2\pi}\{i_{S2}(\theta) + i_{Cs2}(\theta)\}d\theta = \frac{w(C_{S1}+C_{S2})}{2\pi}V_{in} \quad (56)$$

$$C_{S1} = C_{S2} \equiv C \quad (57)$$

Using equation (57) we understand that currents flowing through the shunt capacitors will be same and half of the output current that is $I_{out}/2$. The current and waveforms of the proposed amplifier elements can be found in figure 2.3.

We can calculate the magnitudes of the voltages with the help of Fourier analysis. To start with the output voltage

$$v_{out}(\theta) = V_{out}(-\sin\theta) \quad (58)$$

$$V_{out} = RI_{out} \quad (59)$$

The voltage across the series inductor L is

$$v_L(\theta) = V_L(-\cos\theta) \quad (60)$$

$$V_L = wLI_{out} \quad (61)$$

The fundamental frequency component of the switch voltage is

$$v_{S1}(\theta) = v_{out}(\theta) + v_L(\theta) \quad (62)$$

Using (59) and (61)

$$\frac{V_L}{V_{out}} = \frac{wL}{R} \quad (63)$$

Finally applying the Fourier analysis to the output and series inductance voltage equations

$$V_{out} = \frac{1}{\pi}\int_0^{2\pi} v_{S1}(\theta)(-\sin\theta)d\theta = \frac{V_{in}}{\pi} \tag{64}$$

$$V_L = \frac{1}{\pi}\int_0^{2\pi} v_{S1}(\theta)(-\cos\theta)d\theta = \frac{V_{in}}{2} \tag{65}$$

To be able to calculate the efficiency of an ideal system like this, first we need to come up with input and output powers. Using average input current equation (56) and knowing the input dc voltage

$$P_{in} = V_{in}I_D = \frac{w(C_{S1}+C_{S2})}{2\pi}V_{in}^2 \tag{66}$$

Also, output current and voltage equations, (28) and (64) respectively, will result in output power

$$P_{out} = \frac{I_{out}V_{out}}{2} = \frac{w(C_{S1}+C_{S2})}{2\pi}V_{in}^2 \tag{67}$$

Thus leaving out a 100% efficiency of conversion that is shown as

$$\eta = \frac{P_{out}}{P_{in}} = 1 \tag{68}$$

So far, all the above equations have proved that the high efficiency class-DE type power amplifier is an ideal candidate for an application where the coil-coupling factor is so high that most of the efficiency drop would be caused by the converter. Class-E switching conditions are also applied as seen in waveforms in figure 2.3.

Now, we need to find the component values to build a circuit for simulation as a stepping-stone. From equations (64) and (67), either output or input power can be expressed as follows.

$$P = \frac{V_{out}^2}{2R} = \frac{V_{in}^2}{2R\pi^2} \tag{69}$$

The load resistance R and the shunt capacitors Cs can be found as below if we have the input voltage V_{in} and the power P.

$$R = \frac{V_{in}^2}{2\pi^2 P} = \frac{1}{2\pi w C} \tag{70}$$

$$C = C_{S1} = C_{S2} = \frac{1}{2\pi w R} = \frac{\pi P}{w V_{in}^2} \tag{71}$$

Placing both (63) and (64) into (62) to solve for the inductance L

$$L = \frac{\pi R}{2w} \tag{72}$$

Using (7), (8), and (72)

$$L_f = Q\frac{R}{w} \tag{73}$$

$$L_r = L_f - L = (Q - \frac{\pi}{2})\frac{R}{w} \tag{74}$$

To solve for series capacitor C_f, placing (74) for L_r in (6)

$$C_f = \frac{1}{w^2 L_f} = \frac{1}{wR(Q - \frac{\pi}{2})} \tag{75}$$

Assuming the receiver side resonant frequency to be same as switching frequency f_s, the value of the receiver coil compensation capacitor C_{C2} that is connected across the secondary coil can be found as

$$C_{C2} = \frac{1}{w^2 L_{sec}} \tag{76}$$

Besides the secondary side compensation capacitor, the primary side needs a compensator for the inductance of both the primary coil and the mutual inductance that is created by the secondary coil on the primary. The simplified equation for primary side compensation capacitor C_{C1} that is connected across the primary coil is given in paper [4] as below.

$$C_{C1} = \frac{1}{w^2 (L_{prim} - \frac{M^2}{L_{sec}})} \tag{77}$$

Eventually, we have the equations (70), (71), (72), (75), (76), and (77) to build a class-DE dc-ac high efficiency converter. In the next chapter, the circuit component values will be determined by using these formulas and a Simulink file will be created.

Inductive Coupling of Two Planar Coils

This part of the project is studied by Ethan Zimany as his master's degree thesis project. To give some perspective and knowledge about the planar coils' design, a brief design method and resultant product will be discussed in this section.

The very first requirement of designing two planar coils was to achieve 16 turns ratio to obtain 10 V_{dc} at the output. The second obligation was to keep the coupling factor as high as 0.9 with the possible highest efficiency. The third one was to have significantly small resistive losses on the coils while operating under 30kHz.

Having 2mm gap was the smallest air gap we could have between the transmitter and receiver parts, so Ethan decided to keep the gap at 2mm to help increase the k. Having small gap didn't provide the needed minimum of $k = 0.9$ so he added 6 ferrite I-cores to increase the flux coupling, in other words, transferred magnetic fields to the secondary part. Also, having the ferrite cores reduced the dissipated heat loss on the coils by spreading the heat to the I-cores. Figure 2.7 is a screenshot of his coil designs in Ansys/Maxwell software.

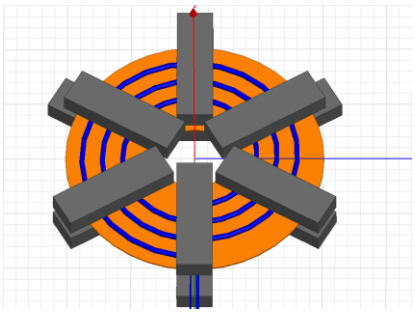

Figure 2.7: Screenshot of the Two Planar Coils' Design in Maxwell

CHAPTER III

MATLAB/SIMULINK SIMULATION

Simulation Settings

The Matlab/Simulink file is gathered together as in shown in figure 3.2. The component values of the $710V_{ac}$ to $10V_{ac}$ converter circuit that operates under constant and full load ($500W$) condition, in which the coil's non-physical step down turns ratio is $16/1$ and coupling factor k to be 0.9, can be found in table 3.1 using the equations (70), (71), (72), (75), (76), and (77) in chapter I. The Powergui block in Simulink file is set to discrete analysis and the $T_s = 5e-8\ s$. Here, to have an accurate system, it is important to have a sample time less than the switching frequency that is ${}^{1}/_{30e^3} = 3.33e-5s$.

PWM signal block is created using a triangle block, two constant blocks to set the threshold levels, and two comparators. By adjusting the top and bottom constant blocks' values to +0.5 and -0.5 respectively, and having a triangle wave between ± 1, we obtain two separate switch control waveforms with 25% ON and 75% OFF duty cycle. The Simulink schematic and the waveforms can be seen as in figure 3.1 and figure 3.2.

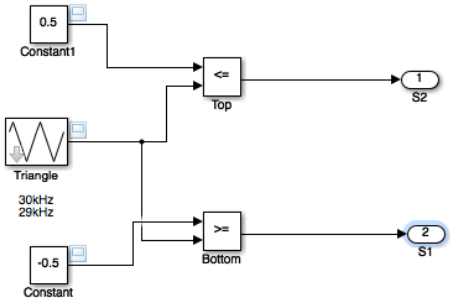

Figure 3.1: Inside PWM Block

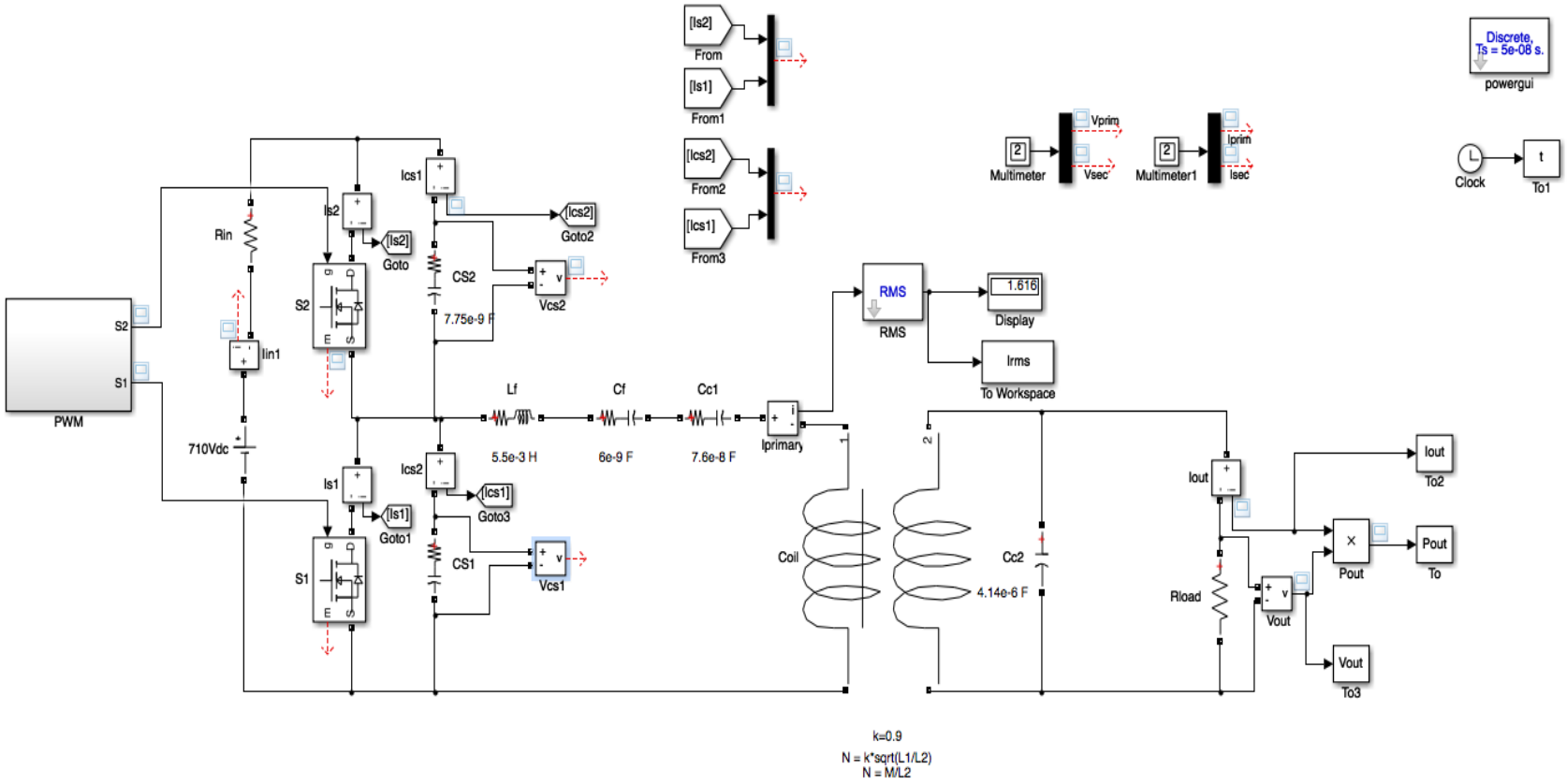

Figure 3.2: Matlab/Simulink Circuit of the Proposed Wireless Power System

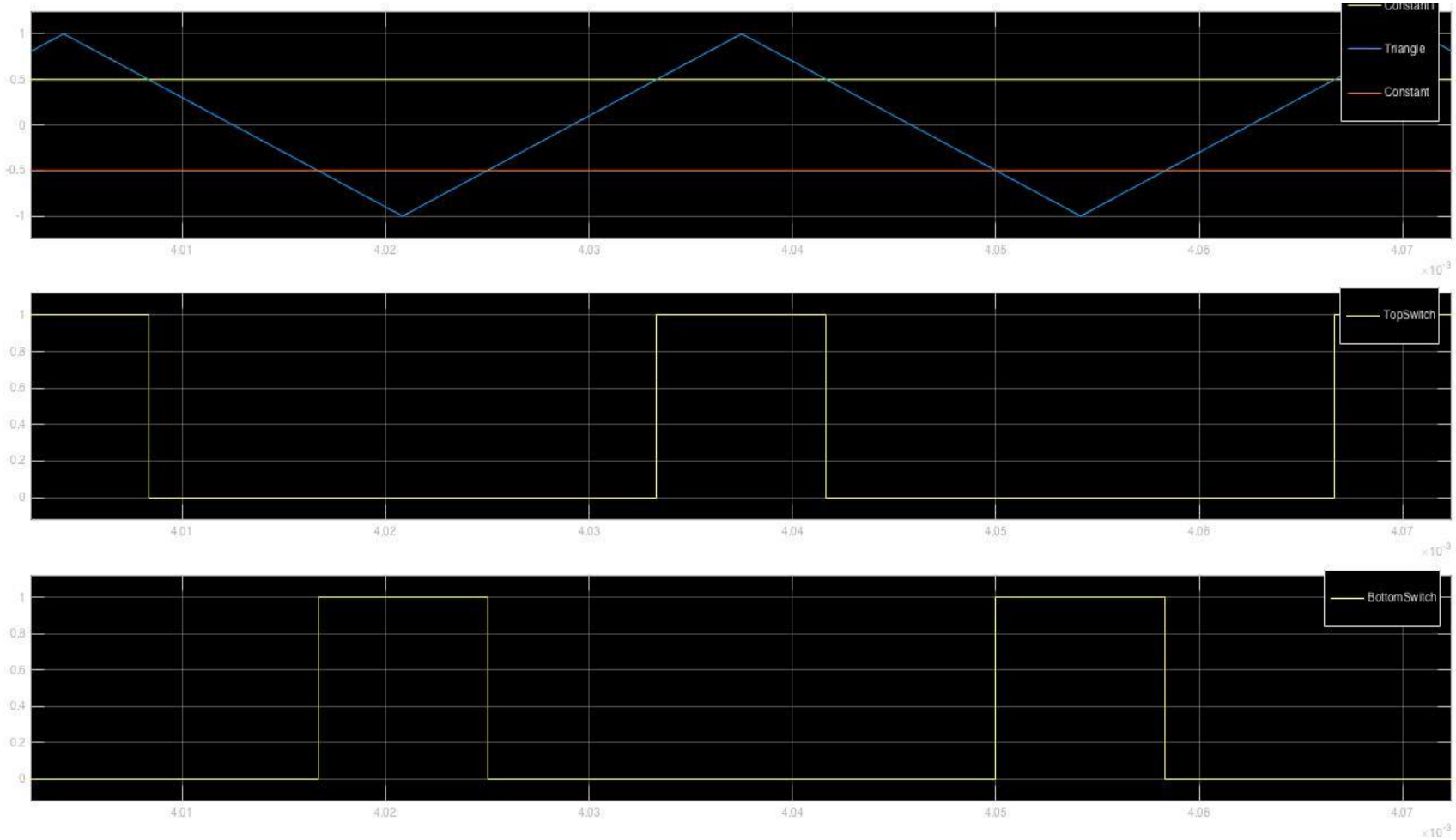

Figure 3.3: Two Transistor Driving PWM-Block Outputs Created Using Two Constant and a Triangle Wave

	Value	Series Resistance	Ron	Rdiode
Vin	710Vdc	NA	NA	NA
S1 & S2	NA	NA	0.12 ohms	0.01ohms
Cs1 & Cs2	15e-9 F	NA	NA	NA
Lf	2.88e-3 H	1.2 Ω	NA	NA
Cf	11.3e-9 F	1e-4 Ω	NA	NA
Cc1	7.6e-8 F	1e-3 Ω	NA	NA
LcoilPrim	2.1e-3 H	1.4 Ω	NA	NA
LcoilSec	6.8e-6 H	6.9e-3 Ω	NA	NA
Rload	0.2 Ω	NA	NA	NA

Table 3.1: Calculated Values of the Circuit Components

Simulation Results

Running the simulation, we obtain the ideal current and voltage waveforms of the switches, the coils, and the output that are expected to occur as depicted in chapter I figure 2.3. To start with the analysis of the top switch S_1, we see that during the yellow PWM signal that decides the ON/OFF situation of S_1, the voltage across S_1 and its shunt capacitor C_{S1} has the input voltage magnitude as their voltage level as in figures 3.4 and 3.5 The amount of current that flows from either switch is equal to the amount of current flowing to the output as that is the only path that the current circulates on the primary side. However, if we look at the shunt capacitors' current value, it also can be understood from the Kirchhoff's Current Law, the summation of the currents $i_{Cs1}(\theta)$ and $i_{Cs2}(\theta)$ that are flowing from the shunt capacitors C_{S1} and C_{S2} to the middle point will be equal to the output current $i_{out}(\theta)$.

The class-E ZVS and ZVDS conditions are fully satisfied. It can be seen as the switch voltages hit $0V$ right before the next ON cycle of the other switch, as well as when the switches are ON, the voltage levels stay constant resulting in zero derivatives. Having class-E switching

conditions improve the system's efficiency by refraining the switches from having shunt capacitor currents flowed through and resulted in power loss as heat dissipation. When we observe the two figures 3.4 and 3.5 we see that main difference appears in the current waveforms. While the switch current occurs during one interval, the shunt capacitor current occurs during two intervals as we showed in equations (51) through (54).

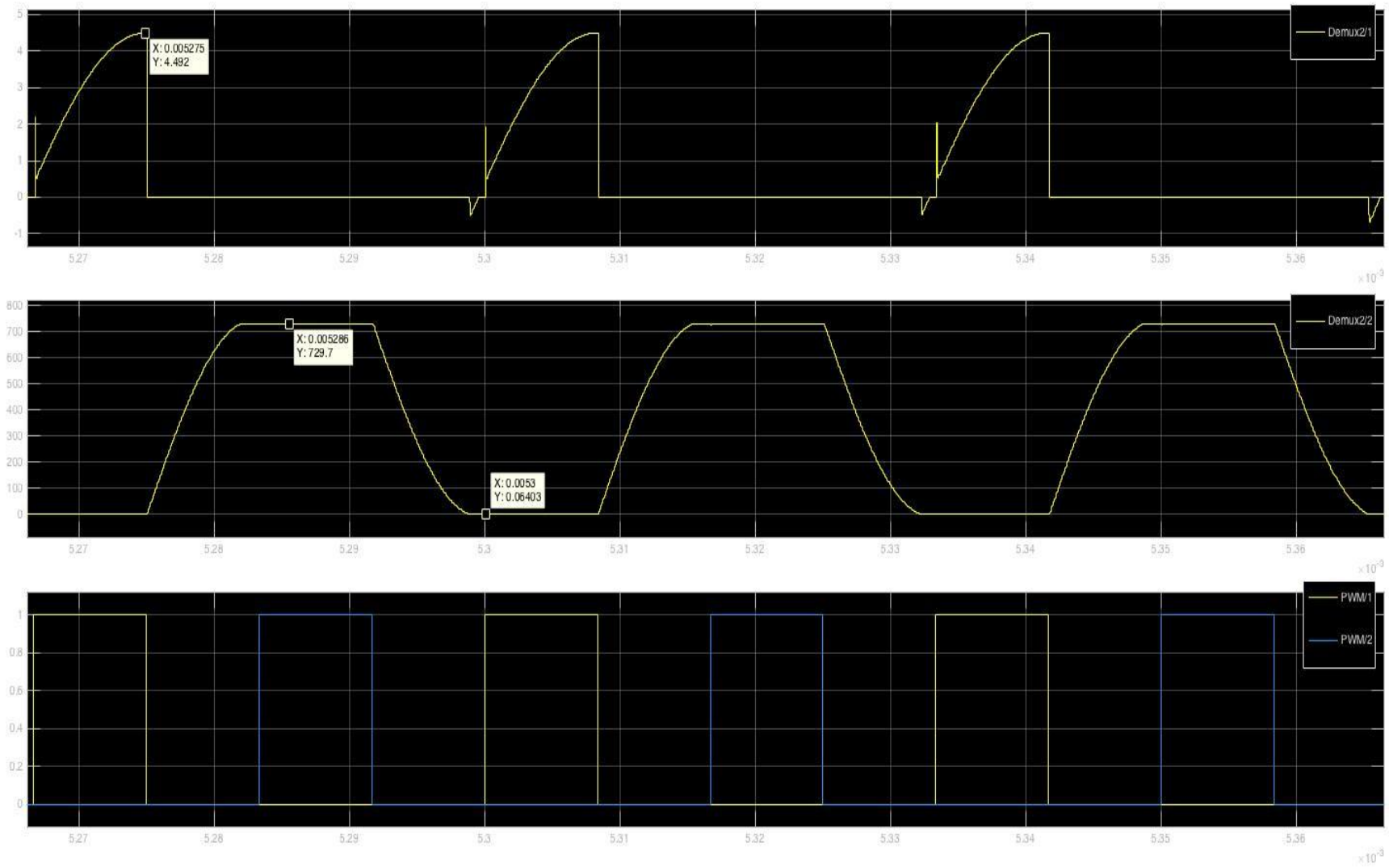

Figure 3.4: Current, Voltage, PWM vs. Time (top to bottom) Waveforms of the Top Switch S_2 for Full Load Design

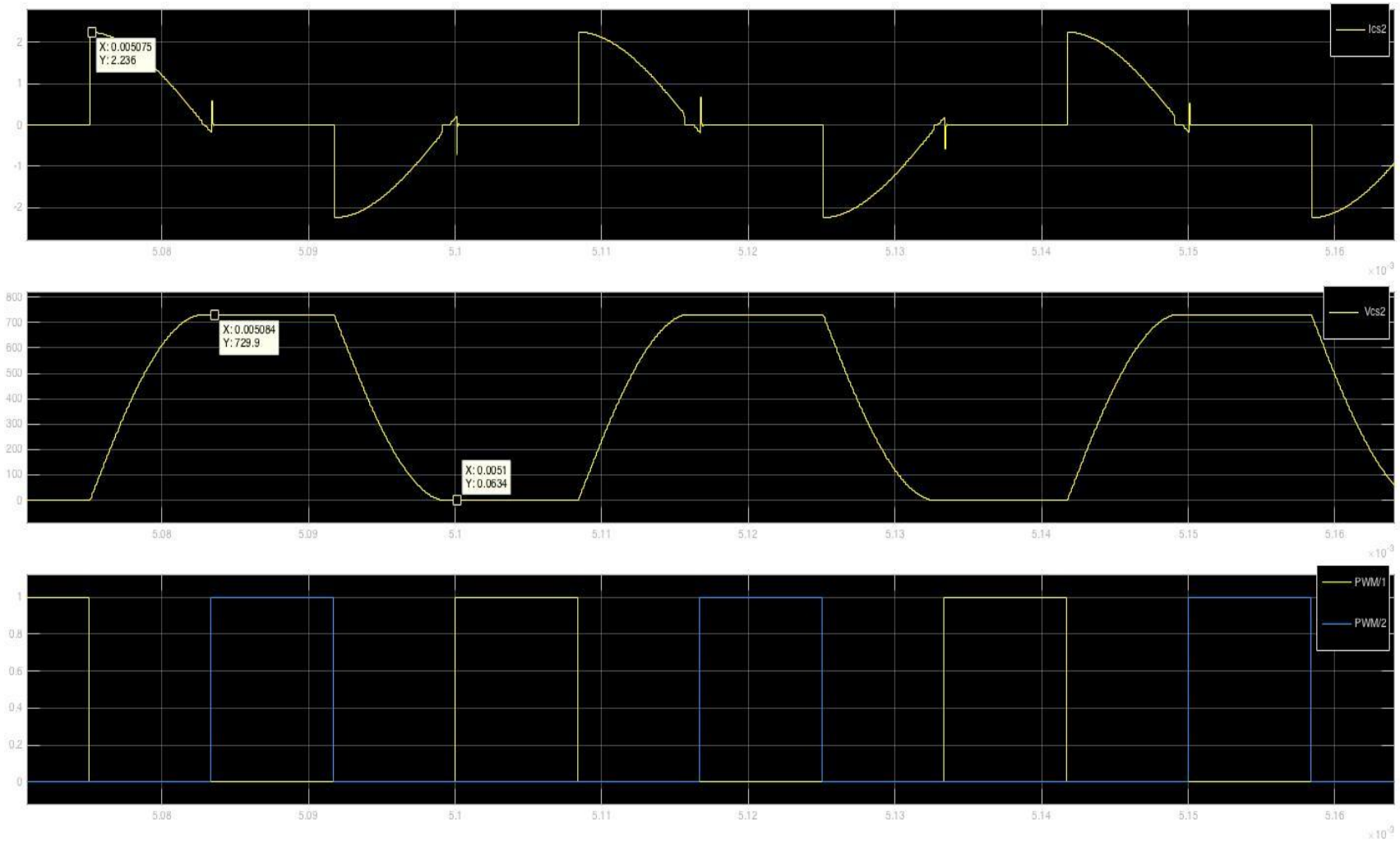

Figure 3.5: Current, Voltage, PWM vs. Time (top to bottom) Waveforms of the Top Shunt Capacitor C_{S2} for Full Load Design

In figure 3.6, current and voltage waveforms of the primary and secondary coils can be found. The primary coil and secondary coil have peak currents of $+4.49A$ and $-72A$ respectively. The reason of polarity is because of the induced current's flow direction. The ratio between these two values is proportional with the turns ratio of the coil $N = 16$. On the other hand, the primary coil voltage has a peak of $389V$ where the secondary coil voltage has a peak of $14.25V$. The system doesn't sustain the turns ratio proportion in here. The reason is that the coils don't have a perfect coupling of 1 but it is 0.9. As the coils don't have an iron core, in this case it is air insulation, the missing 0.1 coupling results in loss of voltage. In other words, when my classmate Ethan Zimany has designed the coils to have a turns ratio of 16, he designed so that the currents are proportional with the turns ratio of 16 with a 2mm gap in between the coils.

The output power, voltage, and current waveforms can be seen in figure 3.7. In this figure, the output power is calculated simply by multiplying the current and voltage signals. Therefore, it is important to note that the signal magnitude will be the double of the actual power level. In other words, if we look at the figure 3.7, the peak of the power is about $1000W$ which will represent $500W$ in actual scenario.

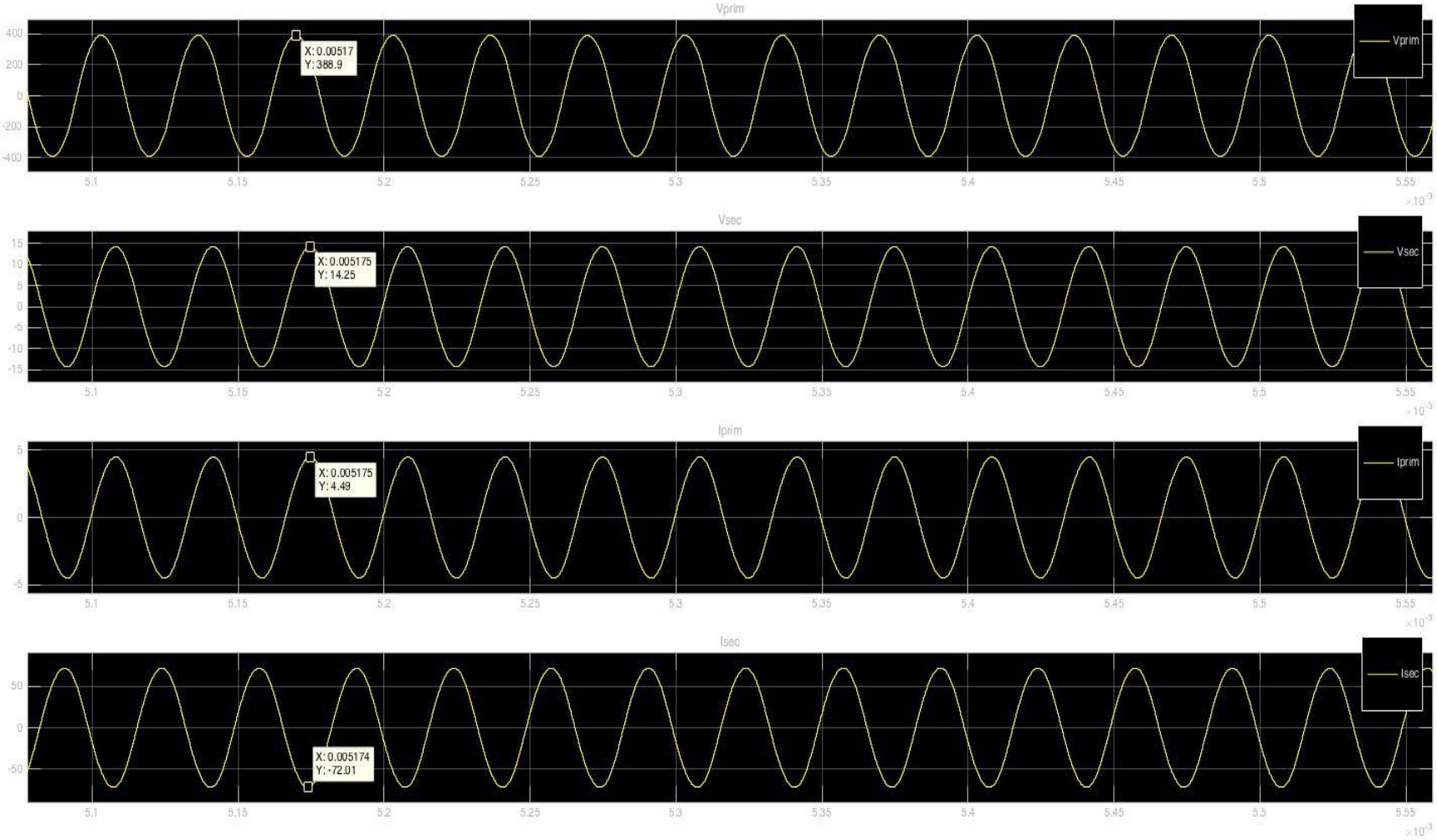

Figure 3.6: Primary Coil Voltage, Secondary Coil Voltage, Primary Coil Current, Secondary Coil Current (top to bottom) vs. Time Wave Forms for Full Load Design

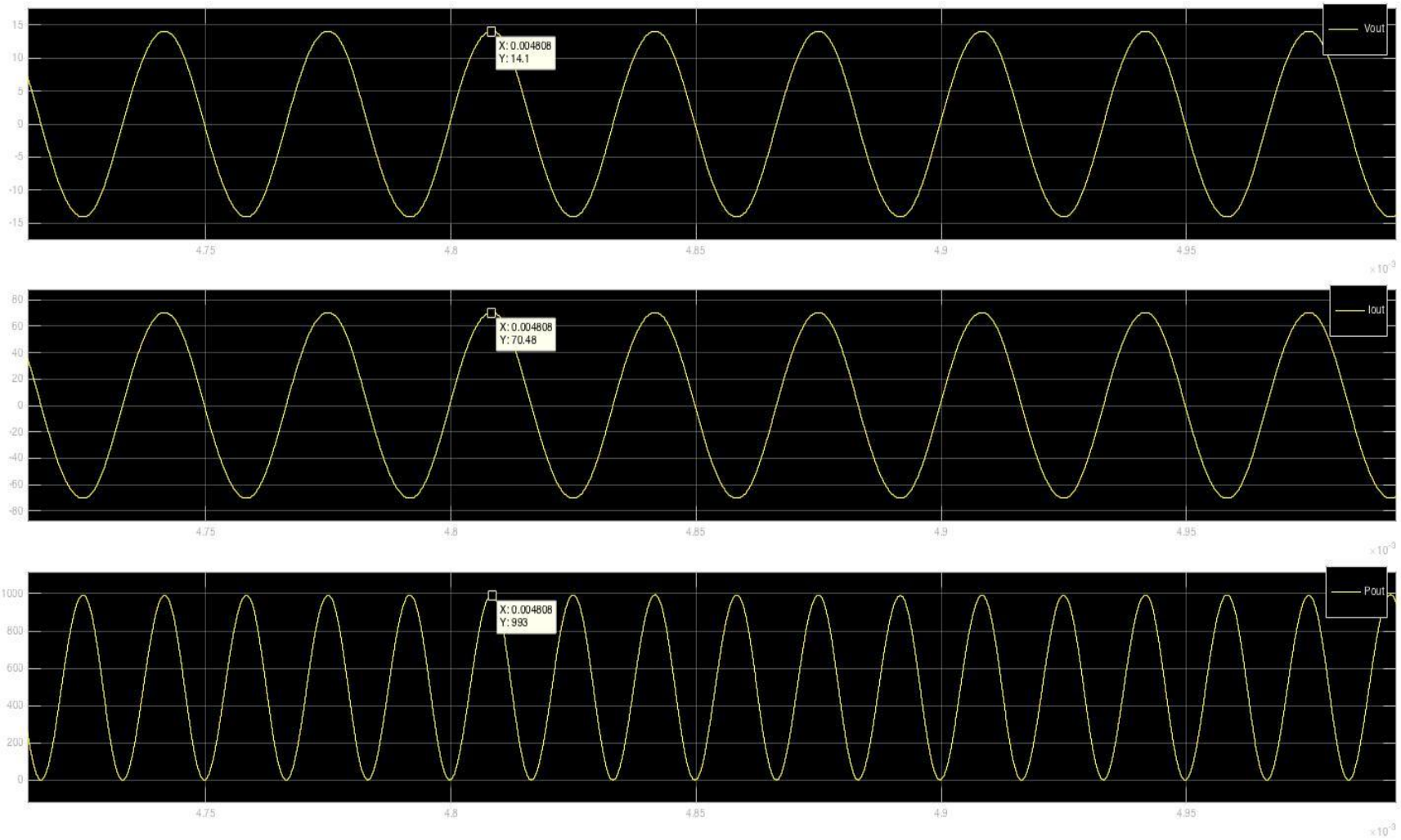

Figure 3.7: Voltage, Current, and Power (top to bottom) vs. Time Waveforms of the Load for Full Load Design

Efficiency Calculations

Efficiency of the system would be 100% if everything were ideal. However, to measure the practicality of a system we need to take a look at the efficiency calculations. To be able to consider system non-ideal, the circuit components will require series resistances added to them. For this purpose, close to real life values of the components were looked up online to get their potential series resistance values. For the switches, Mosfet PG-TO247 was taken reference.

For the effective efficiency calculation of the overall system, scholars have published papers and there are couples of different methods. In the following part, two methods will be described and formulized. In this study, method 1 will be taken into consideration for the efficiency computations.

Method 1: Loss Calculation via Resistive Losses

In this method, we assume that the only power loss will be occurring because of the heat on resistances of the circuit components and nothing else would contemplate it [3]. The power that will be lost on the switch resistances is based on the integration of power dissipation for the duration of an interval in which the switch is in conduction mode.

$$P_{S1} = P_{S2} = \frac{R_{S1}}{2\pi}\int_0^{\pi/2} I_{out}^2 sin^2\theta \, d\theta = \frac{R_{S1}}{8} I_{out}^2 \tag{78}$$

The power loss on shunt capacitors will be ideal and that is calculated in two conducting intervals as

$$P_{CS1} = P_{CS2} = \frac{R_{CS1}}{2\pi}\int_0^{2\pi} i_{CS1}^2(\theta)\, d\theta =$$

$$= \frac{R_{CS1}}{2\pi}\left\{\int_{\pi/2}^{\pi} \frac{I_{out}^2}{4} sin^2(\theta) d\theta + \int_{3\pi/2}^{2\pi} \frac{I_{out}^2}{4} sin^2(\theta) d\theta\right\} = \frac{R_{CS1}}{16} I_{out}^2 \tag{79}$$

The rest of the circuit components' power losses are simply calculated as follows

$$P_{L_f} = \frac{R_{L_f}}{2\pi}\int_0^{2\pi} I_{out}^2 sin^2\theta \, d\theta = \frac{R_{L_f}}{2} I_{out}^2 \tag{80}$$

$$P_{C_f} = \frac{R_{C_f}}{2\pi}\int_0^{2\pi} I_{out}^2 sin^2\theta\, d\theta = \frac{R_{C_f}}{2} I_{out}^2 \quad (81)$$

$$P_{CC1} = \frac{R_{CC_1}}{2\pi}\int_0^{2\pi} I_{out}^2 sin^2\theta\, d\theta = \frac{R_{CC_1}}{2} I_{out}^2 \quad (82)$$

$$P_{L_{prim}} = \frac{R_{L_{prim}}}{2\pi}\int_0^{2\pi} I_{out}^2 sin^2\theta\, d\theta = \frac{R_{L_{prim}}}{2} I_{out}^2 \quad (83)$$

$$P_{L_{sec}} = \frac{R_{L_{sec}}}{2\pi}\int_0^{2\pi} (16I_{out})^2 sin^2\theta\, d\theta = 128R_{L_{sec}} I_{out}^2 \quad (84)$$

Therefore the total dissipated power can be found as the summation of all

$$P_{diss} = I_{out}^2\left(\frac{R_{S_1}}{8} + \frac{R_{S_2}}{8} + \frac{R_{CS_1}}{16} + \frac{R_{CS_2}}{8} + \frac{R_{L_f}}{2} + \frac{R_{C_f}}{2} + \frac{R_{CC_1}}{2} + \frac{R_{L_{prim}}}{2} + 128R_{L_{sec}}\right) \quad (85)$$

Using equation (57) in (28), and (71) the dissipated power can be calculated. Afterwards, the efficiency would be

$$\eta = \frac{P_{out}}{P_{out}+P_{diss}} \quad (86)$$

In order to calculate the efficiency by using this method, a Matlab script is written as

```
%open up the .mdl file first
%change the load manually in the .mdl file itself
%resistance values can be changed below based on real series resistance values

Rs1=0.12;Rcs=1e-5;Rlf=1.2;Rcf=1e-4;Rcc=1e-3;Rprim=1.4;Rsec=6.9e-3;

%calculate the system efficiency by
%setting up the freq below in "set_param" command
%changing freq will regulate the output voltage

set_param('FCwoRec30/PWM/Triangle','Freq','30e3')
sim('FCwoRec30')

Pdiss = ([max(Irms)*sqrt(2)]^2)*[(Rs1/4)+(Rcs/8)+(Rlf/2)+(Rcf/2)+(Rcc/2)+(Rprim/2)+
(Rsec*128)];

Pout=max(Vout)*max(Iout);
n=100*Pout/(Pout+Pdiss)
```

Table 3.2: Efficiency Calculations for Matlab

Method 2: Input Power vs. Output Power

This method is based on the average input power and the measured output power [5]. To calculate the average input power P_{input}, average input current is needed at first place. The average input current would be equal to the average summation of two upper branches' currents that are flowing through the switch S_2 and the capacitor C_{S2} that is parallel to the switch.

$$I_{in,ave} = \frac{1}{2\pi}\int_0^{2\pi}\{i_{S2}(\theta) + i_{CS2}(\theta)\}d\theta =$$

$$= \frac{1}{2\pi}\int_0^{2\pi}\left\{\frac{v_{S2}(\theta)}{R_{S2}} + wC_{S1}\frac{dv_{S2}(\theta)}{d\theta}\right\}d\theta \quad (87)$$

In order to observe the integration above easily, we can divide the integral to be the first part and the second part as (87a) and (87b).

$$\frac{1}{2\pi}\int_{\pi}^{3\pi/2}\left\{\frac{v_{S2}(\theta)}{R_{S2}}\right\}d\theta \quad (87a)$$

$$\frac{1}{2\pi}\int_0^{2\pi}\left\{wC_{S1}\frac{dv_{S2}(\theta)}{d\theta}\right\}d\theta \quad (87b)$$

Figure 3.8 can be analyzed for each interval. Voltage plot of S_2 and the derivative of it can be drawn using equation (50). For the easiness of the calculation, we believe that trapezoidal rule of the integration would be a good fit. As the switch resistance will be non-zero during interval 3 and infinite in the rest of a period, equation (87a) will be calculated only for interval 3. Likewise, interval 3 of the derivative plot can be explained by equations (88) and (89). Eventually, with the average input current we will have, the efficiency of the system can be calculated as in equation (90).

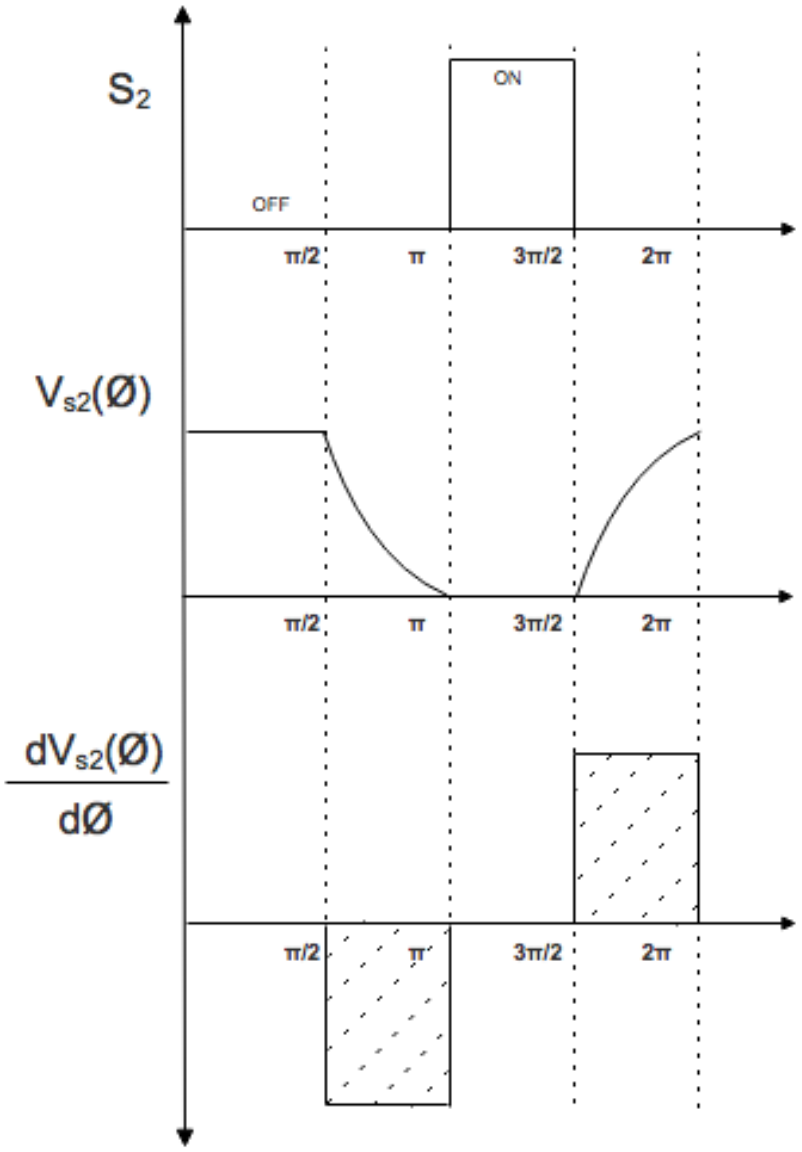

Figure 3.8: PWM Signal, Voltage, Voltage Derivative (top to bottom) vs. Theta of Top Switch

$$v_{cap}(t) = V - Ve^{-\frac{t}{RC}} \tag{88}$$

$$\frac{dv_{cap}(t)}{dt} = \frac{V}{RC}e^{-\frac{t}{RC}} \tag{89}$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2}{R_{load}V_{in}I_{in,ave}} \tag{90}$$

CHAPTER IV

VARYING LOAD CONDITION ANALYSIS FOR REAL LIFE CASES

For a real life system to be practical and adaptive to load changes, it is important to notice the possible deficiencies of the system that may result because of the load variations. Basically, the load variation is the change in the drawn power from the system, which can be simulated by playing with the resistive load at the output. In this design project, one of the requirements is to have a safe operation mode while working under both half load and full load conditions. Ideally, the worst-case scenario of this project, the half load condition, would be $250W$ that is provided with $0.4\ \Omega$ load resistance whereas the full load would be $500W$ with $0.2\ \Omega$ load resistance.

Varying load test is highly needed for a system like this where the circuit components will change or be affected negatively based on required current and voltage amounts. For example, voltage stress on a component will change the power dissipation as heat loss, or a shunt capacitor charge will be much higher or much less than the required power level to supply the circuit. To observe the advantages and disadvantages of a circuit with non-variable components, the following part will scrutinize the two cases mentioned above.

Case 1: Circuit Designed for Full Load

In Chapter III, we have used the circuit components' values that are calculated for the full load condition. Knowing the followings,

- $P_{out} = 500W$ (a1)

- $w = 2\pi f$ where $f = 30 \times 10^3\ Hz$

(b)

- $Q = 10$ (c)
- $R_{sec,total} = R_{load} + R_{L_{sec}}$ (d)
- $R_{prim,total} = R_{L_f} + R_{C_f} + R_{CC1} + R_{L_{prim}}$ (e)
- $R = R_{prim,total} + N^2 R_{sec,total}$ (f)

Assuming $710V$ of input voltage source in equation (70), and only analyzing the transmitter side of the circuit

$$R_{needed} = \frac{V_{in}^2}{2\pi^2 P} = \frac{710^2}{2\pi^2 500} = 51\ \Omega$$

At the receiver side's output, $10V$ with $500W$ is obtained with the resistance of

$$R_{load} = \frac{V_{out}^2}{P_{out}} = \frac{10^2}{500} = 0.2\ \Omega$$

So we need a step down turns ratio of about

$$N = \sqrt{\frac{R_{needed}}{R_{load}}} \approx 16$$

After careful design of the planar coils with a 16 step down turns ratio, transmitter and receiver coils have the values of of

$$L_{sec} = 6.8e^{-6}\ H$$

$$L_{prim} = 2.1e^{-3}\ H$$

$$R_{L_{sec}} = 6.9\ e^{-3}\Omega$$

$$R_{L_{prim}} = 1.4\ \Omega$$

So from this point on, we will have to consider these resistances as well while calculating the component values. Placing known parameters in equation (d)

$$R_{sec,total} = R_{load} + R_{L_{sec}} = 0.2 + 6.9\, e^{-3} = 0.2069\, \Omega$$

Using equation (70) again, but this time for shunt capacitors

$$C_{S1} = C_{S2} = \frac{1}{2\pi w R_{needed}} = \frac{1}{2\pi 2\pi f 51} = 16.5e^{-9}\, F$$

Using equation (73) and so far known resistance values we can find L_r as below. It should be noted that, in the overall calculations, we would still need the resistance of L_f, C_f, C_{CC1}, C_{CC2}.

$$L_f = Q\frac{R}{w} = Q\frac{(N^2 R_{sec,total} + R_{L_{prim}})}{w} \approx 10\frac{54.36}{2\pi 30000} \approx 2.88e^{-3}\, H$$

Finding an inductor working under 30kHZ with $2.8e^{-3}\, H$ gives us

$$R_{L_f} = 1.2\, \Omega$$

Assuming C_f and C_{CC1} to have series resistances of

$$R_{C_f} = 1e^{-4}\, \Omega$$

$$R_{CC1} = 1e^{-3}\, \Omega$$

Now, we can consider the series capacitor resistance R_{C_f} and series compensator capacitor resistance R_{CC1} added to the value as well and rolling the number up, the new total resistance will be approximately as below

$$R \approx 54.36 + 1.2 + R_{C_f} + R_{CC1} \approx 55.7\, \Omega$$

To find the series capacitor on the primary side we use equation (75)

$$C_f = \frac{1}{wR(Q - \frac{\pi}{2})} = \frac{1}{w53.8(10 - \frac{\pi}{2})} = 11.3e^{-9}\, F$$

To calculate the compensator capacitors that are added to match the coil inductances on both sides so the circuit is still in resonance we use equations (76) and (77)

$$C_{C2} = \frac{1}{w^2 L_{sec}} = \frac{1}{w^2 6.8e^{-6}} = 4.14e^{-6}\, F$$

$$C_{C1} = \frac{1}{w^2(L_{prim} - \frac{M^2}{L_{sec}})} = \frac{1}{w^2(2.1e^{-3} - \frac{(1.085e^{-4})^2}{6.8e^{-6}})} = 7.6e^{-8}\ F$$

Finally, it is vital to know that when we started calculating the $R_{prim,needed}$ at the very first place, we haven't considered the resistances of the circuit components. So, it is necessary to include all the components' resistance values in the equation below to find the final value of shunt capacitors for a better design.

$$C_{S1} = C_{S2} = \frac{1}{2\pi wR} = \frac{1}{2\pi 2\pi f 55.7} = 15.15e^{-9}\ F$$

Now, with the values we have in table 3.1, the system works safe and efficiently as discussed in previous chapter. However, we are still unaware at this point if a system designed with these values will still be a healthy system even at half load condition or at any other operating point between full load and half load. Calculated efficiency using the Matlab script presented in table 3.2 is 95.75%.

Case 2: Circuit Designed for Half Load

In this scenario, we are trying to build a circuit for the worst condition that we expect to have for this wireless power system. Having the same conditions and parameters as in full load design except the output power that is

- $P_{out} = 250W$ (a2)

And using the same planar coil designs with exact same values, we can now compute each and every component value by following the same methodology as followed below.

$$R'_{needed} = \frac{V_{in}^2}{2\pi^2 P} = \frac{710^2}{2\pi^2 250} = 102\ \Omega$$

Also, secondary side should be simulated with the resistance value below in order to have $10V$ with $250W$ power

$$R'_{load} = \frac{V_{out}^2}{P_{out}} = \frac{10^2}{250} = 0.4\ \Omega$$

New scenario's step down ratio stays the same, which will allow us to utilize the same planar coil designs with the values provided before.

$$N = \sqrt{\frac{R'_{needed}}{R'_{load}}} \approx 16$$

$$R'_{sec,total} = R'_{load} + R_{L_{sec}} = 0.4 + 6.9\ e^{-3} = 0.4069\ \Omega$$

Knowing these three parameters

$$R_{L_f} = 1.2\ \Omega$$

$$R_{C_f} = 1e^{-4}\ \Omega$$

$$R_{CC1} = 1e^{-3}\ \Omega$$

For more effective calculations circuit total resistance will be

$$R' \approx 104.1 + R_{L_{prim}} + R_{L_f} + R_{C_f} + R_{CC1} \approx 106.9\ \Omega$$

Series inductor

$$L'_f = Q\frac{(R' - R_{L_f})}{w} \approx 10\frac{105.7}{2\pi 30000} \approx 5.6e^{-3}\ H$$

The inductor that we could find on the market that is close to the value above and working efficiently under 30kHz was $5.5e^{-3}\ H$. In order to reach this value, we need to decrease the quality factor from 10 to 9.8. Using this new quality factor $Q' = 9.8$

Series capacitor

$$C'_f = \frac{1}{wR'(Q' - \frac{\pi}{2})} = \frac{1}{w106.9(9.8 - \frac{\pi}{2})} = 6e^{-9}\ F$$

Because the coils' values haven't changed, the compensating capacitors won't change either.

Shunt capacitors

$$C'_{S1} = C'_{S2} = \frac{1}{2\pi w R'} = \frac{1}{2\pi 2\pi f 106.9} = 7.9e^{-9}\ F$$

So a new parameter table can be gathered up for half load condition as seen in table 4.1.

	Value	**Series Resistance**	**Ron**	**Rdiode**
$\mathbf{V'_{in}}$	710Vdc	NA	NA	NA
S1 & S2	NA	NA	0.12 ohms	0.01ohms
$\mathbf{C'_{S1}}$ & $\mathbf{C'_{S2}}$	7.9e-9 F	NA	NA	NA
$\mathbf{L'_f}$	5.5e-3 H	1.2 Ω	NA	NA
$\mathbf{C'_f}$	6e-9 F	1e-4 Ω	NA	NA
Cc1	7.6e-8 F	1e-3 Ω	NA	NA
LcoilPrim	2.1e-3 H	1.4 Ω	NA	NA
LcoilSec	6.8e-6 H	6.9e-3 Ω	NA	NA
$\mathbf{R'_{load}}$	0.4 Ω	NA	NA	NA

Table 4.1: Calculated Values of the Circuit Components for New Design

After simulating the new design for half load condition, we see that the circuit applies ZVS and ZVDS conditions of class-E amplifier. In addition to this, we have the expected voltage and current waveforms as it is depicted in chapter II. Using Matlab efficiency calculation code as laid out before in table 3.2, the overall efficiency of the system appears to be 97.8%.

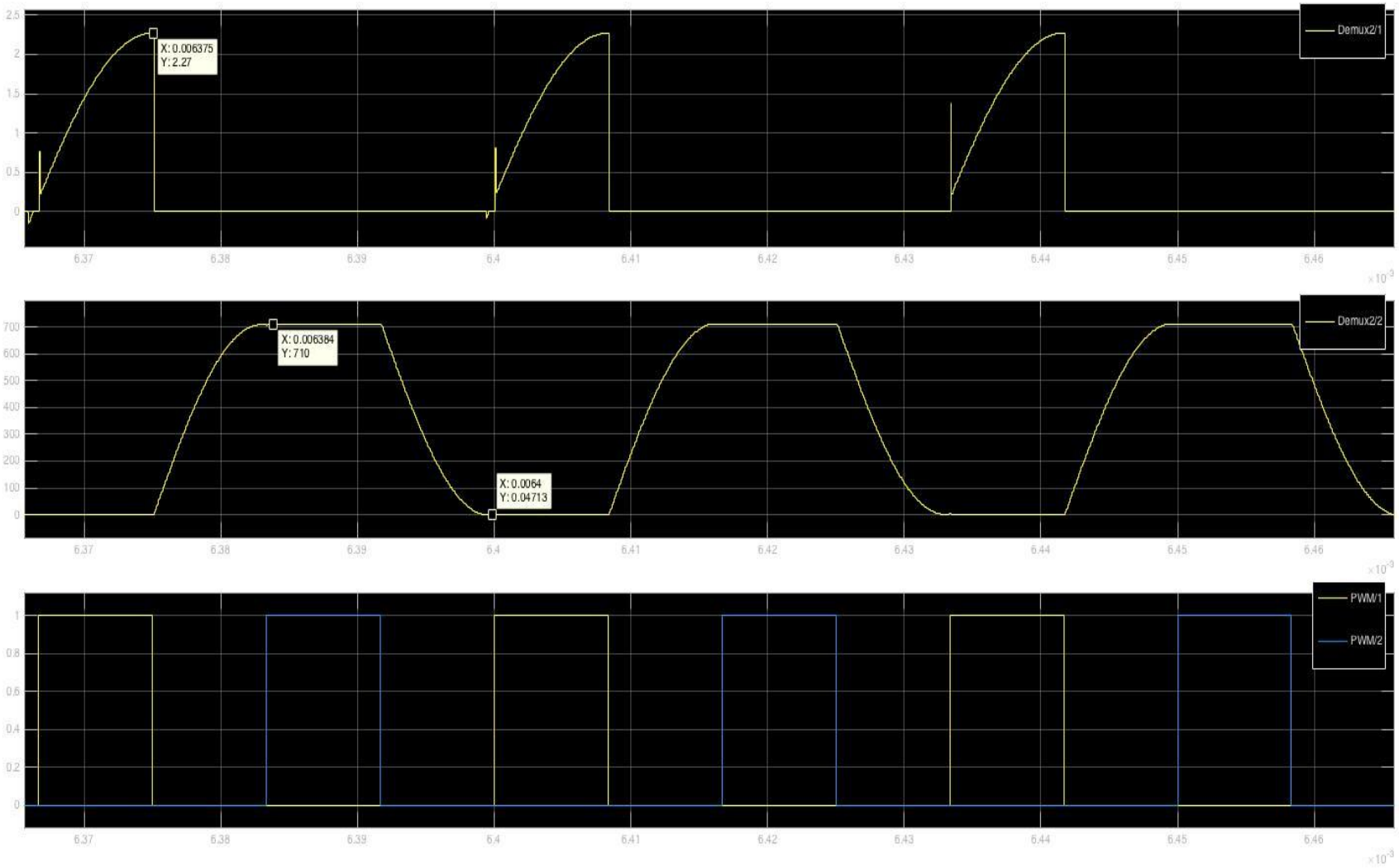

Figure 4.1: Current, Voltage, PWM vs. Time (top to bottom) Waveforms of the Top Switch S_2 for Half Load Design

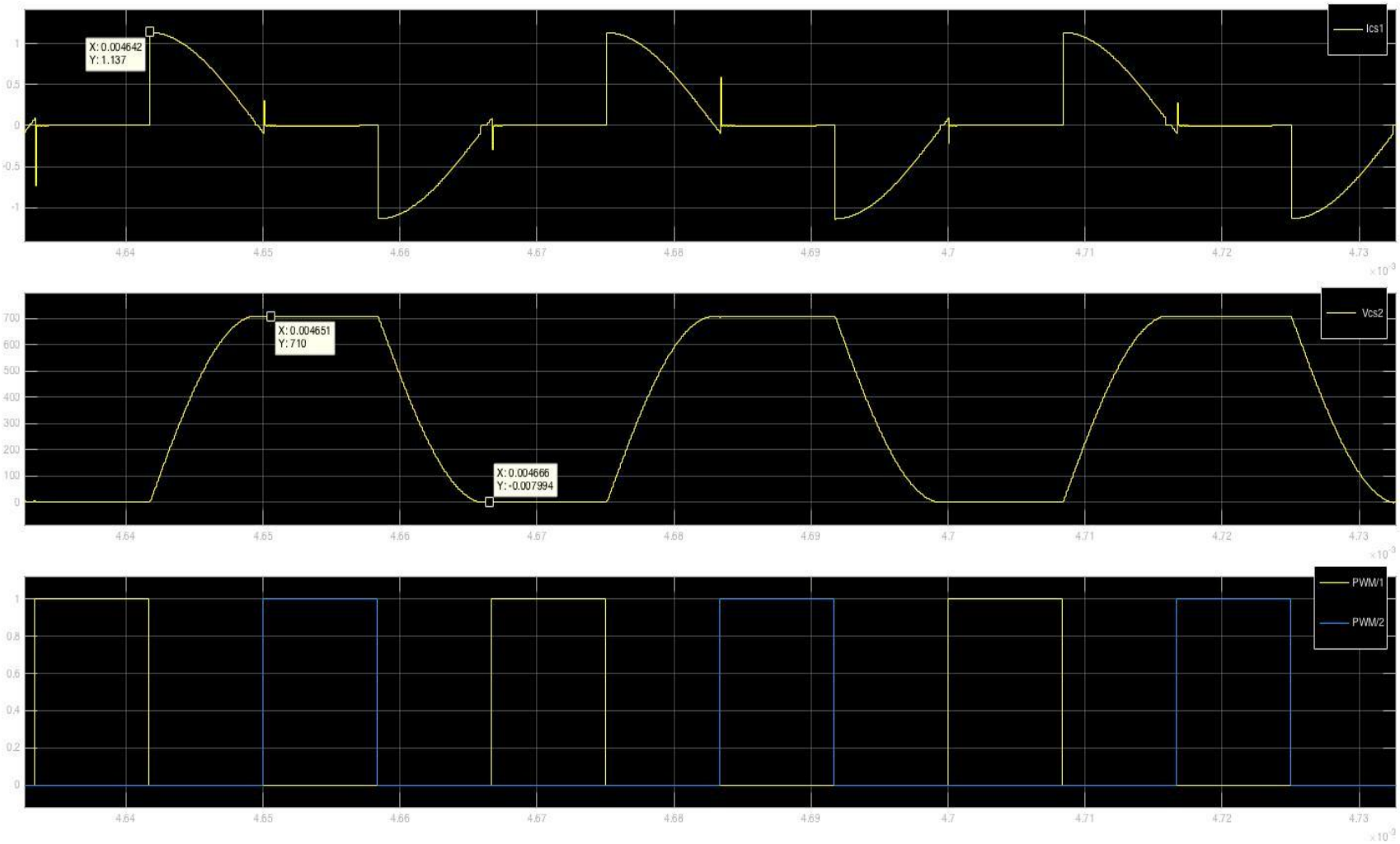

Figure 4.2: Current, Voltage, PWM vs. Time (top to bottom) Waveforms of the Top Shunt Capacitor C_{S2} for Half Load Design

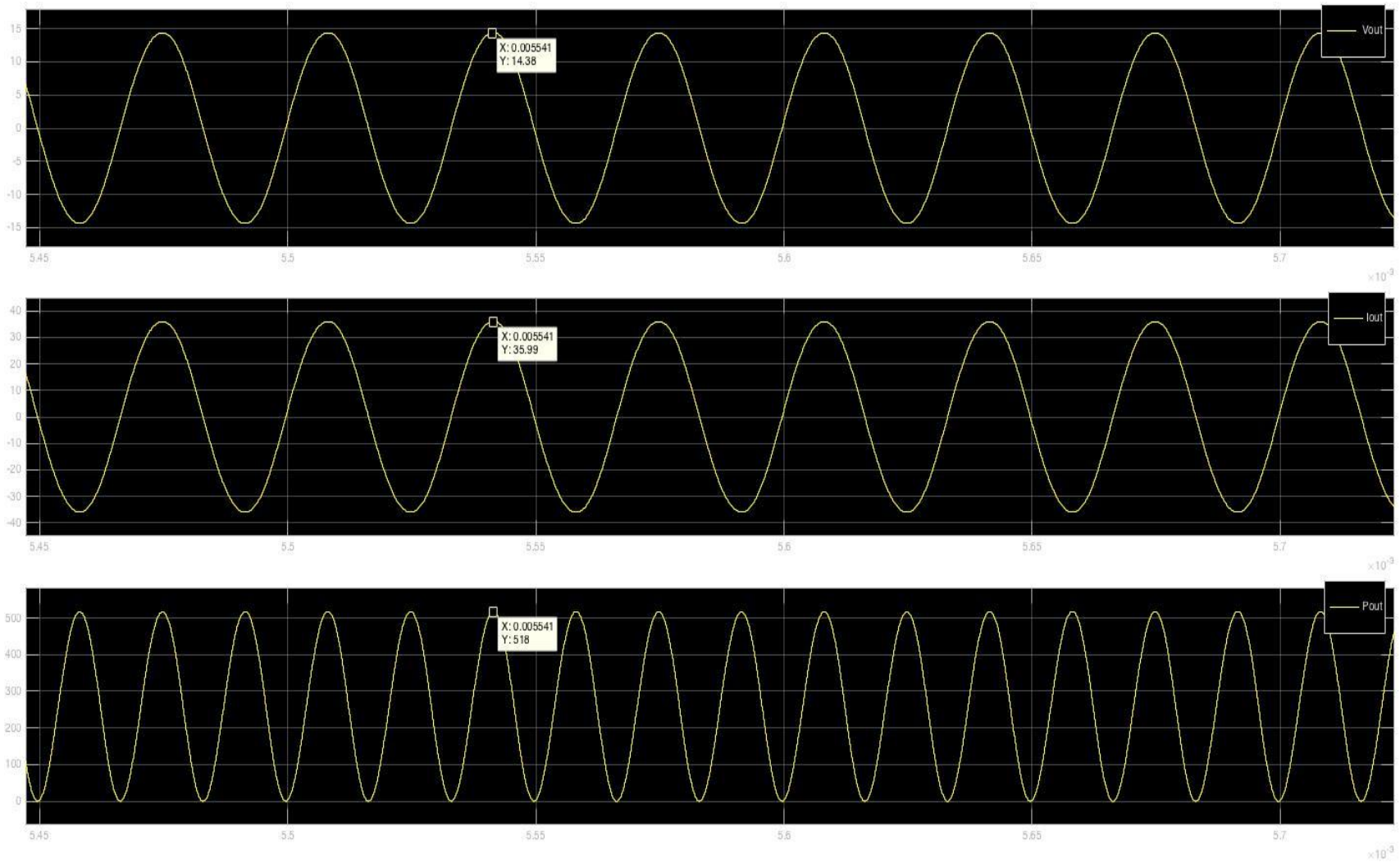

Figure 4.3: Voltage, Current, and Power (top to bottom) vs. Time Waveforms of the Load for Half Load Design

Comparison of the Two Designs

So far, we have seen the two distinct scenarios and their simulation results. We have proven that with the equations discussed in chapter II, it is possible to build a circuit of a class-DE power amplifier for a highly coupled wireless power transfer system. Both circuits have sustained the high efficiency application as well as ZVS and ZVDS conditions that are adopted from class-E type power amplifier.

The purpose of this section is to validate if any of these scenario-based designs would be a perfect fit for all conditions between full power and half power. To determine this, we will have to run the circuits for the loads that are not designed for. To be more specific, we will run the full load design with half load and the other way around, the half load design will be run for full load.

a. Full Load Circuit Run Under Half Load

To test this scenario we have to keep the circuit components values as found in Case 1, but only change the resistive load R_{load} from 0.2 Ω to 0.4 Ω so that half load operation is applied. However, running the simulation under these parameters causes high voltage and current levels, which in real case can burn up the load side device or even the whole system. To overcome this problem, switching frequency is changed to drop down the current and voltage levels. The explanation of frequency-change control method is a topic we would like to touch in the "Output Voltage Control" section, thus we will just provide the switching frequency that is selected to be 31.8kHz. Operating the circuit with this new switching frequency results in 14.2 V_{ac} peak value at the load side that will be equivalent of $\approx 10V_{dc}$.

Secondly, analyzing figure 4.5, we see that almost perfect sinusoidal voltage and current waveforms occur. Nonetheless, looking at figure 4.4, voltage waveform doesn't retain the ZVS

and ZVDS conditions anymore. The reason is that the amount of current drawn from the source is almost half of the full load case. So, choosing a shunt capacitor to supply the circuit during OFF cycles of the switches and using this same capacitor for a scenario requiring less current results in not fully charged capacitor when the complementary switch turns ON. Following that, the same logic, while this capacitor is discharging, it starts from source voltage level, and it cannot fully discharge itself because of the small amount of current drawn from the load. When the capacitor is not discharged all the way to zero but the switch that is shunted by it turns ON, the remaining charge is being rushed onto this switch. The amount of current seen in figure 4.4 is not something acceptable and practical because those peaks in the current will put too much stress on the switches.

It is believed that calculating efficiency of a system like this will be irrational because the high peak currents on the system components will eventually result in faults and failures.

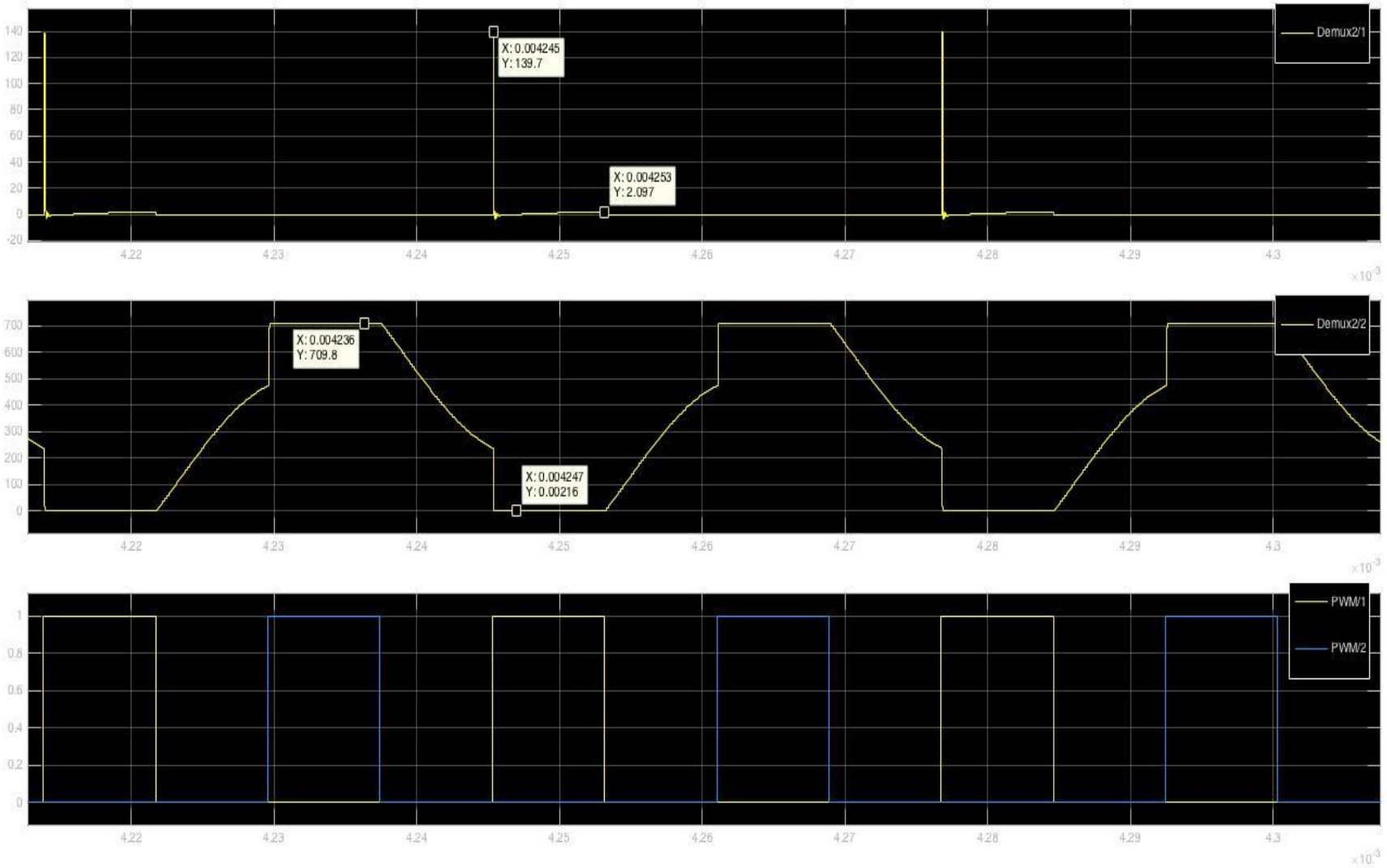

Figure 4.4: Current, Voltage, and PWM (top to bottom) vs. Time Waveforms of the Top Switch S_2 for Full Load Design Run Under Half Load Condition

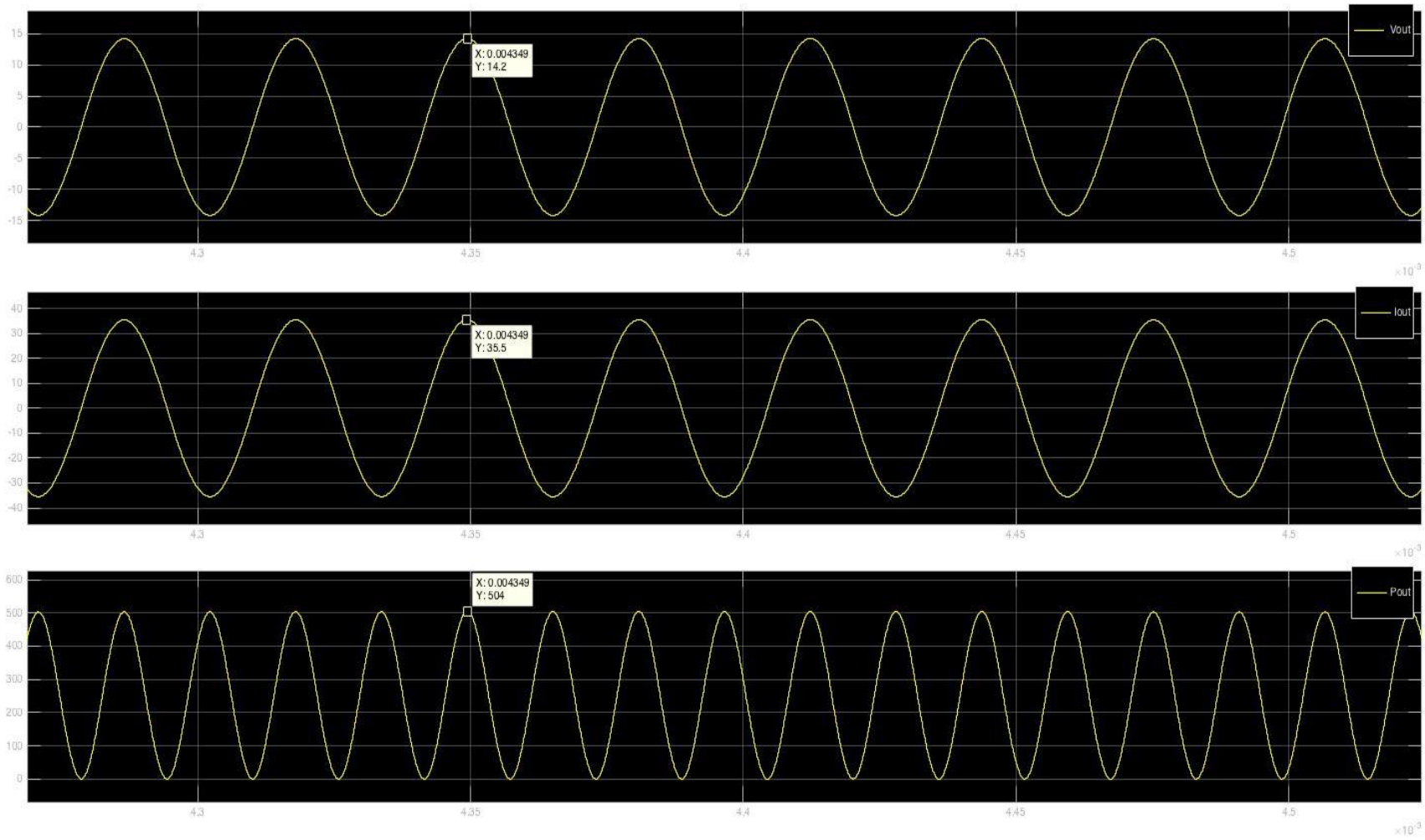

Figure 4.5: Voltage, Current, and Power (top to bottom) vs. Time Waveforms of the Output for Full Load Design Run Under Half Load Condition

b. Half Load Circuit Run Under Full Load

To simulate this scenario, we keep the circuit components at half load values but only change R_{load} from 0.4 Ω to 0.2 Ω so that the load requires $500W$. Before analyzing the top switch S_2 current and voltage waveforms, it is practical to take a glance to the output waveforms. Looking at figure 4.6, we realize the output voltage and current levels are a little less then expected resulting in less power provided to the load.

Also to understand the current flowing schemes concurrently with the current waveforms of the switches and shunted capacitors that were presented in chapter II in figure 2.3, we follow the current path diagrams as depicted in figure 4.8. In figure 4.8.a, the top switch is ON letting current flow from source to the primary coil. In the next cycle, both switches are OFF therefore shunt capacitors are supplying the circuit by discharging the energy they stored as seen in figure 4.8.b1. Because the capacitors were small and discharge faster than supposed timing, a dead time within this 25% cycle occurs between the moment when the capacitor voltage hits zero and the next 25% cycle kicks in. During this dead time, the current that is stored in the series inductor flows on the free willing diode of the bottom switch as in figure 4.8.b2. Following cycle is when the top switch is OFF and bottom switch is ON. The current flows from coil to the switch as seen in figure 4.8.c. In figure 4.8.d1, both switches are OFF and this is the last 25% cycle of a period. Current flows from primary coil side to the shunt capacitors. In opposite to previous case, this time these shunt capacitors reach to their maximum voltage level faster than expected resulting in a dead time again.

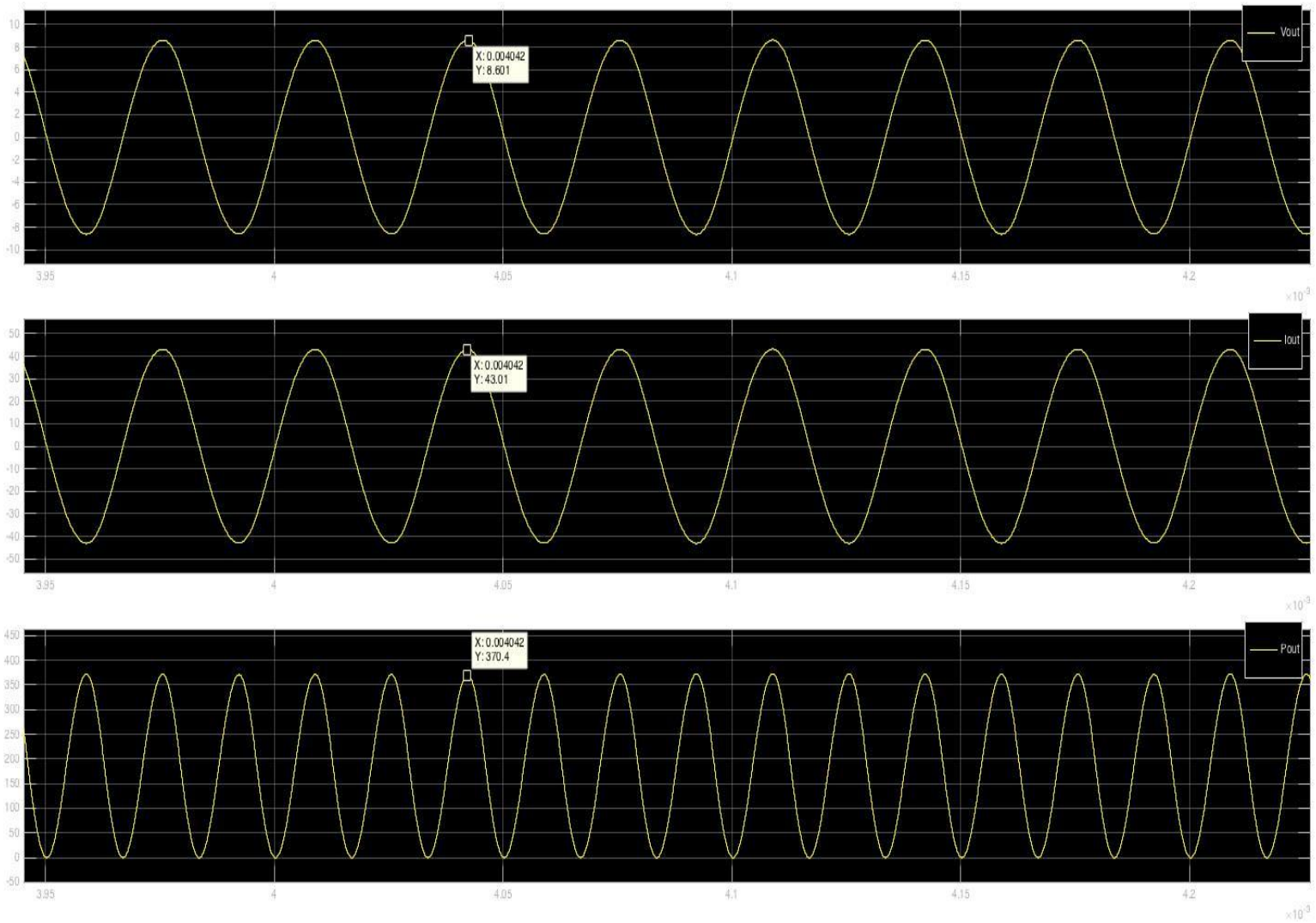

Figure 4.6: Voltage, Current, and Power (top to bottom) vs. Time Waveforms of the Output for Half Load Design Run Under Full Load Condition at 30kHz

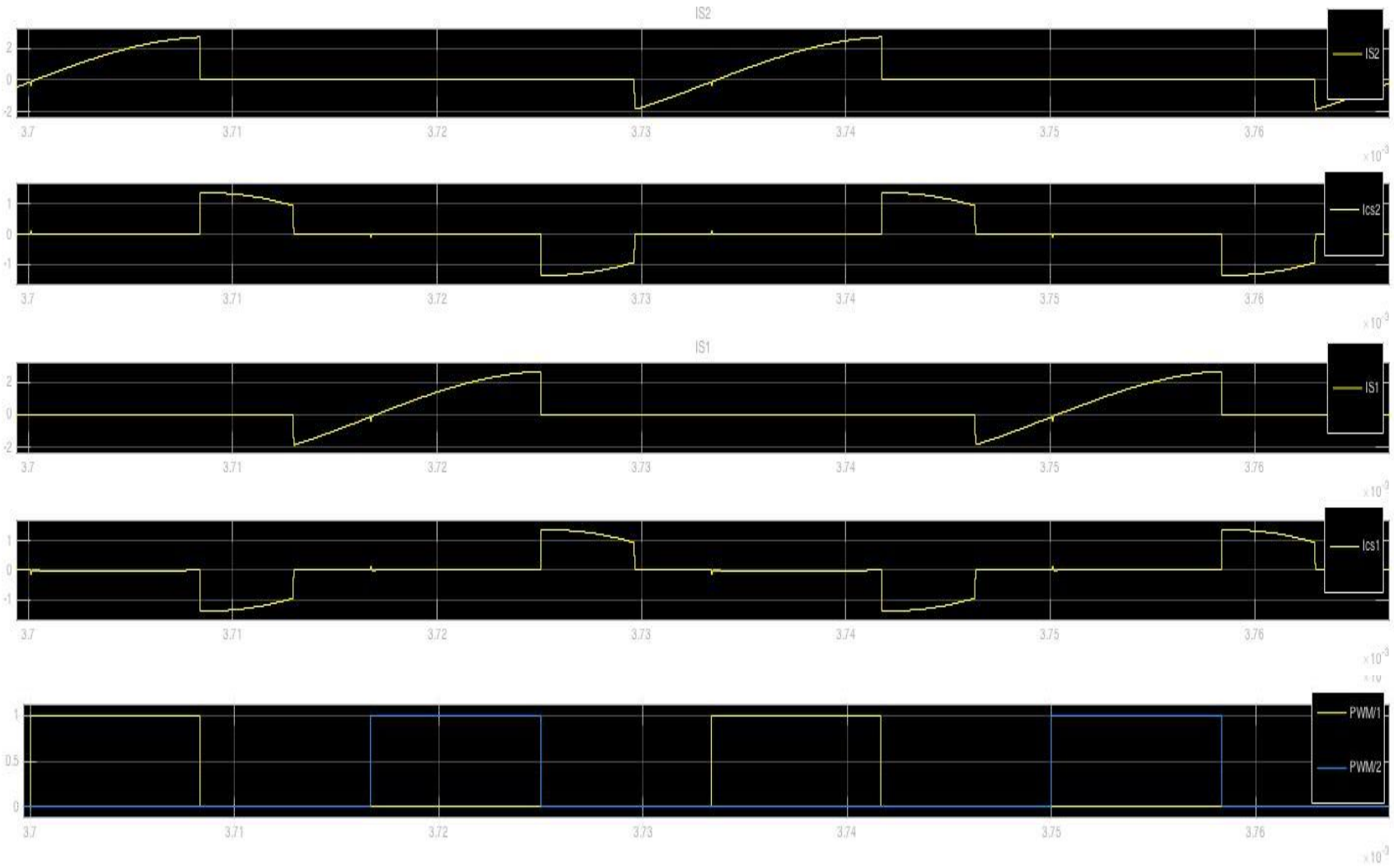

Figure 4.7: Top Switch, Top Shunt Capacitor, Bottom Switch, Bottom Shunt Capacitor Currents (top to bottom) vs. Time Waveforms for Half Load Design Run Under Full Load Condition at 30kHz

During this dead time, current follows the path through the free willing diode of the top switch as shown in figure 4.8.d2. It should be noted that, the efficiency calculations doesn't include the free willing diode resistances, hence these dead times assumed to have zero power losses on the switch diodes.

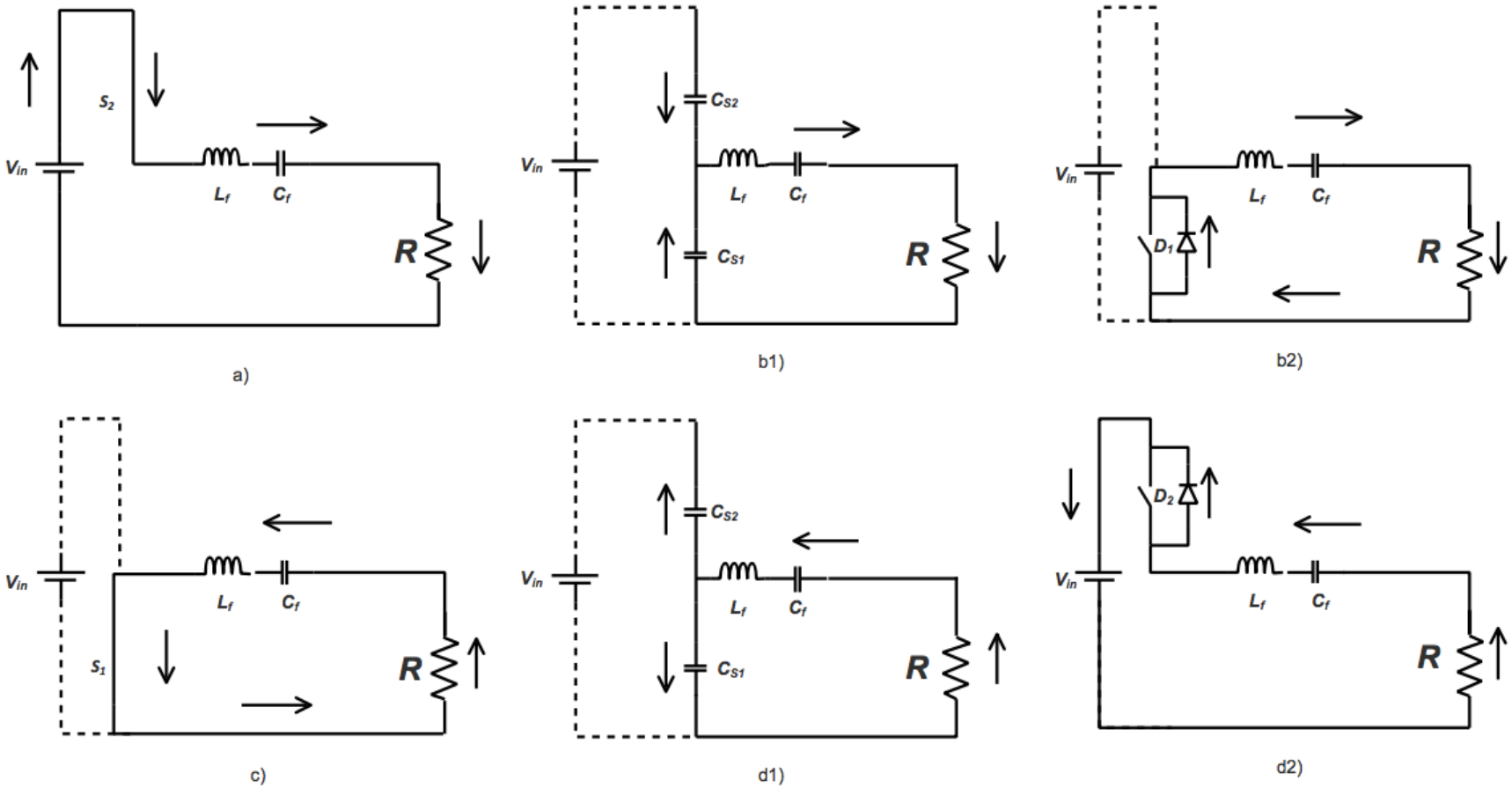

Figure 4.8: Current Flow Paths for Each Operation Cycle of Class-DE Power Amplifier

Output Voltage Control

In order to observe the effect of switching frequency at the output voltage, an algorithm is coded in Matlab to sweep the frequency as in table 4.2. By looking at figure 4.9, we come to the understanding of switching at a smaller f_s provides higher output voltage. So for this system designed for half power yet works in full power, and lost some of the voltage at the output, we can choose $f_s = 29kHz$. New switching frequency results in increase in the output voltage, which is observed from the simulation execution to be approximately $10V_{dc}$. Also analyzing figure 4.10, it is understood that varying frequency of the system will have no effect on the overall efficiency.

Unfortunately, when a frequency change is introduced to the system, some distortions on the voltage and current waveforms occur. The peak currents appearing as a result of frequency change will have a stress on the transistors. In addition to this, since the shunt capacitors reach to their max voltage level much earlier than they are supposed to, they start to discharge before the timing arrives. This results in current flow from shunt capacitors to the supply direction..

```
Rs1=0.12;Rcs=1e-5;Rlf=2;Rcf=1e-4;Rcc=1e-3;Rprim=1.4;Rsec=6.9e-3;
Vdd=710; cshunt=7.9e-9;

%call the file and sweep the freq of triangular wave block
%from 29kHz to 31kHz with .5kHz increments

set_param('halfLoadwoRec30/PWM/Triangle','Freq','29e3')
sim('halfLoadwoRec30')

figure('name','Constant Load - Varying Freq: Time vs. Ouput Voltage','units','normalized','outerposition',[0 0 1 1])

h=plot(t,Vout); l='29kHz';
hold on;
%calculating efficiency n
fs=str2num(get_param('halfLoadwoRec30/PWM/Triangle','Freq'));
Pdiss = ([max(Irms)*sqrt(2)]^2)*[(Rs1/4)+(Rcs/8)+(Rlf/2)+(Rcf/2)+(Rcc/2)+(Rprim/2)+(Rsec*128)];
Pout=max(Vout)*max(Iout);
n=Pout/(Pout+Pdiss);
set_param('halfLoadwoRec30/PWM/Triangle','Freq','29.5e3')
sim('halfLoadwoRec30')
h1=plot(t,Vout); l1='29.5kHz';
```

```
hold on;
%calculating efficiency n1
fs1=str2num(get_param('halfLoadwoRec30/PWM/Triangle','Freq'));

Pdiss = ([max(Irms)*sqrt(2)]^2)*[(Rs1/4)+(Rcs/8)+(Rlf/2)+(Rcf/2)+(Rcc/2)+(Rprim/2)+(Rsec*128)];
Pout=max(Vout)*max(Iout);
n1=Pout/(Pout+Pdiss);

set_param('halfLoadwoRec30/PWM/Triangle','Freq','30e3')
sim('halfLoadwoRec30')
h2=plot(t,Vout); l2='30kHz';
hold on;
%calculating efficiency n2
fs2=str2num(get_param('halfLoadwoRec30/PWM/Triangle','Freq'));
Pdiss = ([max(Irms)*sqrt(2)]^2)*[(Rs1/4)+(Rcs/8)+(Rlf/2)+(Rcf/2)+(Rcc/2)+(Rprim/2)+(Rsec*128)];
Pout=max(Vout)*max(Iout);
n2=Pout/(Pout+Pdiss);

set_param('halfLoadwoRec30/PWM/Triangle','Freq','30.5e3')
sim('halfLoadwoRec30')
h3=plot(t,Vout); l3='30.5kHz';
hold on;
%calculating efficiency n3
fs3=str2num(get_param('halfLoadwoRec30/PWM/Triangle','Freq'));
Pdiss = ([max(Irms)*sqrt(2)]^2)*[(Rs1/4)+(Rcs/8)+(Rlf/2)+(Rcf/2)+(Rcc/2)+(Rprim/2)+(Rsec*128)];
Pout=max(Vout)*max(Iout);
n3=Pout/(Pout+Pdiss);

set_param('halfLoadwoRec30/PWM/Triangle','Freq','31e3')
sim('halfLoadwoRec30')
h4=plot(t,Vout); l4='31kHz';
hold on;
%calculating efficiency n4
fs4=str2num(get_param('halfLoadwoRec30/PWM/Triangle','Freq'));
Pdiss = ([max(Irms)*sqrt(2)]^2)*[(Rs1/4)+(Rcs/8)+(Rlf/2)+(Rcf/2)+(Rcc/2)+(Rprim/2)+(Rsec*128)];
Pout=max(Vout)*max(Iout);
n4=Pout/(Pout+Pdiss);

xlabel('Simulation Time in [sec]');
ylabel('Output Voltage in [V]');
grid on;
legend([h,h1,h2,h3,h4],l,l1,l2,l3,l4, 'Location', 'northwest','Orientation', 'vertical')

%plotting second figure
figure('name','Constant Load - Varying Freq: Freq. vs. Efficiency','units','normalized','outerposition',[0 0 1 1])
frange = [fs,fs1,fs2,fs3,fs4];
nrange=[n,n1,n2,n3,n4];
p=plot(frange,nrange,'r*-');
ylabel('Efficiency in [%]');
xlabel('Frequency in [kHz]');
```

Table 4.2: Matlab Code to Plot Efficiency vs. Frequency

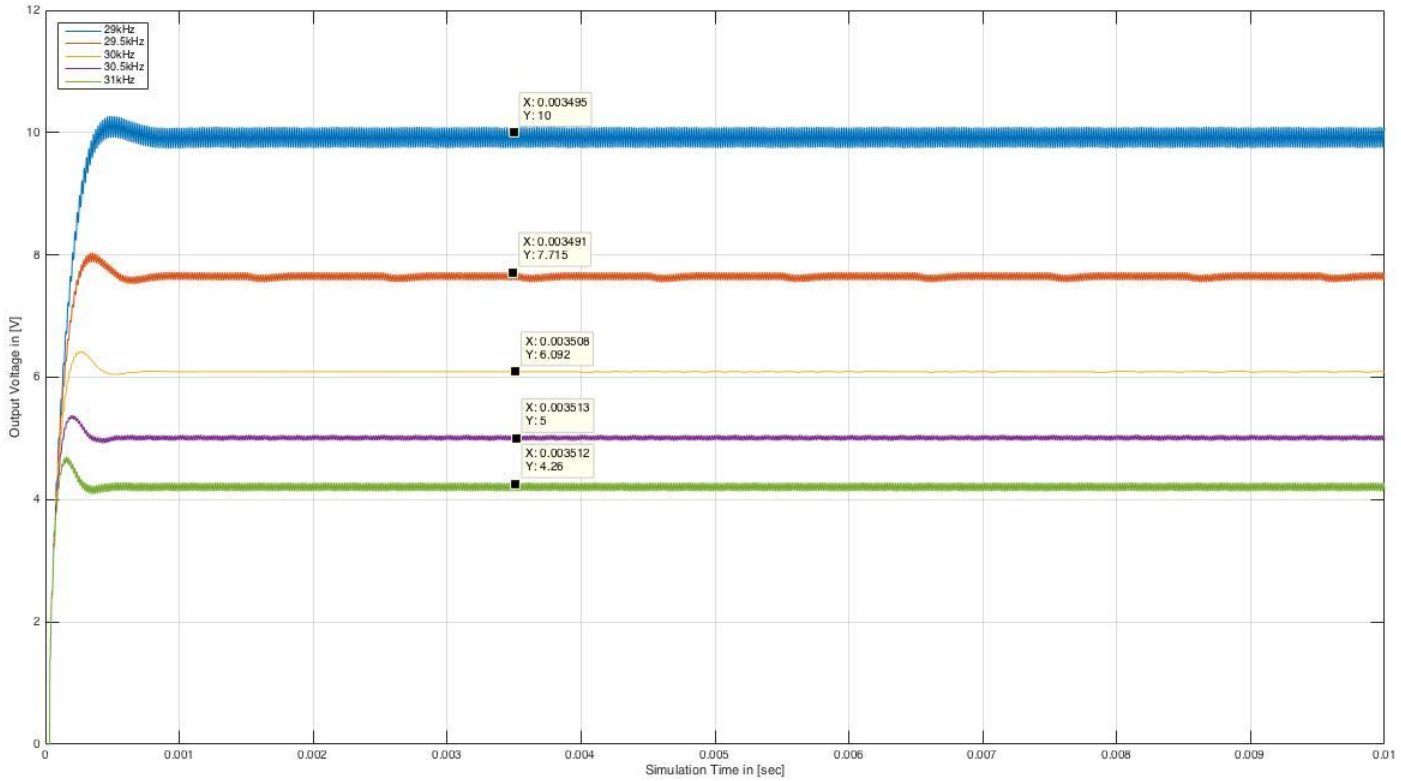

Figure 4.9: Output Voltage vs. Time with Variable Switching Frequency of Half Load Design Run Under Full Load Condition

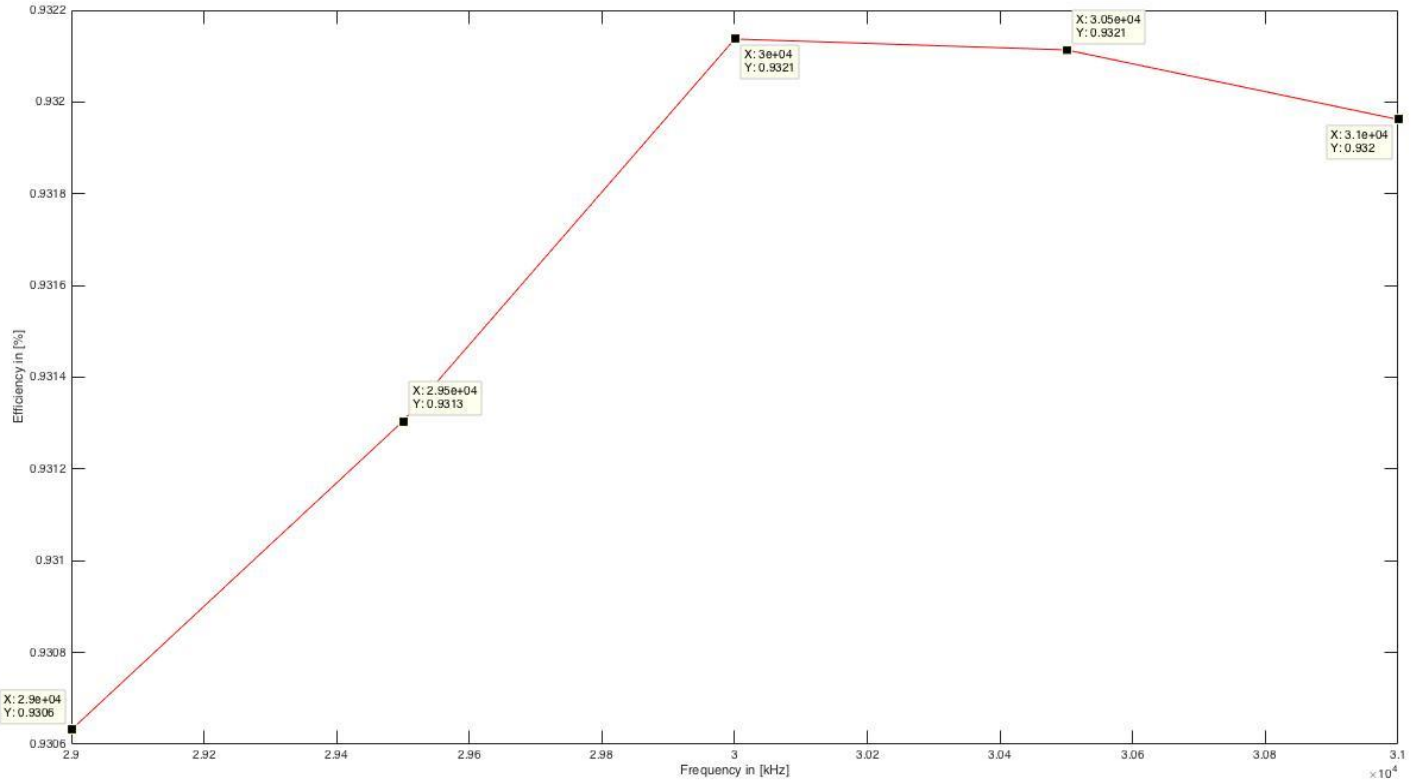

Figure 4.10: Efficiency vs. Frequency of Half Load Design Run Under Full Load Condition

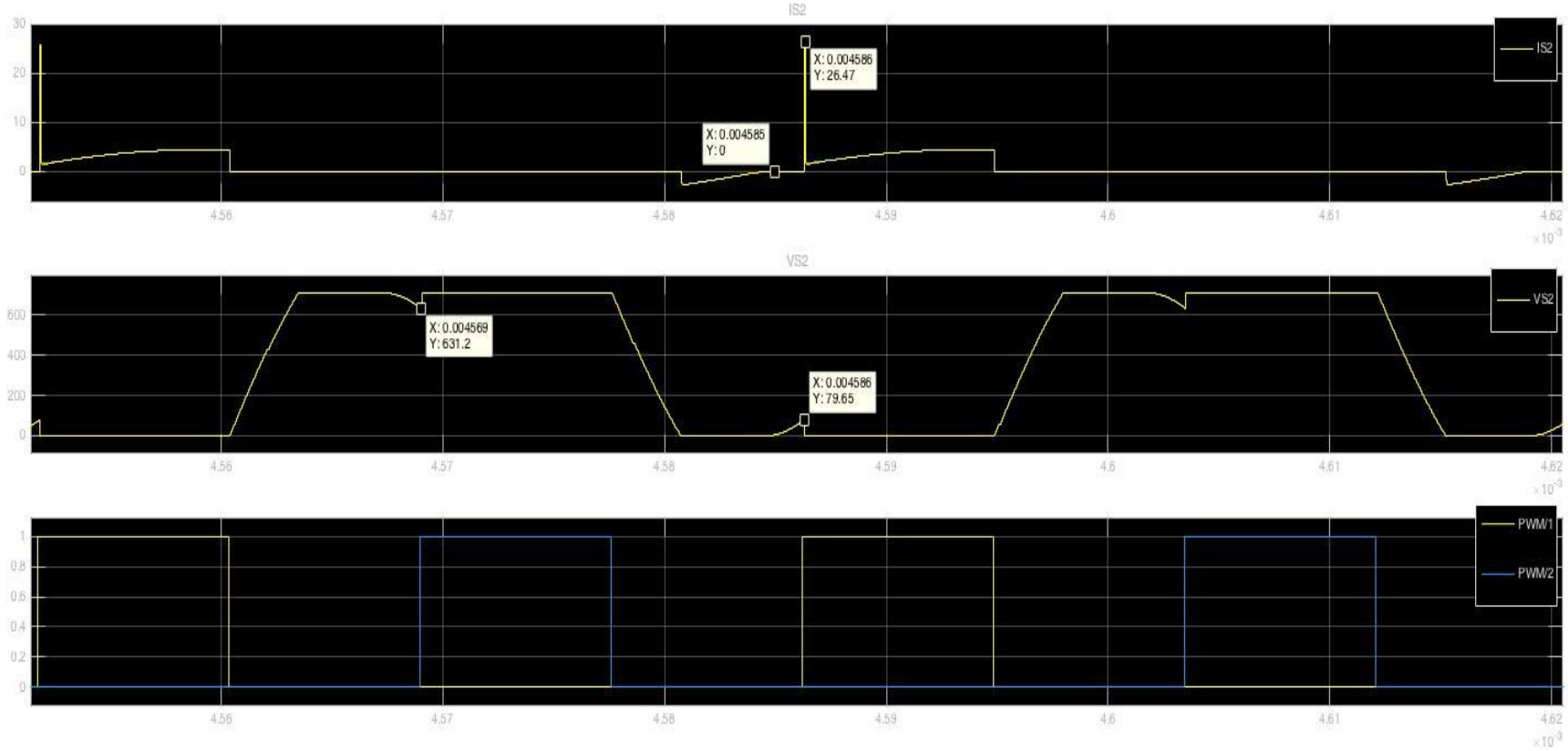

Figure 4.11: Distorted Current, Distorted Voltage, PWM (top to bottom) vs. Time Waveforms of Top Switch S_2 for Half Load Design Run Under Full Load Condition at 29kHz and 25% Duty Cycle

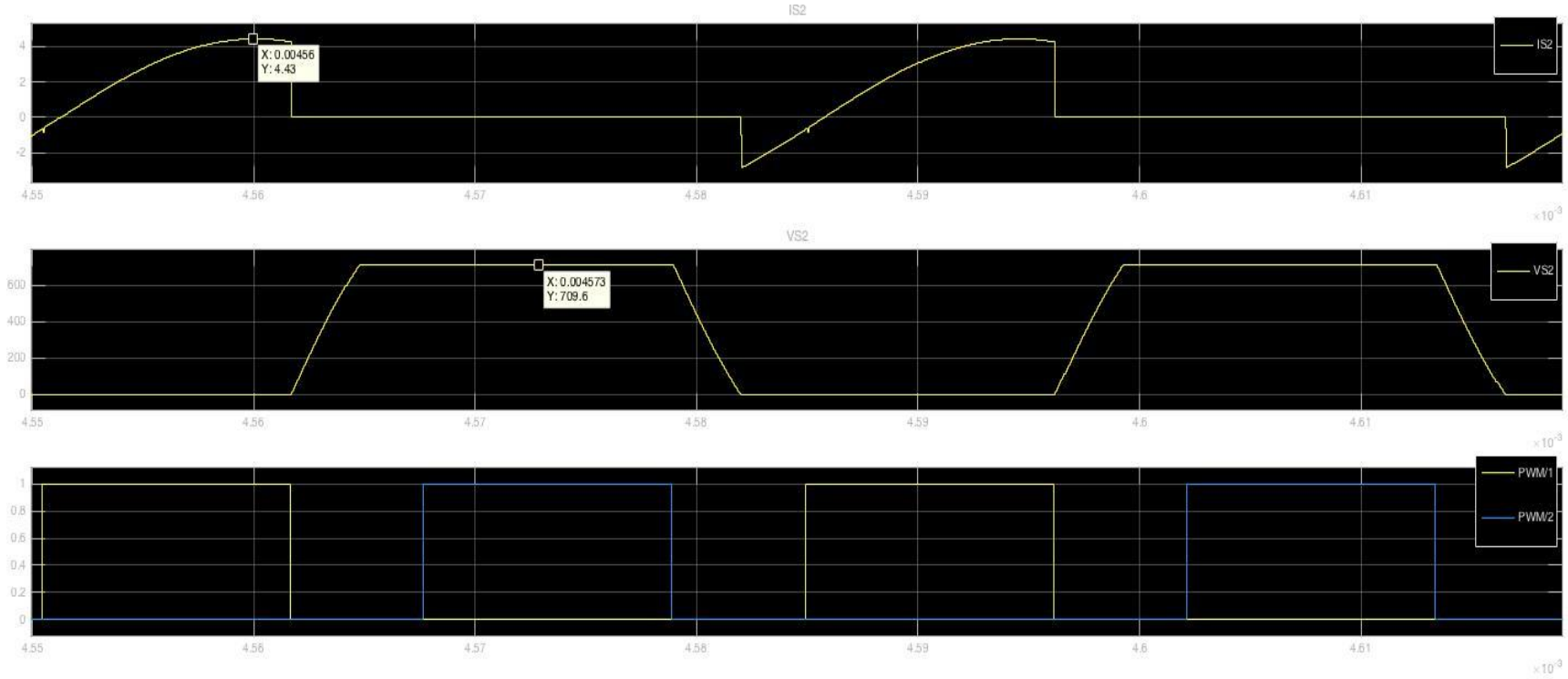

Figure 4.12: Restored Current, Voltage, PWM (top to bottom) vs. Time Waveforms of Top Switch S_2 for Half Load Design Run Under Full Load Condition at 29kHz and 35% Duty Cycle

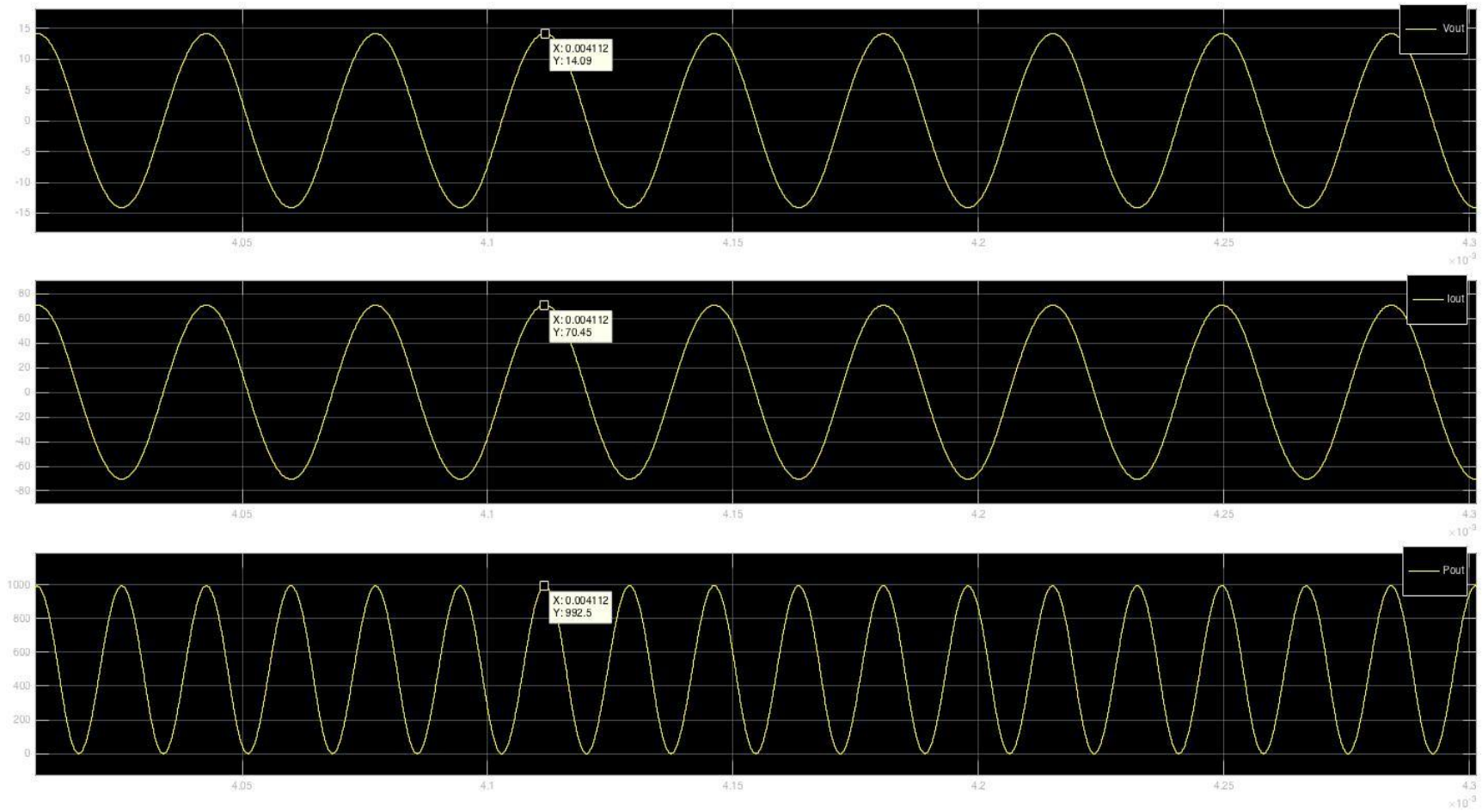

Figure 4.13: Voltage, Current, PWM (top to bottom) vs. Time Waveforms of the Output for Half Load Design Run Under Full Load Condition at 29kHz and 35% Duty Cycle

Distorted waveforms, as seen in figure 4.11, do not quiet match the properties of high efficiency class-DE power amplifiers. Indeed, there was zero distortion on the waveforms before changing frequency from 30kHz to 29kHz. Yet, output voltage level was not sufficient enough. Any distortion on the circuit components would eventually harm the system and drop the efficiency. In order to overcome this problem, changing duty cycle percentage was brainstormed. Even though duty cycle for class-DE applications is considered to be constant at 25%, it is found appropriate to vary the duty cycle for this project needs.

After increasing the duty cycle to 35% for each transistor, the distortion problem is overcome as seen in figure 4.12. The current and voltage waveforms appear as expected besides the curve in the rising part of the voltage waveform loses its visible angle as compared to very first class-DE voltage waveform. Under these operating conditions, calculated overall system efficiency becomes 95.7%.

This type of control method can be engineered in a way that, output voltage can be monitored with the help of a sensor, fed back to the PWM control block in a closed feedback. Based on voltage level, the frequency can be adjusted so as the duty cycle. In this paper, we have not stressed on the actual formulization of the control algorithm but by trial and error method, the results have been justified.

CHAPTER V

CONCLUSION

In the scope of this project we have covered a new highly efficient design of class-DE type power amplifier. This topology has been studied recently with the improvements in the wireless power systems. Under the supervision of engineers at Eaton Corp. and faculty member of UW-Milwaukee Electrical Engineering Power Electronics Group, as well as considering project requirement limitations, a system was designed and simulated in Matlab/Simulink. An inductive resonant circuit was built as per output and input side needs. As a separate project, my classmate Ethan Zimany designed inductive coupled two planar coils and their values were used in our system configuration.

Two circuits were designed and tested under different load conditions to find out the practicality of them. Our sole purpose was to achieve higher power transfer efficiency while challenging ourselves dropping down from high voltage at the input side to low voltage at the load side, and having an adaptive system for load variations. Eventually, the circuit that was designed for half load power condition is chosen to be a better system because of its reliability under both full load power and half load power scenarios. This has proven that the worst case or the optimal case would have no negative effect on the system with appropriate control techniques and methods. In both of the cases, the efficiency was kept above 90%, which is still a higher number than project minimum requirements.

This project is aimed to be used in a data center where the source will have a high voltage. For this reason, a safer work environment needed for hands-on work, maintenance, and failure tests. To provide a touch-safe system, 2mm gap between the transmitter and receiver parts was found wide enough for the type of material that will be used for the insulation. On the other

hand, having a wireless system is advantageous in a way that with the existence of load, there is power transfer. As long as there is no load attached to the system or a short circuit at the load side, the system will be ready and waiting to serve while not wasting any energy.

To conclude, some future work is needed to enhance the quality of this system. In this paper, we have covered the effect of frequency and duty cycle controls to observe the changes at the output and efficiency. However, we haven't actually defined any formulization or a code algorithm. This can be achieved by sensing the output voltage or current and transmitting this data to the receiver side to control the PWM block. One of the other needed future works could be actually building a hardware system to justify the simulation results with experimental results. In addition to all, because one of the requirements was to have a dc power at the load side, a rectifier can be added to the system as proposed in figure 2.1.

CHAPTER VI

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